# 1-wire Bus Communication Protocol

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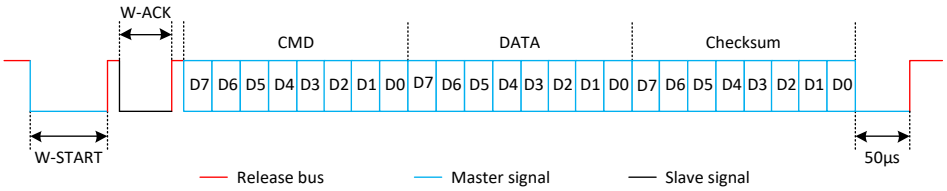
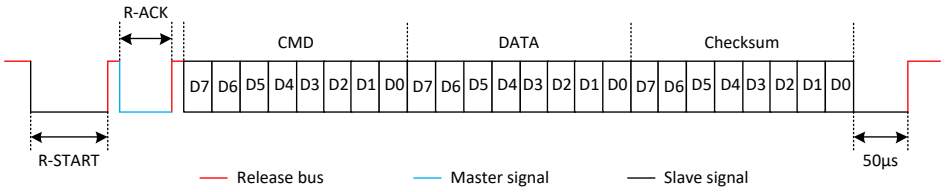
## 1-wire Bus Data Definition

The COM pin is the 1-wire communication bus between the master MCU and the BMZ00040 module. Each data frame contains 24 bits data including 8-bit command (CMD), 8-bit DATA and 8-bit Checksum. The communication timing and data format definitions are as follows.

(a) The 24-bit data format which master MCU writes to the module:
24 bits = CMD(8 bits) + DATA(8 bits) + Checksum(8 bits)




(b) The 24-bit data format which the module responds to the master MCU:
24 bits = CMD(8 bits) + DATA(8 bits) + Checksum(8 bits)




| Name | 1-wire Bus Format Definition |
|---|---|
| W-START | Inform the module to receive data: the master MCU pulls the bus low for 3~18ms to inform the module to receive data. If the bus is pulled low for more than 21ms, the module will discard this signal and no response. |
| R-START | Inform the master MCU to receive data: the module pulls the bus low for 5ms to inform the master MCU to receive data. |
| W-ACK | This ACK signal sent by the module, the low level duration is 80µs. |
| R-ACK | This ACK signal sent by the master MCU, the low level duration is 80µs. |
| CMD | This system command, contains one R/W bit<br>D7 (R/W bit): D7=0, write operation; D7=1, read operation<br>D6~D0: Command address |
| DATA | D7~D0: Data |
| Checksum | This is the Checksum, Checksum=CMD+DATA |

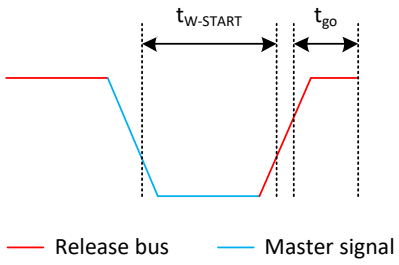
## A.C. Characteristics – 1-wire Bus

| Name | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{W\text{-}START}$ | W-START Signal Pull Low Time | 3.0 | 5.0 | 18.0 | ms |
| $t_{R\text{-}START}$ | R-START Signal Pull Low Time | 4.5 | 5.0 | 5.5 | ms |
| $t_{R\text{-}ACK}$ | R-ACK Signal Low Level Time | 75 | 80 | 85 | μs |
| $t_{W\text{-}ACK}$ | W-ACK Signal Low Level Time | 75 | 80 | 85 | μs |
| $t_{EN}$ | Module Release Bus Time | 10 | 20 | 240 | μs |
| $t_{go}$ | Master Release Bus Time | 10 | 20 | 240 | μs |
| $t_{LOW}$ | Data “0” or “1” Low Level Time | 45 | 50 | 55 | μs |
| $t_{H0}$ | Data “0” High Level Time | 22 | 27 | 33 | μs |
| $t_{H1}$ | Data “1” High Level Time | 65 | 70 | 75 | μs |
| $t_{MODUWD}$ | Write Command Cycle (full data frame) | 10 | — | — | ms |
| $t_{MODURD}$ | Read Command Cycle (full data frame) | 10 | — | — | ms |
| $t_{RR}$ | Time between Read-Command-End and Respond-Data-Start | 1 | — | 500 | μs |

## 1-wire Bus Timing Chart

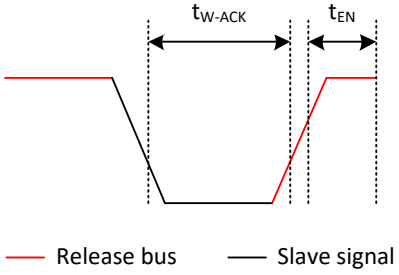
### 1. Procedure for the master to write data to the module

(a) The master sends the W-START signal: The master outputs a low level within a range of 3~18ms on the COM line, after which the bus is released.




**W-START**

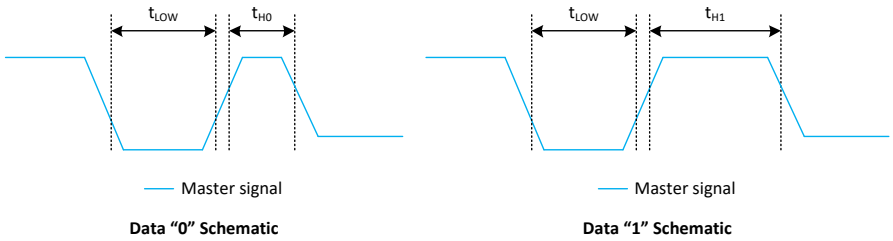
(b) The module sends a W-ACK signal: The BMZ00040 outputs a 80μs low level signal ($t_{W\text{-}ACK}$) when the bus is released, after which the module releases the bus.




**W-ACK**

(c) The master transmits 24-bit data frame: after the module sends the W-ACK signal and releases the bus, it immediately detects the bus status. If there is no data received within 240μs, i.e. the bus level remains unchanged for a 240μs timeframe, the module terminates the communication.

Data '0': 50μs low level + 27μs high level
Data '1': 50μs low level + 70μs high level




**Data "0" Schematic** **Data "1" Schematic**

(d) The master should continue to pull the bus low for 50μs after the 24 bits data has been transmitted, after which the bus is released.

- The module will not process the received command if the checksum is not correct.
- For a write-command, the module updates its internal memory according to the command, and then the command is completed.
- For a read-command, the module will respond 24 bits data frame. If the master does not send R-ACK within a 5ms timeframe, the module will terminate the command and release the bus to wait for the next communication.

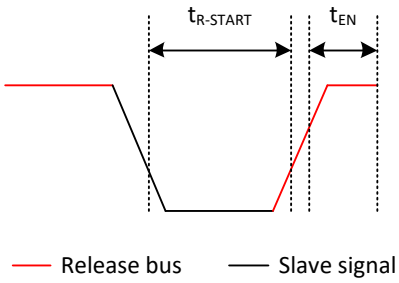
Note: 1. It is recommended that the master disables its interrupts before transmits data.

2. The period for sending a write command should not be less than the $t_{MODUWD}$ specification (10ms), otherwise an unexpected error may occur. The period for sending a read command should not be less than $t_{MODURD}$ specification (10ms), otherwise an unexpected error may occur.

**2. Procedure for the master to read data from the module**

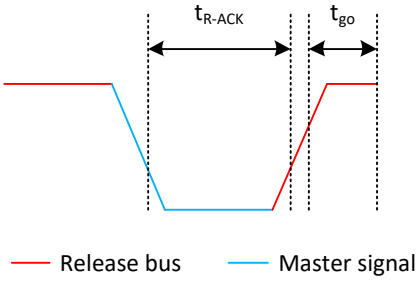
(a) The BMZ00040 will return the 24-bit data frame within 500μs after it receives a read command. If the master does not send R-ACK within a 5ms timeframe, the module will terminate the command and release the bus to wait for the next communication.

(b) The module sends the R-START signal: the COM pin is pulled low for 5ms ($t_{R\text{-}START}$), after which the bus is released.




**R-START**

(c) The master sends the R-ACK signal: After the BMZ00040 sends the R-START signal, it detects the R-ACK signal sent by the master. If the R-ACK signal is not received within 24μs, the module will discard the read command and release the bus.

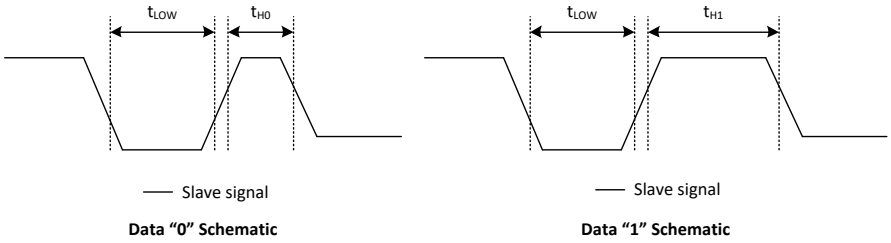



**R-ACK**

(d) The module transmits the 24 bits data frame: after the R-ACK is received, the module will immediately send the 24 bits data. If the master does not release the bus within 240μs, the module will discard the read command and release the bus.

Data '0': 50μs low level + 27μs high level

Data '1': 50μs low level + 70μs high level




**Data "0" Schematic** **Data "1" Schematic**

The module will continue to pull the bus low for 50μs after the 24 bits data has been transmitted and then release the bus.

Note: 1. It is recommended that the master performs the checksum process to avoid incorrect data (Checksum=CMD+ DATA).

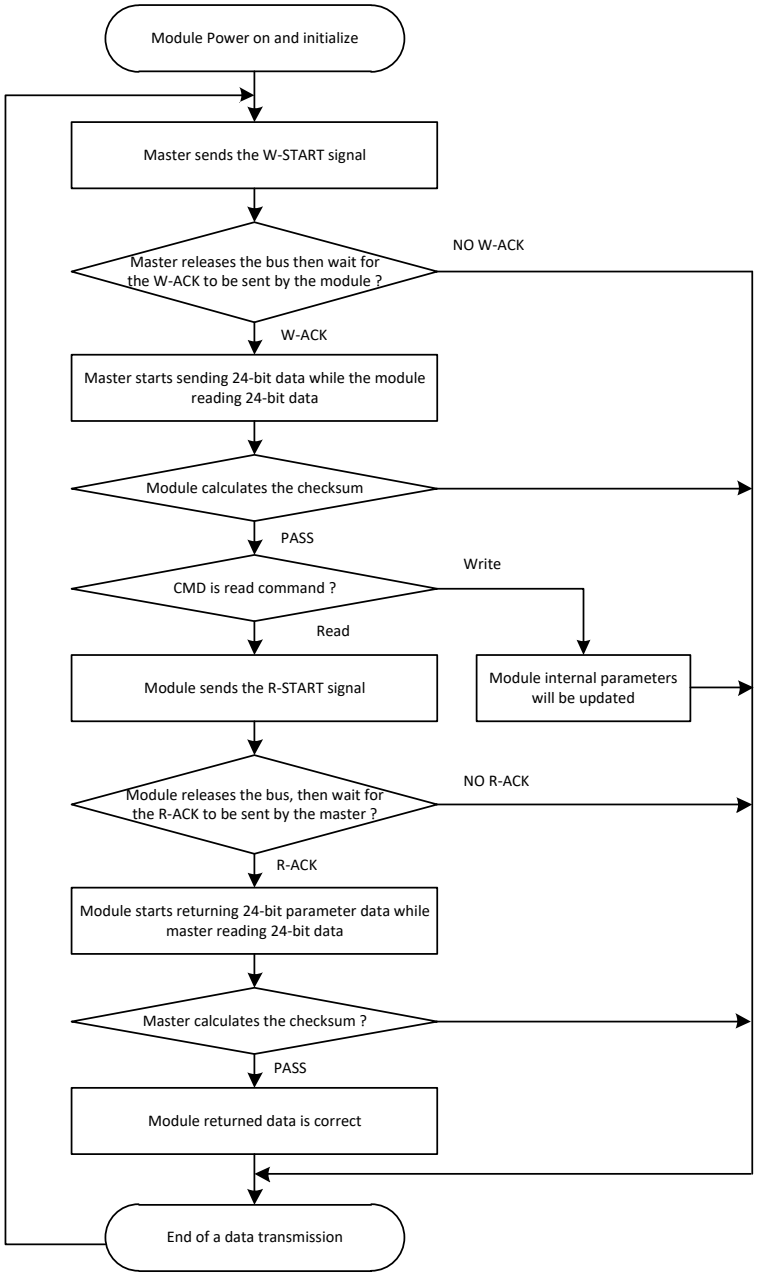
2. It is recommended that the master MCU disables its interrupts before receiving data.

## 1-wire Bus Data Processing Example

The below table lists the command sequences of setting the atomization power level to level 2.

| Function | CMD | DATA | CHCEKSUM |
|---|---|---|---|
| Send Write Command | 00000010 (02H) | 00000010(02H) | 00000100(04H) |
| Return | — | — | — |
| Send Read Command | 10000010(82H) | 00000000(00H) | 10000010(82H) |
| Return | 10000010(82H) | 00000010(02H) | 10000100(84H) |

## 1-wire Bus Read and Write Module Data Flowchart



## CMD Address Definition

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CMDRW | CMD6 | CMD5 | CMD4 | CMD3 | CMD2 | CMD1 | CMD0 |
| R/W | W | W | W | W | W | W | W | W |

Bit 7 **CMDRW**: Module registers read and write control bit
0: Write the module registers
1: Read the module registers

Bit 6~0 **CMD6~CMD0**: System command bits
0000000: Module water level detection value (Read only)
0000001: Module water level alarm value configuration (Read/Write)
0000010: Module power configuration (Read/Write)
0000011: Module fan power control (Read/Write)
0000100: Module RGB drive output control (Read/Write)
0000101: Module type (Read only)
0000110: Module firmware version (Read only)
0000111: Module serial number byte 5 (Read only)
0001000: Module serial number byte 4 (Read only)
0001001: Module serial number byte 3 (Read only)
0001010: Module serial number byte 2 (Read only)
0001011: Module serial number byte 1 (Read only)
0001100: Module serial number byte 0 (Read only)
Others: Undefined, invalid command

### CMD Command Set Summary

The following table describes the CMD command functions. Refer to the corresponding sections for each CMD details.

| R/W | CMD + DATA + Checksum | Return | Description |
|---|---|---|---|
| **WCap(RO): Module water level detection value – CMD address: 00H** | | | |
| R | 80H + 00H + Checksum | 80H + WCap + Checksum | |
| **WCal(RW): Module water level alarm value configuration – CMD address: 01H** | | | |
| W | 01H + WCal + Checksum | — | WCal: 00H~FFH |
| R | 81H + 00H + Checksum | 81H + WCal + Checksum | |
| **PCtrl(RW): Module power configuration – CMD address: 02H** | | | |
| W | 02H + PCtrl + Checksum | — | PCtrl: 00H~03H |
| R | 82H + 00H + Checksum | 82H + PCtrl + Checksum | |
| **FanCtrl(RW): Module fan power control – CMD address: 03H** | | | |
| W | 03H + FanCtrl + Checksum | — | |
| R | 83H + 00H + Checksum | 83H + FanCtrl + Checksum | |

| R/W | CMD + DATA + Checksum | Return | Description |
|---|---|---|---|
| **RGBCtrl(RW): Module RGB drive output control – CMD address: 04H** | | | |
| W | 04H + RGBCtrl + Checksum | — | |
| R | 84H + 00H + Checksum | 84H + RGBCtrl + Checksum | |
| **Type(RO): Module product ID – CMD address: 05H** | | | |
| R | 85H + 00H + Checksum | 85H + Type + Checksum | |
| **Ver(RO): Module firmware version – CMD address: 06H** | | | |
| R | 86H + 00H + Checksum | 86H + Ver + Checksum | |
| **SN5(RO): Module serial number byte 5 – CMD address: 07H** | | | |
| R | 87H + 00H + Checksum | 87H + SN5 + Checksum | |
| **SN4(RO): Module serial number byte 4 – CMD address: 08H** | | | |
| R | 88H + 00H + Checksum | 88H + SN4 + Checksum | |
| **SN3(RO): Module serial number byte 3 – CMD address: 09H** | | | |
| R | 89H + 00H + Checksum | 89H + SN3 + Checksum | |
| **SN2(RO): Module serial number byte 2 – CMD address: 0AH** | | | |
| R | 8AH + 00H + Checksum | 8AH + SN2 + Checksum | |
| **SN1(RO): Module serial number byte 1 – CMD address: 0BH** | | | |
| R | 8BH + 00H + Checksum | 8BH + SN1 + Checksum | |
| **SN0(RO): Module serial number byte 0 – CMD address: 0CH** | | | |
| R | 8CH + 00H + Checksum | 8CH + SN0 + Checksum | |

## Register Functions

1. Module water level detection value – WCap

- Module water level detection value – CMD address: 00H

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W | R | R | R | R | R | R | R | R |
| Factory value | — | — | — | — | — | — | — | — |

Bit 7~0 **D7~D0**: Module water level detection value (00H~FFH)

2. Module water level alarm value configuration – WCal

- Module water level alarm value configuration – CMD address: 01H

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Factory value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Bit 7~0 **D7~D0**: Module water level alarm value configuration (00H~FFH)

Note: 1. The water level alarm value (Wcal) is compared with the water level detection value (Wcap) to implement the water detection function, this data is still retained even when the module has no power supply..

2. The water level alarm value (Wcal) can be configured with the 1-wire communication. It can also be configured by the TP pin.

3. Module power configuration – PCtrl

- Module power configuration – CMD address: 02H

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | D1 | D0 |
| R/W | — | — | — | — | — | — | R/W | R/W |
| Factory value | — | — | — | — | — | — | 1 | 1 |

Bit 2~0 **D1~D0**: Module water atomization power configuration
00: Turn off output
01: First level power (6W)
10: Second level power (8W)
11: Third level power (10W)

4. Module fan power control – FanCtrl

- Module fan power control – CMD address: 03H

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | — | D0 |
| R/W | — | — | — | — | — | — | — | R/W |
| Factory value | — | — | — | — | — | — | — | 0 |

Bit 0 **D0**: Module fan power control
0: First level - Half-power
1: Second level - Full-power

Note: The FanCtrl data is still retained even when the module has no power supply.

5. Module RGB drive output control – RGBCtrl

- Module RGB drive output control – CMD address: 04H

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D7 | D6 | — | — | — | — | — | D0 |
| R/W | R/W | R/W | — | — | — | — | — | R/W |
| Factory value | 1 | 1 | — | — | — | — | — | 1 |

Bit 7~6 **D7~D6**: LED Streaming speed control - the higher the level, the faster the speed
00: First level
01: Second level

10: Third level
11: Fourth level

Bit 0 **D0**: RGB drive output control
0: Disable output
1: Enable output

Note: The RGBCtrl data is still retained even when the module has no power supply.

6. Module product ID – Type

- Module product ID – CMD address: 05H

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W | R | R | R | R | R | R | R | R |
| Factory value | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0 **D7~D0**: Module product ID (BMZ00040)

7. Module firmware version – Ver

- Module firmware version – CMD address: 06H

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W | R | R | R | R | R | R | R | R |
| Factory value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0 **D7~D0**: Module firmware version

8. Module serial number byte 5 – SN5

- Module serial number byte 5 – CMD address: 07H

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D47 | D46 | D45 | D44 | D43 | D42 | D41 | D40 |
| R/W | R | R | R | R | R | R | R | R |
| Factory value | — | — | — | — | — | — | — | — |

Bit 7~0 **D47~D40**: Module serial number

9. Module serial number byte 4 – SN4

- Module serial number byte 4 – CMD address: 08H

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D39 | D38 | D37 | D36 | D35 | D34 | D33 | D32 |
| R/W | R | R | R | R | R | R | R | R |
| Factory value | — | — | — | — | — | — | — | — |

Bit 7~0 **D39~D32**: Module serial number

10.Module serial number byte 3 – SN3

- Module serial number byte 3– CMD address: 09H

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 |
| R/W | R | R | R | R | R | R | R | R |
| Factory value | — | — | — | — | — | — | — | — |

Bit 7~0 **D31~D24**: Module serial number

11.Module serial number byte 2 – SN2

- Module serial number byte 2 – CMD address: 0AH

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 |
| R/W | R | R | R | R | R | R | R | R |
| Factory value | — | — | — | — | — | — | — | — |

Bit 7~0 **D23~D16**: Module serial number

12.Module serial number byte 1 – SN1

- Module serial number byte 1 – CMD address: 0BH

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| R/W | R | R | R | R | R | R | R | R |
| Factory value | — | — | — | — | — | — | — | — |

Bit 7~0 **D15~D8**: Module serial number

13.Module serial number byte 0 – SN0

- Module serial number byte 0 – CMD address: 0CH

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W | R | R | R | R | R | R | R | R |
| Factory value | — | — | — | — | — | — | — | — |

Bit 7~0 **D7~D0**: Module serial number