

Features

- Real-Time Clock (RTC) / Calendar functions
- Operating voltage: 2.0V~5.5V
- Maximum input serial clock: 500kHz at $V_{DD}=2V$, 2MHz at $V_{DD}=5V$
- Operating current:
 - ◆ less than $0.5\mu A$ at 2V
 - ◆ less than $0.7\mu A$ at 3V
 - ◆ less than $1.0\mu A$ at 5V
- TTL compatible
 - ◆ V_{IH} : $2.0V \sim V_{DD} + 0.3V$ at $V_{DD}=5V$
 - ◆ V_{IL} : $0.3V \sim +0.8V$ at $V_{DD}=5V$
- Two data transmission modes: single-byte, or burst mode
- 3-wire interface
- All registers store BCD format
- HT1380A: 8-pin DIP package
HT1381A: 8-pin SOP package

Applications

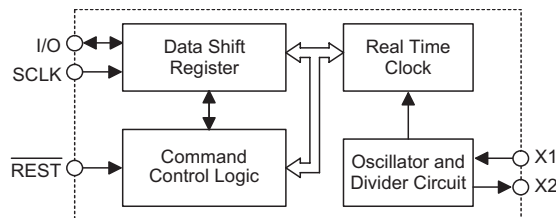
- Microcomputer serial clock
- Clock and Calendar

General Description

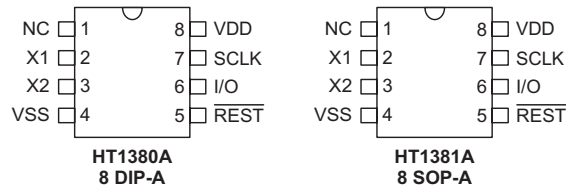
The HT1380A/HT1381A is a real time clock device which provides seconds, minutes, hours, day, date, month and year information. The number of days in each month and leap years are automatically adjusted. The HT1380A/HT1381A is designed for low power consumption and can operate in two modes: one is the 12-hour mode with an AM/PM indicator, the other is the 24-hour mode.

The HT1380A/HT1381A has several registers to store the corresponding information with 8-bit data format. A 32768Hz crystal is required to provide the correct timing. In order to minimize the pin number, the HT1380A/HT1381A use a serial I/O transmission method to interface with a microprocessor. Only three wires are required: (1) \overline{REST} , (2) SCLK and (3) I/O. Data can be delivered 1 byte at a time or in a burst of up to 8 bytes.

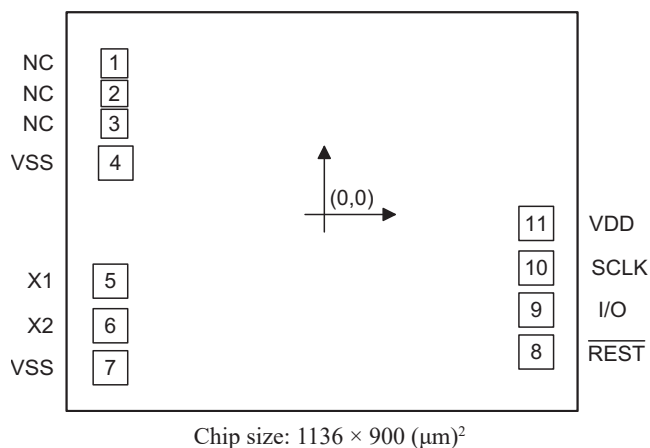
Block Diagram



Pin Assignment



Pad Assignment



* The IC substrate should be connected to VSS in the PCB layout artwork.

Pad Coordinates

Unit: μm

Pad No.	X	Y
1	-456.985	333.025
2	-456.985	264.025
3	-456.985	195.025
4	-455.590	109.935
5	-466.000	-154.955
6	-466.000	-249.955
7	-466.000	-344.955
8	465.966	-309.630
9	465.966	-214.630
10	465.966	-119.630
11	465.966	-24.630

Pad Description

Pin Name	I/O	Internal Connection	Description
VSS	–	CMOS	Negative power supply, ground
X1	I	CMOS	32768Hz crystal input pad
X2	O	CMOS	Oscillator output pad
REST	I	CMOS	Reset pin with serial transmission
I/O	I/O	CMOS	Data Input/Output pin with serial transmission
SCLK	I	CMOS	Serial Clock pulse pin with serial transmission
VDD	–	CMOS	Positive power supply

Absolute Maximum Ratings

Supply Voltage	-0.3V to 5.5V
Input Voltage	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
Storage Temperature	-60°C to 150°C
Operating Temperature	-40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

$T_a=25^\circ\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
I_{STB}	Standby Current	2V	—	—	—	100	nA
		3V		—	—	100	
		5V		—	—	100	
I_{DD}	Operating Current	2V	No load	—	0.30	0.50	μA
		3V		—	0.50	0.70	
		5V		—	0.85	1.00	
I_{OH}	Source Current	2V	$V_{OH}=1.8V$	-0.20	-0.40	—	mA
		3V	$V_{OH}=2.7V$	-0.35	-0.70	—	
		5V	$V_{OH}=4.5V$	-0.50	-1.00	—	
I_{OL}	Sink Current	2V	$V_{OL}=0.2V$	0.70	1.50	—	mA
		3V	$V_{OL}=0.3V$	1.20	2.50	—	
		5V	$V_{OL}=0.5V$	2.00	4.00	—	
V_{IH}	“H” Input Voltage	3V	—	2.00	—	—	V
		5V		2.00	—	—	
V_{IL}	“L” Input Voltage	3V	—	—	—	0.60	V
		5V		—	—	0.80	

Note: I_{STB} is specified with SCLK, I/O, $\overline{\text{REST}}$ open. The clock halt bit must be set to logic 1 (oscillator disabled).

A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
t _{DC}	Data to Clock Setup	2V	—	200	—	—	ns
		3V	—	100	—	—	
		5V	—	50	—	—	
t _{CDH}	Clock to Data Hold	2V	—	280	—	—	ns
		3V	—	140	—	—	
		5V	—	70	—	—	
t _{CDD}	Clock to Data Delay	2V	—	—	—	800	ns
		3V	—	—	—	400	
		5V	—	—	—	200	
t _{CL}	Clock Low Time	2V	—	1000	—	—	ns
		3V	—	500	—	—	
		5V	—	250	—	—	
t _{CH}	Clock High Time	2V	—	1000	—	—	ns
		3V	—	500	—	—	
		5V	—	250	—	—	
f _{SCLK}	Clock Frequency	2V	—	—	—	0.5	MHz
		3V	—	—	—	1.0	
		5V	—	—	—	2.0	
t _r /t _f	Clock Rise and Fall Time	2V	—	—	—	2000	ns
		3V	—	—	—	1000	
		5V	—	—	—	500	
t _{CC}	Reset to Clock Setup	2V	—	4	—	—	μs
		3V	—	2	—	—	
		5V	—	1	—	—	
t _{CCH}	Clock to Reset Hold	2V	—	240	—	—	ns
		3V	—	120	—	—	
		5V	—	60	—	—	
t _{CWH}	Reset Inactive Time	2V	—	4	—	—	μs
		3V	—	2	—	—	
		5V	—	1	—	—	
t _{CDZ}	Reset to I/O High Impedance	2V	—	—	—	280	ns
		3V	—	—	—	140	
		5V	—	—	—	70	

Functional Description

The HT1380A/HT1381A mainly contains the following internal elements: a data shift register array to store the clock/calendar data, command control logic, oscillator circuit and read timer clock. The clock is contained in eight read/write registers as shown below. Data contained in the clock register is in binary coded decimal format.

Two modes are available for transferring the data between the microprocessor and the HT1380A/HT1381A. One is in single-byte mode and the other is in multiple-byte mode.

The HT1380A/HT1381A also contains two additional bits, the clock halt bit (CH) and the write protect bit (WP). These bits control the operation of the oscillator and so

data can be written to the register array. These two bits should first be specified in order to read from and write to the register array properly.

Command Byte

For each data transfer, a Command Byte is initiated to specify which register is accessed. This is to determine whether a read, write, or test cycle is operated and whether a single byte or burst mode transfer is to occur. Refer to the table shown below and follow the steps to write the data to the chip. First give a Command Byte of HT1380A/HT1381A, and then write a data in the register.

This table illustrates the correlation between Command Byte and their bits:

Function Description	Command Byte							
	C7	C6	C5	C4	C3	C2	C1	C0
Select Read or Write Cycle	—	—	—	—	—	—	—	R/W
Specify the Register to be Accessed	—	—	—	—	A2	A1	A0	—
Clock Halt Flag	C	—	—	—	—	—	—	—
Software Reset	1	0	0	1	0	0	0	0
Select Single Byte or Burst Mode	1	0	1	1	1	1	1	x

Note: "x" stands for don't care

The following table shows the register address and its data format:

Register Name	Range Data	Register Definition								Address A2~A0	Bit R/W	Command Byte
		D7	D6	D5	D4	D3	D2	D1	D0			
Seconds	00~59	CH	10 SEC			SEC			000	W R	10000000 10000001	
Minutes	00~59	0	10 MIN			MIN			001	W R	10000010 10000011	
Hours	01~12 00~23	12\ 24	0 0	AP 10	HR HR	HOUR			010	W R	10000100 10000101	
Date	01~31	0	0	10 DATE		DATE			011	W R	10000110 10000111	
Month	01~12	0	0	0	10M	MONTH			100	W R	10001000 10001001	
Day	01~07	0	0	0	0	DAY			101	W R	10001010 10001011	
Year	00~99	10 YEAR			YEAR			110	W R	10001100 10001101		
Write Protect	00~80	WP	ALWAYS ZERO						111	W R	10001110 10001111	

CH: Clock Halt bit

CH=0 oscillator enabled
CH=1 oscillator disabled

WP: Write protect bit

WP=0 register data can be written in
WP=1 register data can not be written in

Bit 7 of Reg2: 12/24 mode flag

bit 7=1, 12-hour mode
bit 7=0, 24-hour mode

Bit 5 of Reg2: AM/PM mode defined

AP=1 PM mode
AP=0 AM mode

R/W Signal

The LSB of the Command Byte determines whether the data in the register be read or be written to.

When it is set as "0" means that a write cycle is to take place otherwise this chip will be set into the read mode.

A0~A2

A0 to A2 of the Command Byte is used to specify which registers are to be accessed. There are eight registers used to control the month data, etc., and each of these registers have to be set as a write cycle in the initial time.

Burst Mode

When the Command Byte is 10111110 (or 10111111), the HT1380A/HT1381A is configured in burst mode. In this mode the eight clock/calendar registers can be written (or read) in series, starting with bit 0 of register address 0 (see the timing on the next page).

Software Reset

In order to improve system stability, it is recommended to execute software reset command first after power-on. Note that the WP bit should be set to 0 first.

Software Reset is a combined command: 10010000b + 00001111b & 10010000b + 10000000b.

Write Protect Register

This register is used to prevent a write operation to any other register. Data can be written into the designated register only if the Write Protect signal (WP) is set to logic 0. The Write Protect Register should be set first before restarting the system or before writing the new data to the system, and it should set as logic 1 in the read cycle. The Write Protect bit cannot be written to in the burst mode.

Clock HALT Bit

D7 of the Seconds Register is defined as the Clock Halt Flag (CH).

When this bit is set to logic 1, the clock oscillator is stopped and the chip goes into a low-power standby mode. When this bit is written to logic 0, the clock will start.

12-hour/24-hour Mode

The D7 of the hour register is defined as the 12-hour or 24-hour mode select bit.

When this bit is in high level, the 12-hour mode is selected otherwise it's the 24-hour mode.

AM-PM Mode

These are two functions for the D5 of the hour register determined by the value D7 of the same register.

One is used in AM/PM selection on the 12-hour mode. When D5 is logic 1, it is PM, otherwise it's AM. The other is used to set the second 10-hour bit (20~23 hours) on the 24-hour mode.

Reset and Serial Clock Control

The $\overline{\text{REST}}$ pin is used to allow access data to the shift register like a toggle switch. When the $\overline{\text{REST}}$ pin is taken high, the built-in control logic is turned on and the address/command sequence can access the corresponding shift register. The $\overline{\text{REST}}$ pin is also used to terminate either single-byte or burst mode data format.

The input signal of SCLK is a sequence of a falling edge followed by a rising edge and it is used to synchronize the register data whether read or write. For data input, the data must be read after the rising edge of SCLK. The data on the I/O pin becomes output mode after the falling edge of the SCLK. All data transfer terminates if the $\overline{\text{REST}}$ pin is low and the I/O pin goes to a high impedance state. The data transfer is illustrated on the next page.

Data Input and Data Out

In writing a data byte with HT1380A/HT1381A, the read/write should first set as R/W=0 in the Command Byte and follow with the corresponding data register on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored. Data inputs are entered starting with bit 0.

In reading a data on the register of HT1380A/HT1381A, R/W=1 should first be entered as input. The data bit outputs on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted on the first falling edge after the last bit of the read command byte is written. Additional SCLK cycles re-transmits the data bytes as long as $\overline{\text{REST}}$ remains at high level. Data outputs are read starting with bit 0.

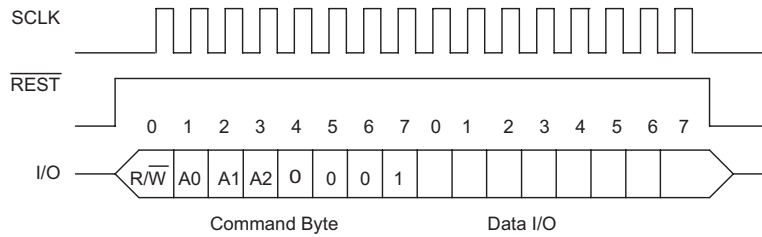
Crystal Selection

A 32768Hz crystal can be directly connected to the HT1380A/HT1381A on pins 2 and 3 which are the crystal X1 and X2 pins. In order to ensure that the desired frequency is achieved, it is recommended to use a crystal with a capacitance of 9.0pF. It is not recommended that additional load capacitors are connected to the X1 and X2 pins. Refer to the following page for the crystal specifications.

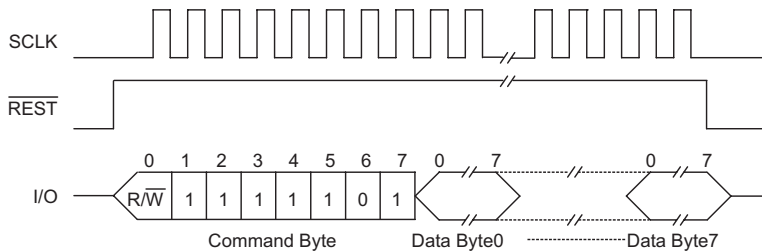


The following diagram shows the single and burst mode transfer:

Single Byte Transfer



Burst Mode Transfer



Crystal Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_0	Nominal Frequency	—	32.768	—	kHz
ESR	Series Resistance	—	—	50	k Ω
C_L	Load Capacitance	—	9.0	—	pF

Note: 1. It is strongly recommended to use a crystal with a load capacitance of 9.0pF. Never use a crystal with a load capacitance of 12.5pF.

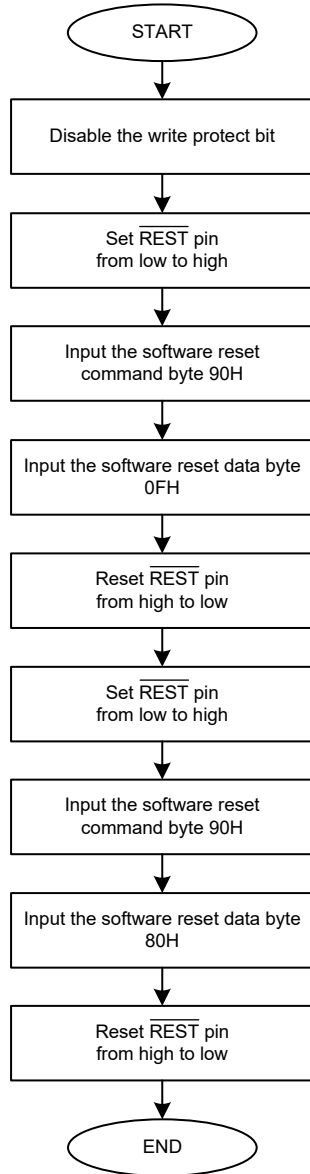
2. The oscillator selection can be optimized using a high quality resonator with a small ESR value. Refer to the crystal manufacturer for more details: www.microcrystal.com.

Operating Flowchart

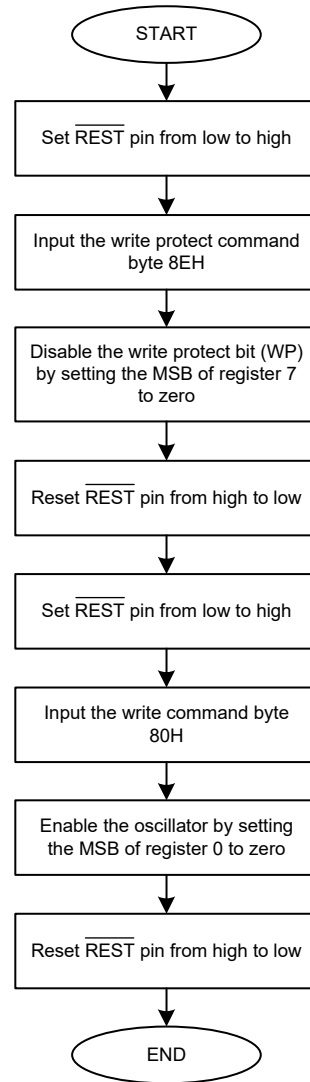
To initiate any transfer of data, $\overline{\text{REST}}$ is taken high and an 8-bit command byte is first loaded into the control logic to provide the register address and command information. Following the command word, the clock/calendar data is serially transferred to or from the corresponding register. The $\overline{\text{REST}}$ pin must be taken low again after the transfer operation is completed. All data enter on the rising edge of SCLK and outputs on the falling edge of SCLK. In total, 16 clock pulses are needed for a single byte mode and 72 for burst mode. Both input and output data starts with bit 0.

In using the HT1380A/HT1381A, set the WP to 0 and execute software rest, then set the WP and CH to 0 and wait for about 3 seconds, the oscillator will generate the clocks for internal use. Then, choose either single mode or burst mode to input the data. The read or write operating flowcharts are shown on the next page.

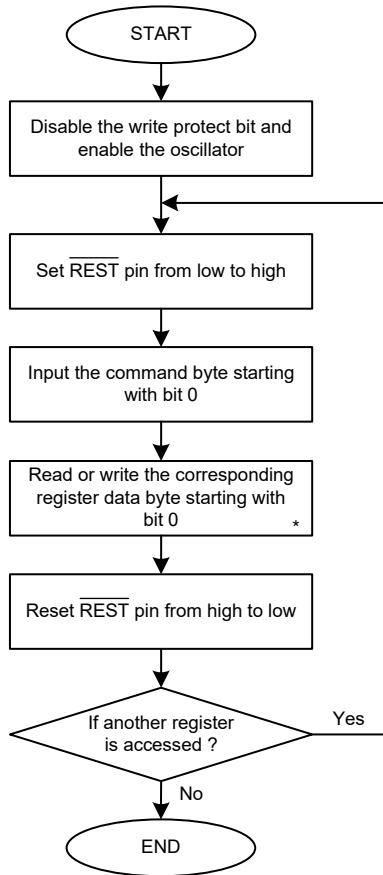
- Software reset flowchart



- To disable the write protect(WP=0) bit and enable the oscillator (CH=0) flowchart

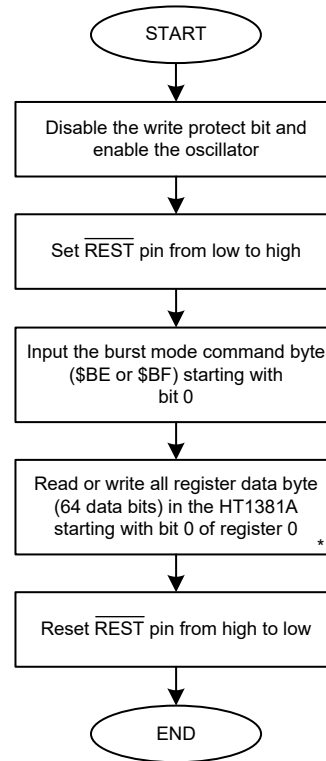


• Single byte data transfer flowchart



Note: * In reading data byte from HT1380A/HT1381A register, the first data bit to be transmitted at the first falling edge after the last bit of the command byte is written.

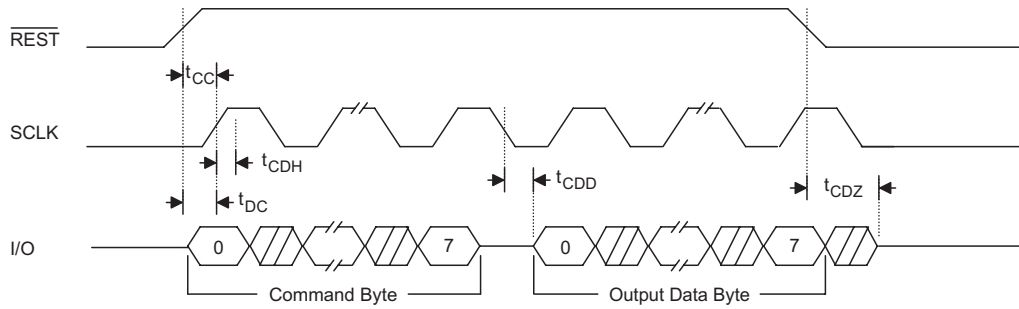
• Burst mode data transfer flowchart



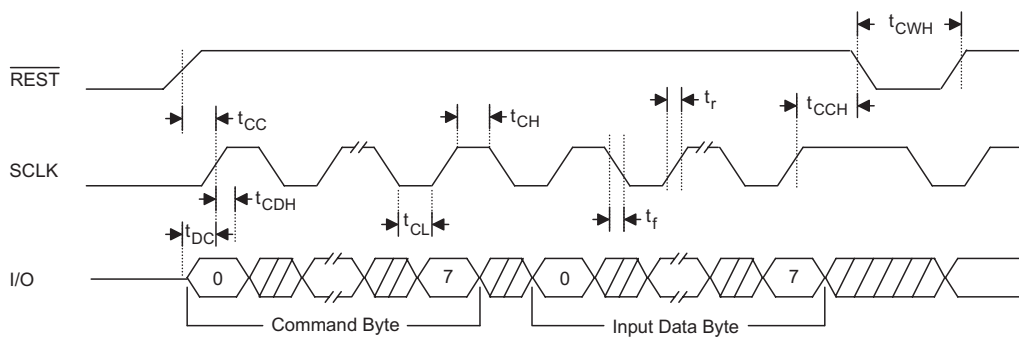
Note: * In reading data byte from HT1380A/HT1381A register, the first data bit to be transmitted at the first falling edge after the last bit of the command byte is written.

Timing Diagrams

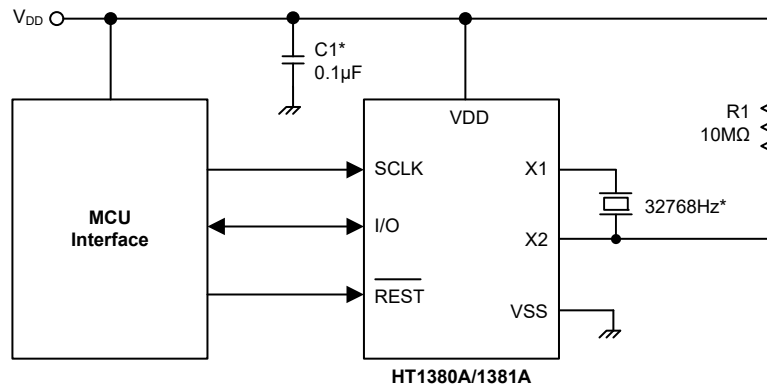
Read Data Transfer



Write Data Transfer



Application Circuit



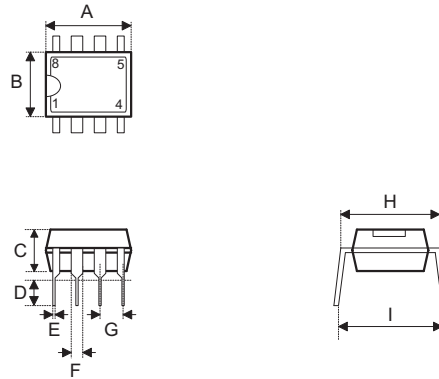
Note: * In order to obtain the correct frequency, it is recommended to use a crystal with a load capacitance of 9.0pF. It is not recommended to connect load capacitors to the X1 and X2 pins. If the power line is noisy, it is recommended to add C1 for filtering out noise.

Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the [Holtek website](#) for the latest version of the [Package Information](#).

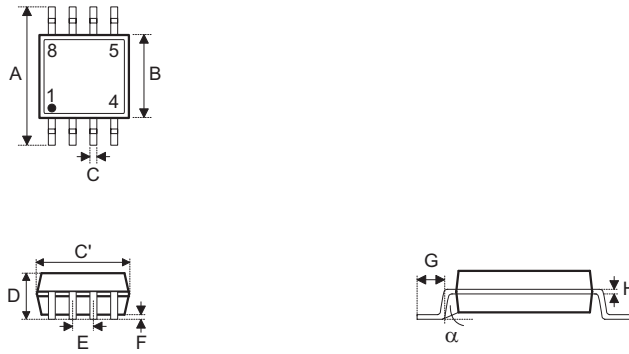
Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Materials Information
- Carton information
-

8-pin DIP (300mil) Outline Dimensions


Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.355	0.365	0.400
B	0.240	0.250	0.280
C	0.115	0.130	0.195
D	0.115	0.130	0.150
E	0.014	0.018	0.022
F	0.045	0.060	0.070
G	—	0.100 BSC	—
H	0.300	0.310	0.325
I	—	—	0.430

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	9.02	9.27	10.16
B	6.10	6.35	7.11
C	2.92	3.30	4.95
D	2.92	3.30	3.81
E	0.36	0.46	0.56
F	1.14	1.52	1.78
G	—	2.54 BSC	—
H	7.26	7.87	8.26
I	—	—	10.92

8-pin SOP (150mil) Outline Dimensions


Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.020
C'	—	0.193 BSC	—
D	—	—	0.069
E	—	0.050 BSC	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—F	6.00 BSC	—
B	—	3.90 BSC	—
C	0.31	—	0.51
C'	—	4.90 BSC	—
D	—	—	1.75
E	—	1.27 BSC	—
F	0.10	—	0.25
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°

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