4-Channel UART IC
WK2114
Register Description

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Register Description

Register List

The WK2114 registers are numbered from 000000 to 111111 according to the address, which is divided into global registers and sub-serial port registers.

There are 5 global registers, the address of the global registers are arranged in the following table.

Global Register List			
Register Address [5:0]	**Register Name**	**Type**	**Register Function Description**
000000	GENA	R/W	Global control register
000001	GRST	R/W	Global sub-serial port reset register
000010	GMUT	R/W	Global main serial port control register
010000	GIER	R/W	Global interrupt enable register
010001	GIFR	R	Global interrupt flag register

There are 16 sub-serial port registers, which are arranged as (C1,C0) and REG[3:0], the (C1,C0) bits are the sub-serial port channel number, the REG[3:0] are the register address. Refer to the following table for the specific arrangement. The descriptions are in the order of the lower 4 register addresses.

Sub-serial Port Control Register				
Register Address [3:0]	**Register Name**	**Type**	**Register Function Description**	
(C1,C0) 0011	SPAGE	R/W	Sub-serial port page control register	
(C1,C0) 0100	SCR	R/W	Sub-serial port control register	SPAGE0
(C1,C0) 0101	LCR	R/W	Sub-serial port configuration register	SPAGE0
(C1,C0) 0110	FCR	R/W	Sub-serial FIFO control register	SPAGE0
(C1,C0) 0111	SIER	R/W	Sub-serial port interrupt enable register	SPAGE0
(C1,C0) 1000	SIFR	R/W	Sub-serial port interrupt flag register	SPAGE0
(C1,C0) 1001	TFCNT	R	Sub-serial port transmitting FIFO counter register	SPAGE0
(C1,C0) 1010	RFCNT	R	Sub-serial port receiving FIFO counter register	SPAGE0
(C1,C0) 1011	FSR	R	Sub-serial port FIFO status register	SPAGE0
(C1,C0) 1100	LSR	R	Sub-serial port receiving status register	SPAGE0
(C1,C0) 1101	FDAT	R/W	Sub-serial port FIFO data register	SPAGE0
(C1,C0) 0100	BAUD1	R/W	Sub-serial port baud rate configuration register high byte	SPAGE1
(C1,C0) 0101	BAUD0	R/W	Sub-serial port baud rate configuration register low byte	SPAGE1
(C1,C0) 0110	PRES	R/W	Fractional part of the sub-serial port baud rate configuration register	SPAGE1
(C1,C0) 0111	RFTL	R/W	Sub-serial port receiving FIFO interrupt trigger configuration register	SPAGE1
(C1,C0) 1000	TFTL	R/W	Sub-serial port transmitting FIFO interrupt trigger point configuration register	SPAGE1

C1, C0: sub-serial port channel number, the 00 ~ 11 corresponding to sub-serial port 1 to sub-serial port 4 respectively.

Register Description

(1) GENA Global Control Register: (000000)

Bit	Reset Value	Function Description	Type
Bit7	1	RSV (Reserved)	R
Bit6	1	RSV (Reserved)	R
Bit5	1	RSV (Reserved)	R
Bit4	1	RSV (Reserved)	R
Bit3	0	UT4EN: Sub-serial port 4 clock enable bit (Turning off the sub-serial clock can achieve lower power consumption) 0: Disable 1: Enable	W/R
Bit2	0	UT3EN: Sub-serial port 3 clock enable bit (Turning off the sub-serial clock can achieve lower power consumption) 0: Disable 1: Enable	W/R
Bit1	0	UT2EN: Sub-serial port 2 clock enable bit (Turning off the sub-serial clock can achieve lower power consumption) 0: Disable 1: Enable	W/R
Bit0	0	UT1EN: Sub-serial port 1 clock enable bit (Turning off the sub-serial clock can achieve lower power consumption) 0: Disable 1: Enable	W/R

(2) GRST Global Sub-serial Reset Register: (000001)

Bit	Reset Value	Function Description	Type
Bit7	0	UT4SLEEP: Sub-serial port 4 sleep status bit (Reducing the power consumption, it can be automatically woken up) 0: No sleep 1: Sleep	R
Bit6	0	UT3SLEEP: Sub-serial port 3 sleep status bit (Reducing the power consumption, it can be automatically woken up) 0: No sleep 1: Sleep	R
Bit5	0	UT2SLEEP: Sub-serial port 2 sleep status bit (Reducing the power consumption, it can be automatically woken up) 0: No sleep 1: Sleep	R
Bit4	0	UT1SLEEP: Sub-serial port 1 sleep status bit (Reducing the power consumption, it can be automatically woken up) 0: No sleep 1: Sleep	R
Bit3	0	UT4RST: Sub-serial port 4 software reset control bit	W1/R0

		0: Sub-serial port 4 is not reset 1: Sub-serial port 4 is reset	
Bit2	0	UT3RST: Sub-serial port 3 software reset control bit 0: Sub-serial port 3 is not reset 1: Sub-serial port 3 is reset	W1/R0
Bit1	0	UT2RST: Sub-serial port 2 software reset control bit 0: Sub-serial port 2 is not reset 1: Sub-serial port 2 is reset	W1/R0
Bit0	0	UT1RST: Sub-serial port 1 software reset control bit 0: Sub-serial port 1 is not reset 1: Sub-serial port 1 is reset	W1/R0

(3) GMUT Global Main Serial Port Control Register: (000010)

Bit	Reset Value	Function Description	Type
Bit7	0	RSV (Reserved)	W1/R0
Bit 6~4	0	RSV (Reserved)	R0
Bit3	0	PAEN: Main serial port check enable control bit 0: No parity 1: Enable parity (Determine the parity mode according to the PAM1~PAM0 bits configuration)	W/R
Bit2~1	0	PAM1~PAM0: Main serial-port parity mode enable control bit When PAEN=1, the main serial port parity is enabled: 00: Forced 0 parity; 01: Odd parity; 10: Even parity; 11: Forced 1 parity;	W/R
Bit0	0	U1IEN: Main serial port stop bit length setting bit 0: 1bit 1: 2bits	W/R

(4) GIER Global Interrupt Register: (010000)

Bit	Reset Value	Function Description	Type
Bit7~5	000	RSV (Reserved)	R
Bit4	0	RSV (Reserved)	W/R
Bit3	0	UT4IE: Sub-serial port 4 interrupt enable control bit 0: Disable 1: Enable	W/R
Bit2	0	UT3IE: Sub-serial port 3 interrupt enable control bit 0: Disable 1: Enable	W/R
Bit1	0	UT2IE: Sub-serial port 2 interrupt enable control bit 0: Disable 1: Enable	W/R

Bit0	0	UT1IE: Sub-serial port 1 interrupt enable control bit 0: Disable 1: Enable	W/R

(5) GIFR Global Interrupt Flag Register: (010001)

Bit	Reset Value	Function Description	Type
Bit7~4	000	RSV (Reserved)	R
Bit3	0	UT4INT: Sub-serial port 4 interrupt flag bit 0: No interrupt 1: Interrupt	R
Bit2	0	UT3INT: Sub-serial port 3 interrupt flag bit 0: No interrupt 1: Interrupt	R
Bit1	0	UT2INT: Sub-serial port 2 interrupt flag bit 0: No interrupt 1: Interrupt	R
Bit0	0	UT1INT: Sub-serial port 1 interrupt flag bit 0: No interrupt 1: Interrupt	R

(6) SPAGE Sub-serial Port Page Control Register: (0011)

Bit	Reset Value	Function Description	Type
Bit7~1	000000	RSV	R
Bit0	0	PAGE: Sub-serial port page control bit (The sub-serial port registers are located in the PAGE0 and PAGE1 page, switching between the different sub-serial port pages are achieved by properly setting this bit) 0: PAGE0 1: PAGE1	W/R

(7) SCR Sub-serial Port Control Register: (PAGE0:0100)

Bit	Reset Value	Function Description	Type
Bit7~3	000	RSV	W/R
Bit2	0	SLEEPEN: Sub-serial port sleep enable bit 0: Disable 1: Enable	W/R
Bit1	0	TXEN: Sub-serial port transmitting enable bit 0: Disable 1: Enable	W/R
Bit0	0	RXEN: Sub-serial port receiving enable bit 0: Disable	W/R

		1: Enable	

(8) LCR Sub-serial Port Configuration Register: (PAGE0:0101)

Bit	Reset Value	Function Description	Type
Bit7~6	00	RSV	W/R
Bit5	0	BREAK: Sub-serial port Line-Break output control bit 0: Normal output 1: Line-Break output (TX forced output 0)	W/R
Bit4	0	IREN: Sub-serial port infrared enable bit 0: Normal mode 1: Infrared mode	W/R
Bit3	0	PAEN: Sub-serial port parity enable bit 0: No parity bit (8 bits data) 1: Parity bit (9 bits data)	W/R
Bit2~1	0	PAM1~PAM 0: Sub-serial port check mode selection bit When PAEN=1, the sub-serial port check is enabled: 00: 0 parity; 01: Odd parity; 10: Even parity; 11: 1 parity	W/R
Bit0	0	STPL: Sub-serial stop bit length control bit 0: 1bit 1: 2bits	W/R

(9) FCR Sub-serial Port FIFO Control Register: (PAGE0:0110)

Bit	Reset Value	Function Description	Type
Bit7~6	00	TFTRIG[1:0]: Sub-serial port transmitting FIFO trigger setting bit When TFTL[7:0] = 0: 00: 8-Byte 01:16-Byte 10: 24-Byte 11:30-Byte	W/R
Bit5~4	00	RFTRIG[1:0]: Sub-serial port receiving FIFO trigger setting bit When RFTL[7:0] = 0: 00: 8-Byte 01:16-Byte 10: 24-Byte 11:28-Byte	W/R
Bit3	0	TFEN: Sub-serial port transmitting FIFO enable bit 0: Disable 1: Enable	W/R
Bit2	0	RFEN: Sub-serial port receiving FIFO enable bit 0: Disable 1: Enable	W/R
Bit1	0	TFRST: Sub-serial port transmitting FIFO reset bit (This bit is reset by writing 1, and automatically cleared to 0 after completion) 0: Disable reset 1: Reset FIFO	W1/R0

Bit0	0	RFRST: Sub-serial port receiving FIFO reset bit (This bit is reset by writing 1, and automatically cleared to 0 after completion) 0: Disable reset 1: Reset FIFO	W1/R0

(10) SIER Sub-serial Port Interrupt Enable Register: (PAGE0:0111)

Bit	Reset Value	Function Description	Type
Bit7	0	FERR_IEN: Receiving FIFO data error interrupt enable bit 0: Disable receiving FIFO data error interrupt 1: Enable receiving FIFO data error interrupt	W/R
Bit6	0	RSV (Reserved)	W/R
Bit5	0	RSV (Reserved)	W/R
Bit4	0	RSV (Reserved)	W/R
Bit3	0	TFEMPTY_IEN: Transmitting FIFO empty interrupt enable bit 0: Disable transmitting FIFO empty interrupt 1: Enable transmitting FIFO empty interrupt	W/R
Bit2	0	TFTRIG_IEN: Transmitting FIFO trigger interrupt enable bit 0: Disable transmitting FIFO trigger interrupt 1: Enable transmitting FIFO trigger interrupt	W/R
Bit1	0	RXOVT_IEN : Receiving FIFO timeout interrupt enable bit 0: Disable receiving FIFO timeout interrupt 1: Enable receiving FIFO timeout interrupt	W/R
Bit0	0	RFTRIG_IEN: Receiving FIFO trigger interrupt enable bit 0: Disable receiving FIFO trigger interrupt 1: Enable receiving FIFO trigger interrupt	W/R

(11) SIFR Sub-serial Port Interrupt Flag Register: (PAGE0:1000)

Bit	Reset Value	Function Description	Type
Bit7	0	FERR_INT: Receiving FIFO data error interrupt flag bit 0: No receiving FIFO data error interrupt 1: Receiving FIFO data error interrupt	W/R
Bit6	0	RSV (Reserved)	W/R
Bit5	0	RSV (Reserved)	W/R
Bit4	0	RSV (Reserved)	W/R
Bit3	0	TFEMPTY_ INT: Transmitting FIFO interrupt flag bit 0: No transmitting FIFO empty interrupt 1: Transmitting FIFO empty interrupt	W/R
Bit2		TFTRIG_ INT: Transmitting FIFO trigger interrupt flag bit 0: No transmitting FIFO trigger interrupt 1: Transmitting FIFO trigger interrupt	W/R
Bit1		RXOVT_ INT: Receiving FIFO timeout interrupt flag bit	W/R

		0: No receiving FIFO timeout interrupt 1: Receiving FIFO timeout interrupt	
Bit0	0	RFTRIG_ INT: Receiving FIFO trigger interrupt flag bit 0: No receiving FIFO trigger interrupt 1: Receiving FIFO trigger interrupt	W/R

(12) TFCNT Sub-serial Port Transmitting FIFO Counter Register: (PAGE0:1001)

Bit	Reset Value	Function Description	Type
Bit7~0	00000000	Number of data in the FIFO transmitted by the sub-serial port	R

(13) RFCNT Sub-serial Port Receiving FIFO Counter Register: (PAGE0:1010)

Bit	Reset Value	Function Description	Type
Bit7~0	00000000	Number of data in the FIFO received by the sub-serial port	

(14) FSR Sub-serial Port FIFO Status Register: (PAGE0:1011)

Bit	Reset Value	Function Description	Type
Bit7	0	RFOE: Sub-serial port receiving FIFO data overflow error flag bit 0: No OE error 1: OE error	R
Bit6	0	RFBI: Sub-serial port receiving FIFO data with the Line-Break error 0: No Line-Break error 1: Line-Break error (RX signal is always 0, including parity bit and stop bit)	W/R
Bit5	0	RFFE: Sub-serial port receiving FIFO data frame error flag bit 0: No FE error 1: FE error	W/R
Bit4	0	RFPE: Sub-serial port receiving FIFO data check error flag bit 0: No PE error 1: PE error	W/R
Bit3	0	RDAT: Sub-serial port receiving FIFO empty flag bit 0: Sub-serial port receiving FIFO is empty 1: Sub-serial port receiving FIFO is not empty	W/R
Bit2	0	TDAT: Sub-serial port transmitting FIFO empty flag bit 0: Sub-serial port transmitting FIFO is empty 1: Sub-serial port transmitting FIFO is not empty	W/R
Bit1	0	TFULL: Sub-serial port transmitting FIFO full flag bit 0: Sub-serial port transmitting FIFO is not full 1: Sub-serial port transmitting FIFO is full	W/R
Bit0	0	The sub-serial port transmitting TX busy flag bit 0: Sub-serial port transmitting TX is empty 1: Sub-serial port transmitting TX is busy	W/R

(15) LSR Sub-serial Port Receiving Status Register: (PAGE0:1100)

Bit	Reset Value	Function Description	Type
Bit7~4	0	RSV (Reserved)	R
Bit3	0	OE: Sub-serial port receiving FIFO current read byte overflow error flag bit 0: No OE error 1: OE error	R
Bit2	0	BI: Sub-serial port receiving FIFO current read byte Line-Break error flag bit 0: No Line-Break error 1: Line-Break error (RX signal is always 0, including parity bit and stop bit)	R
Bit1	0	FE: Sub-serial port receiving FIFO current read byte frame error flag bit 0: No FE error 1: FE error	R
Bit0	0	PE: Sub-serial port receiving FIFO current read byte error check flag bit 0: No PE error 1: PE error	R

(16) FDAT Sub-serial Port FIFO Data Register: (PAGE0:1101)

Bit	Reset Value	Function Description	Type
Bit7~0	00000000	Write function: Write the FIFO data send by the sub-serial port Read function: Read the FIFO data received by the sub-serial port	W/R

(17) BAUD1 Sub-serial Port Baud Rate Configuration Register High Byte: (PAGE1:0100)

Bit	Reset Value	Function Description	Type
Bit7~0	00000000	BAUD[15:8]: Sub-serial port baud rate configuration register high bytes	W/R

(18) BAUD0 Sub-serial Port Baud Rate Configuration Register Low Byte: (PAGE1:0101)

Bit	Reset Value	Function Description	Type
Bit7~0	00000000	BAUD[7:0]: Sub-serial port baud rate configuration register low bytes	W/R

(19) PRES Sub-serial Port Baud Rate Configuration Register Fractional Part: (PAGE1:0110)

Bit	Reset Value	Function Description	Type
Bit7~4	0000	RSV	R
Bit3~0	0000	PRES[3:0]	W/R

(20) RFTL Sub-serial Port Receiving FIFO Trigger Interrupt Register: (PAGE1:0111)

Bit	Reset Value	Function Description	Type
Bit7~0	00000000	Receiving FIFO trigger control	W/R

(21) TFTL Sub-serial Port Transmitting FIFO Trigger Interrupt Register: (PAGE1:1000)

Bit	Reset Value	Function Description	Type
Bit7~0	00000000	Transmitting FIFO trigger control	W/R