RGB LED 8×8 Module

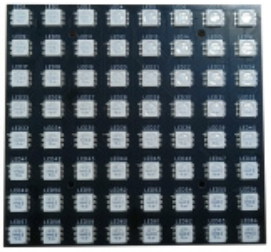
BM32D2021-1

Revision: V1.00 Date: March 12, 2024

www.bestmodulescorp.com

Table of Contents

Features



- V_{DD} operating voltage: 2.7V~5.5V
- Static operating current: 12μA @ 5V
- LED driver
  - LED_V_{DD} operating voltage: 4.5V~5.5V
  - Driving current: 550mA(MAX) @ 5.0V (Constant current ratio=48mA, white light, highest brightness)
  - Drive IC: HT16D33B
- RGB LEDs display function
  - 16 million colours when the RGB is in full colour
  - Brightness: 256-level adjustment
  - 16-level (3mA~48mA) constant current adjustment
- 64 RGB LEDs: 8×8 matrix layout
- Cascade function: can be cascaded
- Maximum cascading number: 4
- Communication Interface
  - BMCOM interface × 2 (SYNC, SCL, SDA, VDD, GND)
  - Communication mode: I^2C (Address: 0x2E+0x64~67 (select 1 of 4))
- Provides Arduino Library application support
- Module size: 79mm×73mm×8mm

General Description

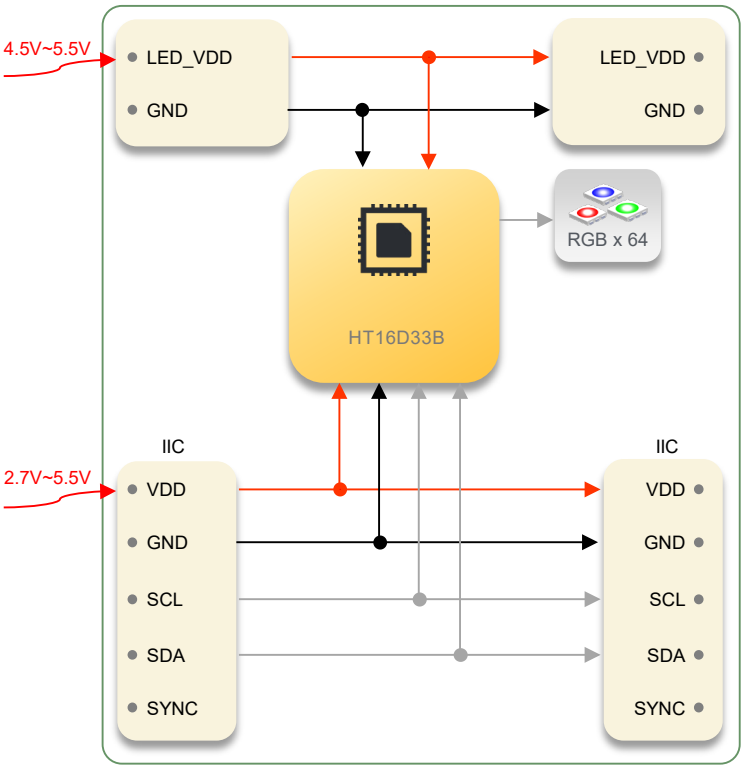
The BM32D2021-1 is a RGB LED 8×8 dot matrix module, which uses the HT16D33B LED driver chip and supports up to 256 LEDs driver. The design of this module shares 64 RGB LEDs and has a total of 192 LEDs control.

The module includes an I^2C communication interface, which can be configured with up to 4 I^2C addresses to achieve RGB control.

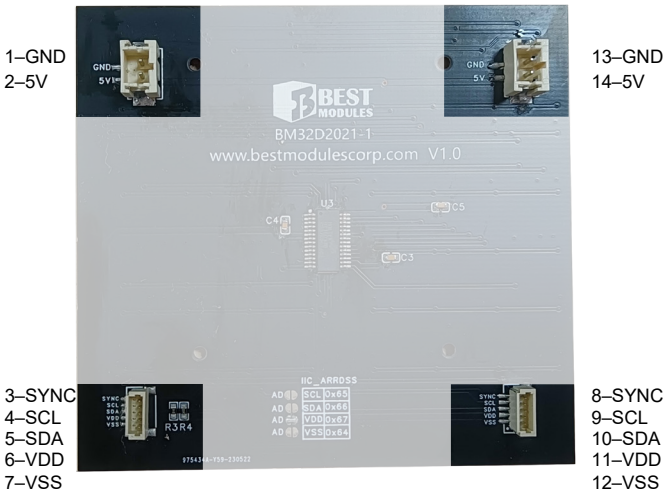
Applications

- Indicator
- Advertising light
- Dimming light

Block Diagram



Pin Assignment



Pin Description

Power supply pins:

Pin	Function	Description
2&14	LED_VDD	LED positive power supply
1&13	GND	LED negative power supply, ground

Communication interface pins:

Pin	Function	Description
3&8	SYNC	—
4&9	SCL	I²C clock line
5&10	SDA	I²C data line
6&11	VDD	Positive power supply
7&12	VSS	Negative power supply, ground

Technical Specifications

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V~V_{SS}+6.0V

Input Voltage ..... V_{SS}-0.3V~V_{DD}+0.3V

Storage Temperature..... -50℃~125℃

Operating (Ambient) Temperature ..... -40℃~85℃

Total power consumption (Max.) 3.025W

Note: Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of the device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Electrical Characteristics

Ta=25°C, V_{DD}=5V

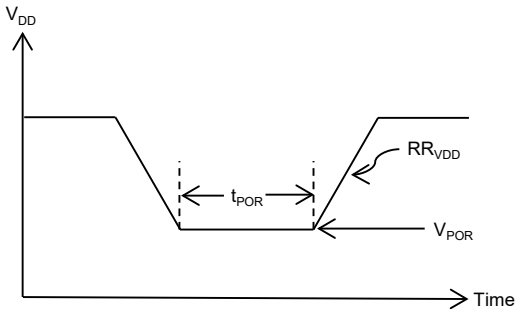
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	—	2.7	5.0	5.5	V
LED_V_{DD}	LED Operating Voltage	—	4.5	5.0	5.5	V
I_{LED_VDD}	Standby Current	Constant current ratio=48mA, white light, highest brightness	—	500	550	mA
V_{IL}	Input Low Voltage	—	0	—	0.3V_{DD}	V
V_{IH}	Input High Voltage	—	0.7V_{DD}	—	5.0	V

A.C. Electrical Characteristics

System Timing

Ta=25°C, V_{DD}=2.7~5V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{SYS}	System Clock	On-chip RC oscillator	2.1	2.4	2.7	MHz
f_{LED}	LED Frame Rate	Matrix-type 3 (16×16)	—	551	—	Hz
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	—	0	—	100	mV
RR_{VDD}	V_{DD} Rise Rate to Ensure Power-on Reset	—	0.05	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} Stay at V_{POR} to Ensure Power- on reset	—	10	—	—	ms

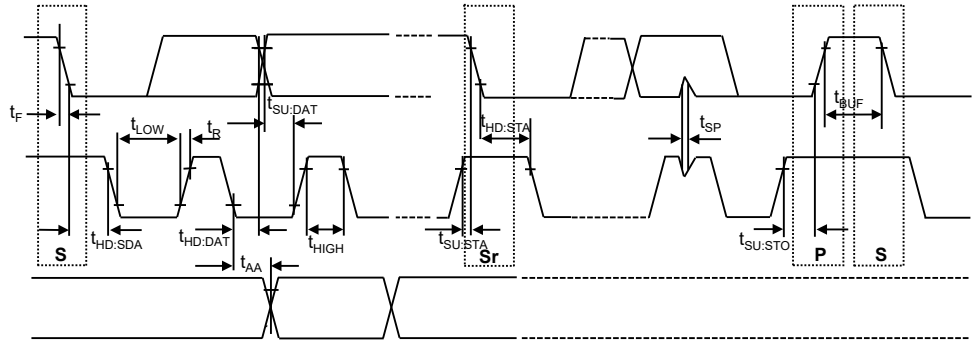


I²C Interface

Ta=25°C, V_{DD}=5V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	Clock Frequency	—	—	—	400	kHz
t_{BUF}	Bus Free Time	Time in which the bus must be free before a new transmission can start	1.3	—	—	μs
$t_{HD: STA}$	Start Condition Hold Time	After this period, the first clock pulse is generated	0.6	—	—	μs
t_{LOW}	SCL Low Time	—	1.3	—	—	μs
t_{HIGH}	SCL High Time	—	0.6	—	—	μs
$t_{SU: STA}$	Start Condition Setup Time	Only relevant for repeated START condition	0.6	—	—	μs
$t_{HD: DAT}$	Data Hold Time	—	0	—	—	ns
$t_{SU: DAT}$	Data Setup Time	—	100	—	—	ns
t_R	SDA and SCL Rise Time (Note)	—	—	—	0.3	μs
t_F	SDA and SCL Fall Time(Note)	—	—	—	0.3	μs
$t_{SU: STO}$	Stop Condition Setup Time	—	0.6	—	—	μs
t_{AA}	Output Valid from SCL is Low	—	—	—	0.9	μs
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	—	20	ns

Note: These parameters are periodically sampled but not 100% tested.



I²C Timing Diagram

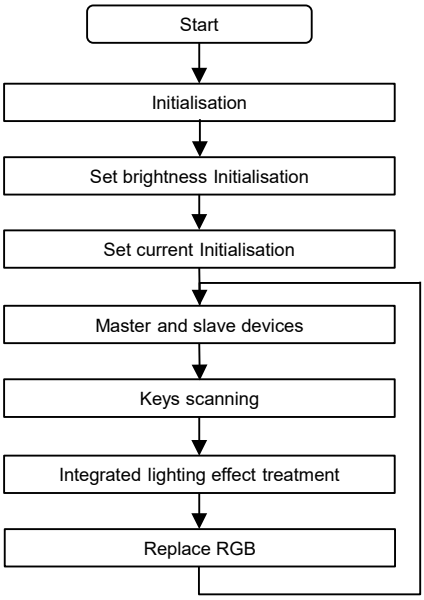
Functional Description

System Description

The BM32D2021-1 is a RGB LED 8×8 module that can be directly connected to the BMduino BMCOM interface. This module uses the HT16D33B LED driver chip and supports up to 256 LED drivers. The design of this module shares 64 RGB LEDs and has a total of 192 LEDs control.

Operating Principle

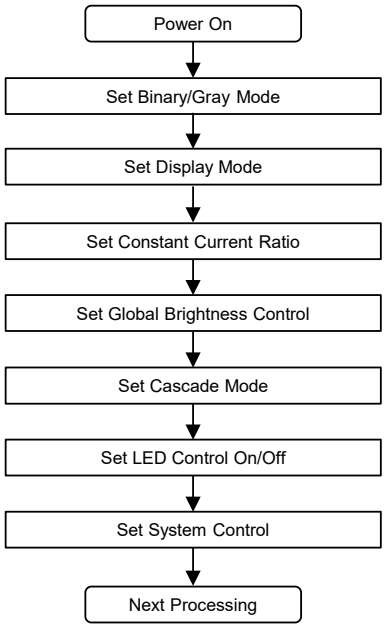
The system controls 64 RGB LEDs on/off. The HT16D33B uses 16 I/O ports to read the 64 LEDs. The higher 8-bit take turns to output the low level for progressive scanning the matrix LED. When the lower 8-bit are not all "1", by which the received data is "0" to determine which light is turned on/off.



BM32D2021-1 System Flow Chart

Initialise Operating Principle

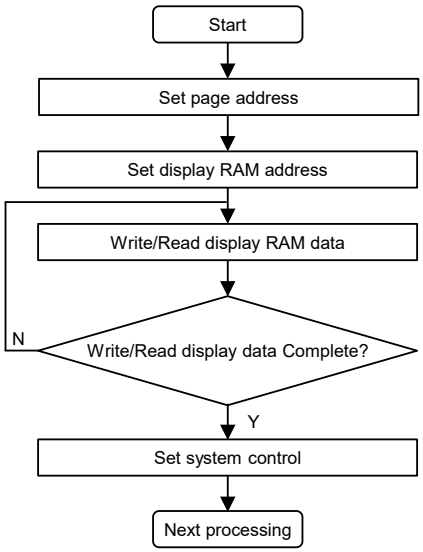
Set binary/gray mode, set lighting effect display, integrated lighting effect function and key scanning function. Set constant current ratio, to make the output current consistent. Set global brightness control, integrated PWM signal control lighting effect. Set cascade mode, use the I^2C interface for multi-module cascading. Set LED control on/off, use the integrated key scanning function to control the lighting effect.



Initialisation Flow Chart

Address Selection Operating Principle

Integrated lighting effect function and key scanning function, set the page address, then follows is the data 00h~0Fh to select the Page No., and then users can configure the display data value and function in that Page No. Set the display memory address, a logic “1” in the RAM bit-map indicates an “on” state of the corresponding LED ROW. Similarly a logic “0” indicates an “off” state.



Address Selection Flow Chart

Interface

The BM32D2021-1 provides the I²C communication mode. In this mode, the Master device sends address information to the BM32D2021-1. Refer to the I²C interface for details.

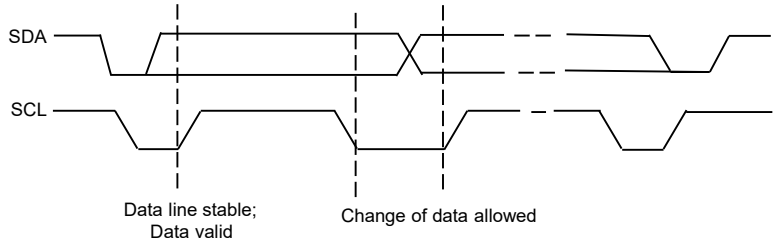
I²C Interface

I²C Operation

The module includes an I²C serial interface, which is a bidirectional two-line communication link between different ICs or modules. The two lines of the interface are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via a pull-up resistor, typical 4.7kΩ. When the bus is free both lines are high. The output stages of devices connected to the bus must have open-drain or open-collector types to implement the wired-and function necessary for connection. Data transfer is initiated only when the bus is not busy.

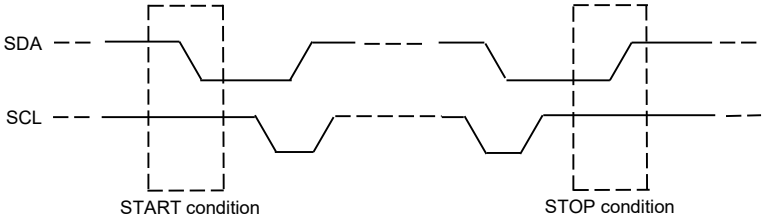
Data Validity

The data on the SDA line must be stable during the clock high period. The high or low state of the data line can only change when the clock signal on the SCL line is low as shown in the accompanying diagram.



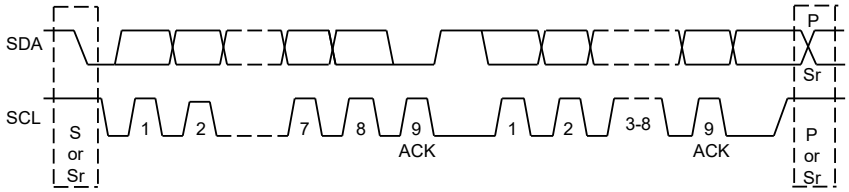
START and STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus remains busy if a repeated START (Sr) is generated instead of a STOP condition. The START(S) and repeated START (Sr) conditions are functionally identical.



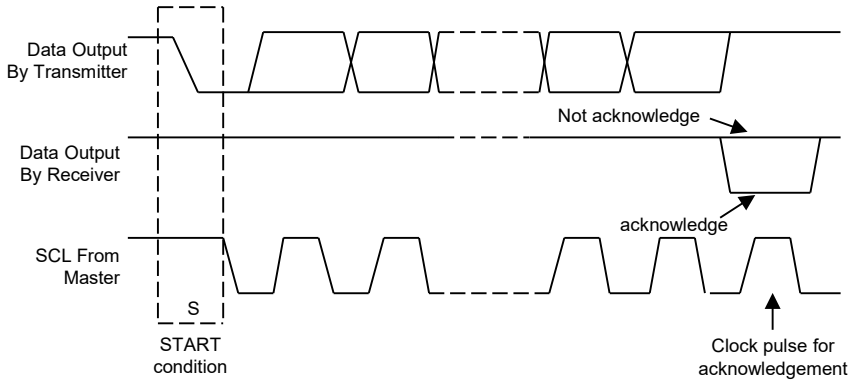
Byte Format

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.



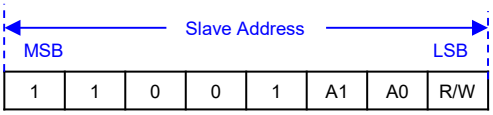
Acknowledge

- Each byte of eight bit length is followed by one acknowledge bit. This acknowledges bit is a low level placed on the bus by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an Acknowledge, ACK, after the reception of each byte.
- The device that provides an Acknowledge must pull down the SDA line during the acknowledge clock pulse so that it remains at a stable low level during the high period of this clock pulse.
- A master receiver must signal an end of data to the slave by generating a not-acknowledge, NACK, bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse so as to not acknowledge. The master will generate a STOP or a repeated START condition.



Slave Addressing

- The device requires an 8-bit slave address word following a start condition to enable the device for a write operation. The device address word consist of a mandatory one, zero sequence for the first four most significant bits. Refer to the diagram showing the slave Address. This is common to all LED devices.
- The slave address byte is the first byte received following the START condition from the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines whether a read or write operation is to be performed. When the R/W bit is "1", then a read operation is selected. A "0" selects a write operation.
- When a slave address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an Acknowledge on the SDA line.
- The address bits are "1, 1, 0, 0, 1, A1, A0".



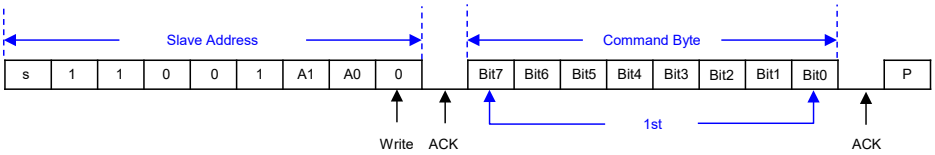
Note: 1. Common address that all devices are responding on the slave address bits are "0, 1, 0, 1, 1, 1, 0". The I²C address is: 0x2E.
2. When the AD pin is connected to VSS (GND), the [A1, A0] bits should be set to [0, 0]. The I²C address is: 0x64.
3. When the AD pin is connected to the SCL, the [A1, A0] bits should be set to [0, 1]. The I²C address is: 0x65.
4. When the AD pin is connected to the SDA, the [A1, A0] bits should be set to [1, 0]. The I²C address is: 0x66.
5. When the AD pin is connected to VDD, the [A1, A0] bits should be set to [1, 1]. The I²C address is: 0x67.

I²C Communication Protocol

Write Operation

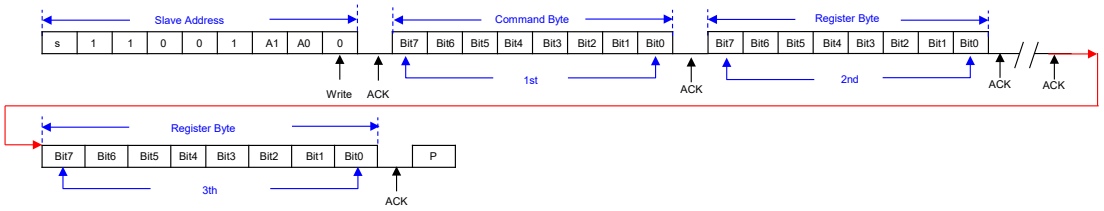
Single Command Byte

Byte write operation requires a START condition, slave address with R/W bit, a command (1st) and a STOP condition for single command byte.



Compound Command Byte

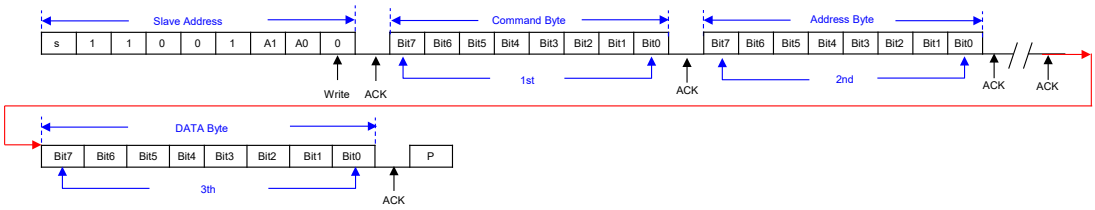
A byte write operation requires a START condition, a slave address with an R/W bit, a command (1st), one or more register byte command (2nd~nth) and a STOP condition for compound command byte.



Note: If the input memory location value is greater than limit value, the input memory location value will invalid.

Single Write RAM Data Byte Operation

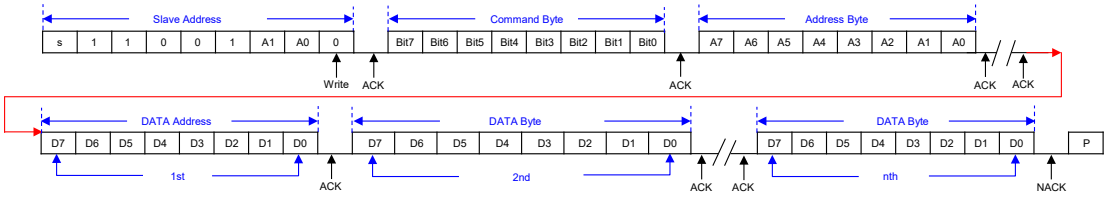
Following a START condition, the slave address with an R/W bit is placed on the bus. Then follows the display data address setting command code (1st) and the address point (An) is written to the address pointer (2nd) and then valid data and a STOP condition for a compound write single data byte.



Note: If the input memory location value is greater than limit value, the input memory location value will invalid.

Page Write RAM Data Operation

Following a START condition, the slave address with a R/W bit is placed on the bus along with the display data address setting command code (1st) and the address point (An) (2nd). The data to be written to the memory is next, after which the internal address pointer is incremented to the next address location on the reception of an acknowledge clock.



Note: If memory location exceeds limit value, the memory pointer will return to 00H. The Memory location limit values are shown as below:

Mode	Memory Location Limit Value		
	Display Data	Fade Data	LED On/Off Control
Binary	1FH	—	—
Gray	FFH	7FH	1FH

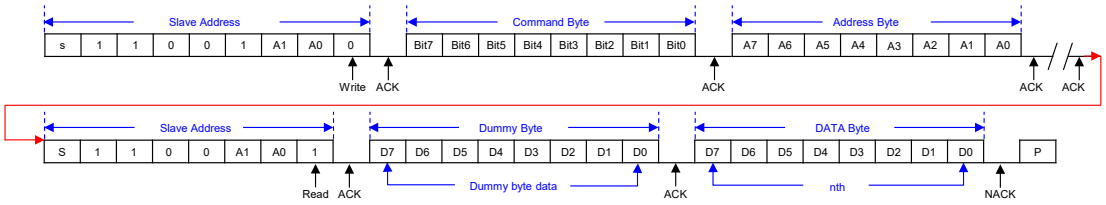
Memory Location Limit Value

Read Operation

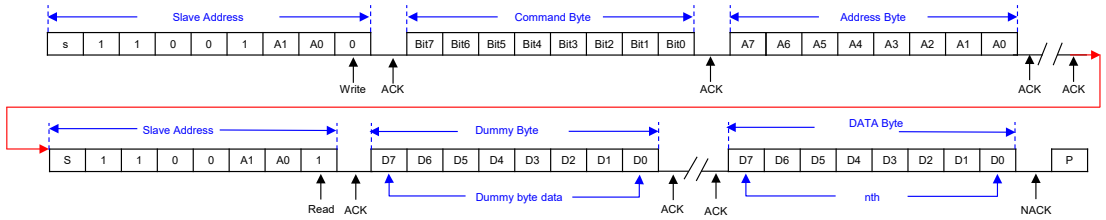
In this mode, the master reads the device data after setting the slave address. Following the R/W bit (=“0”), and the acknowledge bit, then follows the address setting command code (1st). After this is the address pointer (An) which is written to the address pointer (2nd). Next come the START condition and slave address, followed by an R/W bit (=“1”). The addressed data is then transmitted. The address pointer is only incremented on reception of an acknowledge clock. The device will

place the data at address An+1 onto the bus. The master reads and acknowledges the new byte and the address pointer is incremented to "An+2". If only a read command is sent to the I²C interface, then dummy data is transmitted. This cycle for reading consecutive addresses will continue until the master sends a NACK and STOP condition.

Single Read RAM Data Operation



Page Read RAM Data Operation



Note: 1. This cycle to read consecutive addresses will continue until the master sends a NACK and STOP condition.

2. If memory location exceeds limit value, the memory pointer will return to 00H. The Memory location limit values are shown as below.

Mode	Memory Location Limit Value		
	Display Data	Fade Data	LED On/Off Control
Binary	1FH	—	—
Gray	FFH	7FH	1FH

Memory Location Limit Value

Cascade Mode

This command will select master/slave mode and input clock source.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Cascade Mode	W	0	0	1	1	0	1	0	0	34H
	W	X	X	X	X	X	X	MS1	MS0	00H

MS1	MS0	SYNC Pin Status	Remarks
0	0	High impedance	Default value
0	1	Oscillator output mode	Master Mode
1	0	Oscillator input mode	Slave Mode
1	1	High impedance	

Communication Interface

Communication method: I²C

I²C address: 0x2E+ (0x64, 0x65, 0x66, 0x67 (select 1 of 4))

If the address is not set, only the broadcast address 0x2E can be used. The I²C address format is shown as follows.

I²C address format:

MSB LSB

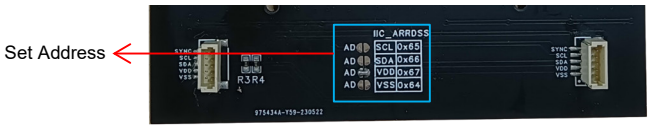
A6	A5	A4	A3	A2	A1	A0	R/W
0	1	0	1	1	1	0	

Slave address(0x2E)

Note: R/W=1: Read direction

=0: Write direction

The address setting can be executed by four addresses on the board. The broadcast address 0x2E is still supported in any state.



I²C address selection:

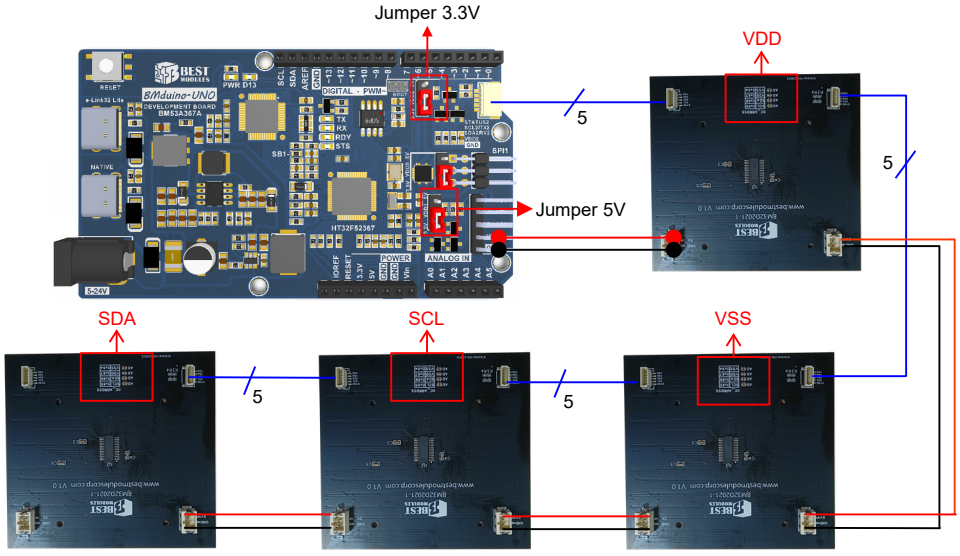
Jumper				I²C Address
1VDD-AD	2SDA-AD	3SCL-AD	4VSS-AD	
Short circuit	Open circuit	Open circuit	Open circuit	0x67
Open circuit	Short circuit	Open circuit	Open circuit	0x66
Open circuit	Open circuit	Short circuit	Open circuit	0x65
Open circuit	Open circuit	Open circuit	Short circuit	0x64

Note:1. The address must be set before using the application, and then power on.

2. The broadcast address of the module is 0x2E. When the address is set according to the above table, the broadcast address can also be used for communication.

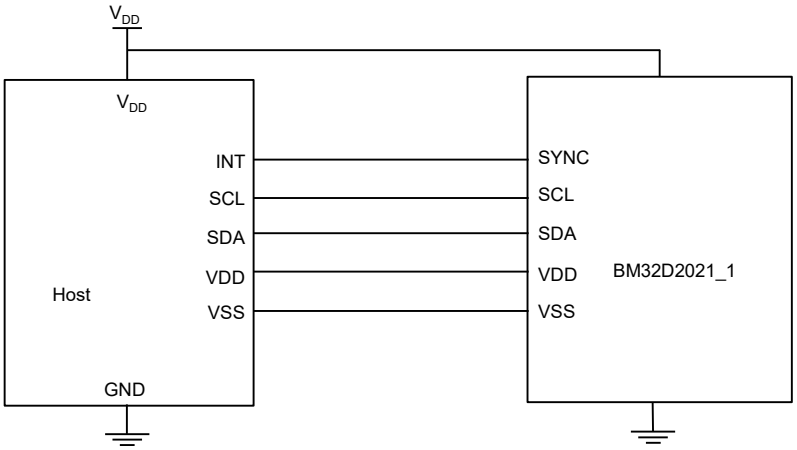
Multi-module Cascading

The modules can be cascaded to form a master and multiple slave communication. Since the jumper only can be set four I²C addresses, a maximum of four modules can be connected to the same I²C bus.

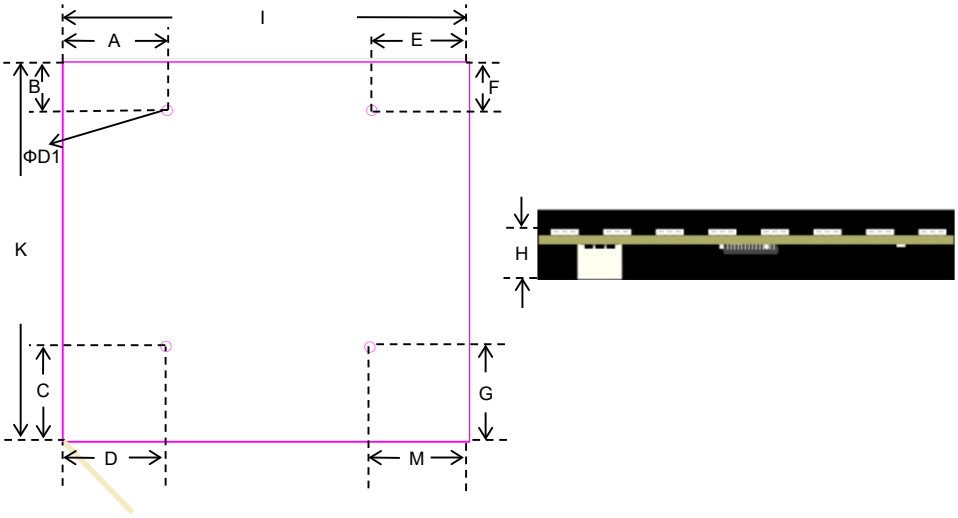


Cascading Diagram

Application Circuits



Dimensions



Dimension Information

Symbol \ Unit	mm	inch
A	20.574	0.81
B	9.271	0.365
C	18.415	0.725
D	19.939	0.785
E	18.796	0.74
F	9.398	0.37
G	19.177	0.755
M	18.796	0.74
K	73.66	2.9
I	78.994	3.11
D1	0.8	0.032
H	8.00	0.32

Dimension List

Reference Information

Revision History

Data	Author	Issue	Modification Information
2024.1.3	江嘉欣	V1.00	First Version

Online Purchase

https://www.bestmodulescorp.com