BC2102
Sub-1GHz RF Transmitter

Features

- Frequency bands: 315MHz, 433MHz, 868MHz, 915MHz
- Supports OOK/FSK modulation
- Supports 2-wire I^2C interface
- Operating voltage range of 2.2V~3.6V
- Programmable OOK symbol rate up to 25ksps
- Programmable FSK data rate up to 50kbps
- 0.4μA deep sleep mode current with data retention
- TX current consumption @ 433MHz:
  - 17mA @ 10dBm POUT (FSK)
  - 11mA @ 10dBm POUT (OOK, 50% duty cycle)
- On-chip VCO and Fractional-N synthesizer with integrated loop filter
- Supports low cost 16MHz crystal
- Supports hardware control mode – MCU is not required for radio control
- Integrated 64×1-bit FUSE Data Memory
- Package type: 8-pin SOP-EP

Abbreviation Notes

TX: RF Transmitter

SX: Synthesizer

XO: External Crystal

PA: Power Amplifier

OOK: On-Off Keying

FSK: Frequency Shift Keying

VCO: Voltage Control Oscillator

PLL: Phase Lock Loop

MMD: Multi-Mode Divider

XTAL: External Crystal

Development Tools

For rapid product development and to simplify device parameter setting, Holtek has provided relevant development tools which users can download from the following link:

https://www.holtek.com/rf-workshop

General Description

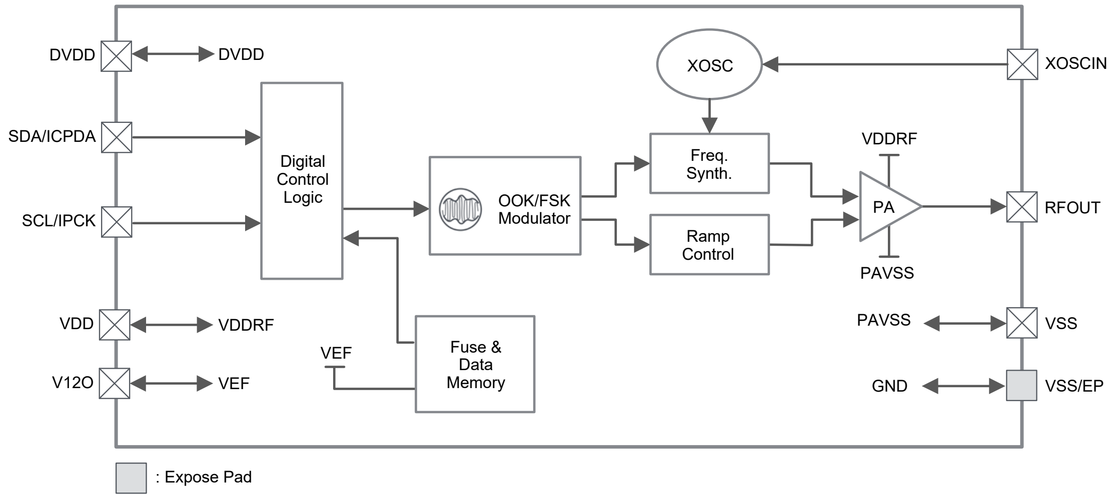
The BC2102 is a low cost sub-GHz OOK/FSK transmitter for wireless applications in the 315MHz, 433MHz, 470MHz, 868MHz and 915MHz frequency bands. It is a highly integrated and low cost solution for one-way transmitters. It only needs a crystal, a few external capacitors and a few PA output matching components on PCB to form a complete RF solution.

The BC2102 consists of a highly integrated fractional-N Synthesizer and a Class-E Power Amplifier (PA). As it adopts a fractional-N synthesizer, the users can potentially design their transmitters to operate at a wider frequency range. A class-E PA can deliver up to +13dBm output power. With proper setting through an external MCU, the BC2102 can support OOK and FSK modulation with symbol rate of up to 25ksps and data rate of up to 50kbps, respectively.

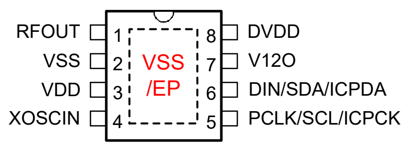
To minimize power consumption, the BC2102 provides a data tracking function. After no input data is detected during a preset time which can be adjusted through MCU, the BC2102 will return to the deep sleep mode.

These features can be easily programmed through I^2C interface or internal FUSE. With these combined features the BC2102 can provide a power-saving and cost effective solution for a wide range of wireless applications.

Block Diagram



Pin Assignment



BC2102
8 SOP-EP-A

Pin Description

Pin No.	Pin Name	Function	Type	Description
1	RFOUT	PA_OUT	AO	RF power amplifier output
2	VSS	PA_GND	PWR	Analog ground
3	VDD	VDD	PWR	Analog power supply
4	XOSCIN	Crystal	AI	External crystal input
5	PCLK/SCL/ ICPCK	PCLK	I	Clock input
		SCL	I	I^2C clock input
		ICPCK	I	ICP clock input pin
6	DIN/SDA/ ICPDA	DIN	I	RF transmitter data input
		SDA	I	I^2C data input
		ICPDA	I	ICP data input pin
7	V12O	LDO_OUT	PWR	LDO output, must be connected a 0.1μF capacitor
8	DVDD	VDD	PWR	Digital power supply
—	VSS/EP(*)	Ground	PWR	Exposed pad, must be connected to ground

Note: I: Digital Input   O: Digital Output   AI: Analog Input

AO: Analog Output   PWR: Power

*: 1. The VSS/EP pin located at the exposed pad.

2.The backside plate of EP shall be well soldered to ground on PCB, otherwise it will downgrade RF performance.

Absolute Maximum Ratings

Supply Voltage .... V_{SS}-0.3V to V_{SS}+3.6V

Voltage on I/O pins .... V_{SS}-0.3V to V_{DD}+0.3V

ESD HBM .... ±2kV

Storage Temperature .... -60°C to 150°C

Operating Temperature .... -40°C to 85°C

*This device is ESD sensitive. HBM (Human Body Mode) is based on the MIL-STD-883.

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those has listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C, V_{DD}=3.3V, f_{XTAL}=16MHz, OOK/FSK modulation with Matching circuit, PAOUT is powered by V_{DD}=3.3V, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{OP}	Operating Temperature	—	-40	—	85	°C
V_{DD}	Supply Voltage	—	2.2	3.3	3.6	V
T_{FP}	FUSE Programming Temperature	—	—	25	—	°C
Digital I/Os						
V_{IH}	High Level Input Voltage	—	0.7×V_{DD}	—	V_{DD}	V
V_{IL}	Low Level Input Voltage	—	0	—	0.3×V_{DD}	V
V_{OH}	High Level Output Voltage	I_{OH}=-5mA	0.8×V_{DD}	—	V_{DD}	V
V_{OL}	Low Level Output Voltage	I_{OL}=5mA	0	—	0.2×V_{DD}	V
Current Consumption						
I_{Sleep}	Deep Sleep Mode Current Consumption	—	—	—	0.4	μA
$I_{Standby}$	Idle Mode Current Consumption	XTAL on, PA off, Synthesizer on	—	6.5	—	mA
I_{TX}	High Data Current Consumption @ 315MHz (Data=1)	P_{RF}=0dBm	—	11	—	mA
		P_{RF}=10dBm	—	19	—	
		P_{RF}=13dBm	—	24	—	
	High Data Current Consumption @ 433MHz (Data=1)	P_{RF}=0dBm	—	11	—	mA
		P_{RF}=10dBm	—	17	—	
		P_{RF}=13dBm	—	24	—	
	High Data Current Consumption @ 868MHz (Data=1)	P_{RF}=0dBm	—	11	—	mA
		P_{RF}=10dBm	—	19	—	
		P_{RF}=13dBm	—	24	—	
	High Data Current Consumption @ 915MHz (Data=1)	P_{RF}=0dBm	—	12	—	mA
		P_{RF}=10dBm	—	20	—	
		P_{RF}=13dBm	—	25	—	
Pull-high Resistance						
R_{PH}	Pull-high Resistance for I/O Ports	3.3V	—	33	—	kΩ

A.C. Characteristics

RF Characteristics

Ta=25°C, V_{DD}=3.3V, f_{XTAL}=16MHz, OOK/FSK modulation with Matching circuit, PAOUT is powered by V_{DD}=3.3V, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Transmitter Characteristics						
f_{RF}	RF Frequency Band	315MHz band	—	315	—	MHz
		433MHz band	—	433.92	—	
		868MHz band	—	868.35	—	
		915MHz band	—	915	—	
SR	Symbol Rate	OOK modulation	0.5	—	25	ksps
DR	Data Rate	FSK modulation (@f_{DEV}=12.5kHz)	0.5	—	50	kbps
P_{RF}	RF Transmit Output Power	433MHz band	0	—	13	dBm
		868MHz band	0	—	13	
t_{ST}	RF Transmit Settling Time	Standby mode to Transmit mode	—	370	—	μs
ER_{OOK}	OOK Extinction Ratio	OOK modulation depth	—	70	—	dB
f_{DEV}	Frequency Deviation	FSK modulation @ f_{XTAL}=16MHz	2	—	100	kHz
	Output Blanking	From Deep Sleep to Transmit mode	—	—	1	Ms
	One Shot Delay Time	OOK/FSK	4	—	32	ms
$S.E._{TX}$	TX Spurious Emission (P_{RF}=10dBm)	f < 1GHz	—	—	-36	dBm
		47MHz < f < 74MHz	—	—	-54	
		87.5MHz < f < 118MHz				
		174MHz < f < 230MHz				
		470MHz < f < 862MHz				
		2^{nd}, 3^{rd} Harmonic	—	—	-30	
LO Characteristics						
f_{LO}	RF Frequency Coverage Range	315MHz band	290	—	335	MHz
		433MHz band	415	—	490	
		868MHz band	830	—	960	
f_{STEP}	LO Frequency Resolution	—	—	—	1	kHz
PN_{LO}	433MHz Phase Noise	@ 100kHz offset	—	-76	—	dBc/Hz
		@ 1MHz offset	—	-104	—	
	868MHz Phase Noise	@ 100kHz offset	—	-70	—	
		@ 1MHz offset	—	-100	—	
Crystal Oscillator						
f_{XTAL}	XTAL Frequency	—	—	16	—	MHz
ESR	XTAL Equivalent Series Resistance	—	—	—	100	Ω
C_{LOAD}	XTAL Capacitor Load	—	—	16	—	pF
TOL (Note)	XTAL Tolerance	—	-20	—	+20	ppm
t_{SU}	XTAL Startup Time	49US	—	—	1	ms
		3225SMD	—	3	1	ms

Note: This is the total tolerance including (1) Initial tolerance (2) Crystal loading (3) Aging and (4) Temperature dependence.

The acceptable crystal tolerance depends on RF frequency and channel spacing/band width.

I²C Characteristics

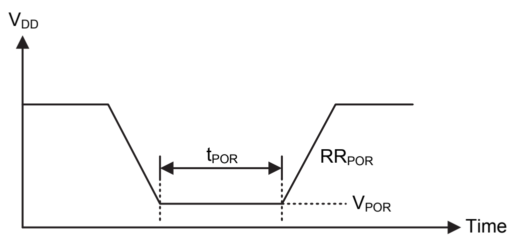
Ta=-40°C~85°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I²C Characteristics						
f_{SCL}	Serial Clock Frequency	—	—	—	1	MHz
t_{BUF}	Bus Free Time between Stop and Start Condition	SCL=1MHz	250	—	—	ns
t_{LOW}	SCL Low Time	SCL=1MHz	500	—	—	ns
t_{HIGH}	SCL High Time	SCL=1MHz	500	—	—	ns
$t_{su(DAT)}$	Data Setup Time	SCL=1MHz	100	—	—	ns
$t_{su(STA)}$	Start Condition Setup Time	SCL=1MHz	250	—	—	ns
$t_{su(STO)}$	Stop Condition Setup Time	SCL=1MHz	250	—	—	ns
$t_{h(DAT)}$	Data Hold Time	SCL=1MHz	100	—	—	ns
$t_{h(STA)}$	Start Condition Hold Time	SCL=1MHz	250	—	—	ns
$t_{r(SCL)}$	Rise Time of SCL Signal	SCL=1MHz	—	—	100	ns
$t_{f(SCL)}$	Fall Time of SCL Signal	SCL=1MHz	—	—	100	ns
$t_{r(SDA)}$	Rise Time of SDA Signal	SCL=1MHz	—	—	100	ns
$t_{f(SDA)}$	Fall Time of SDA Signal	SCL=1MHz	—	—	100	ns

Power on Reset Electrical Characteristics

Ta=-40°C~85°C, Ta=25°C Typical

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	—	—	—	—	100	mV
RR_{POR}	V_{DD} Rising Rate to Ensure Power-on Reset	—	—	0.035	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} Stays at V_{POR} to Ensure Power-on Reset	—	—	1	—	—	ms



Functional Description

The BC2102 is a low cost sub-GHz OOK/FSK transmitter for wireless applications in the 315MHz, 433MHz, 470MHz, 868MHz and 915MHz frequency bands. It consists of a highly integrated fractional-N Synthesizer and a Class-E Power Amplifier (PA).

The RF frequency is generated by a fully integrated fractional-N Synthesizer which includes RF VCO, loop filter and Digital controlled XO (DCXO). A fractional-N synthesizer allows users to extend their applications to a wider frequency range with the same XO.

The transmit session is a VCO direct modulation architecture. Different from the conventional direct-up conversion transmitter, the FSK modulation signal is fed into the VCO directly to take advantage of fractional-N synthesizer. As a result, both layout area and current consumption are much smaller. The modulated signal, generated by VCO, is fed into a Class-E PA and the maximum output power can be up to +13dBm.

For OOK modulation applications, the BC2102 provides an optimized PA ramping up and down feature to avoid the power spreading in the frequency domain.

Solution Overview

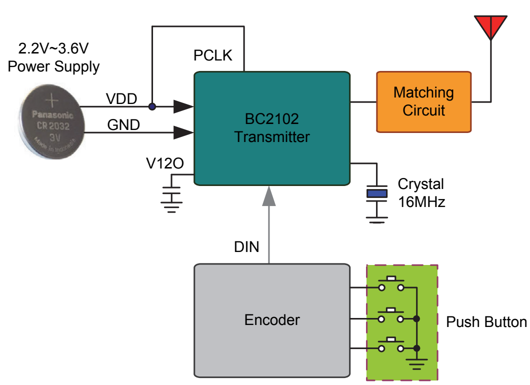
The BC2102 provides a 64×1-bit FUSE data memory, similar to One-time Programming (OTP) Non-volatile Memory.

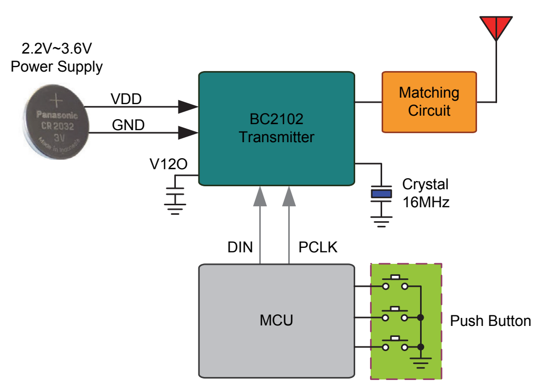
If the FUSE is un-programmed, which can be detected by checking the EFPGM bit in the CFG7 register, the user should connect the device to an MCU and setup the relevant RF registers configuration in the I^2C Mode using an I^2C interface. However, the registers will be reset to their initial state when the device is powered off.

For devices with programmed FUSE, users can implement a complete and versatile RF transmitter system to work together with an external MCU or Encoder. The corresponding application solutions are shown as below. Note that when EFPGM bit is low the device can only be connected to an external MCU.

If the device is connected with an Encoder, the FUSE data will be automatically copied to the corresponding registers. After a delay time, the encoder can send data to the device through the DIN pin and thus start a transmission sequence.

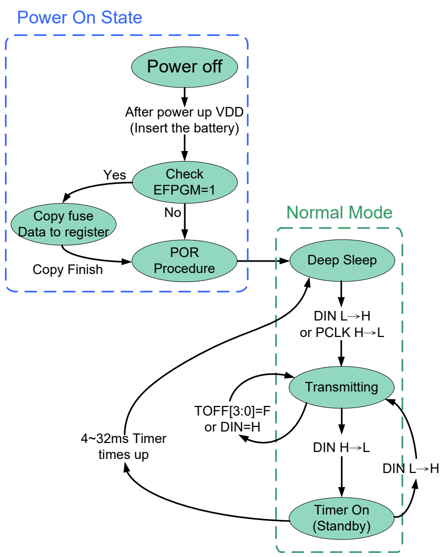
If the device is connected to an MCU, the same function aforementioned can also be implemented. The difference is that the MCU can configure the frequency, power and other parameters by setting the relevant registers using an I^2C interface when operating in the I^2C Mode.



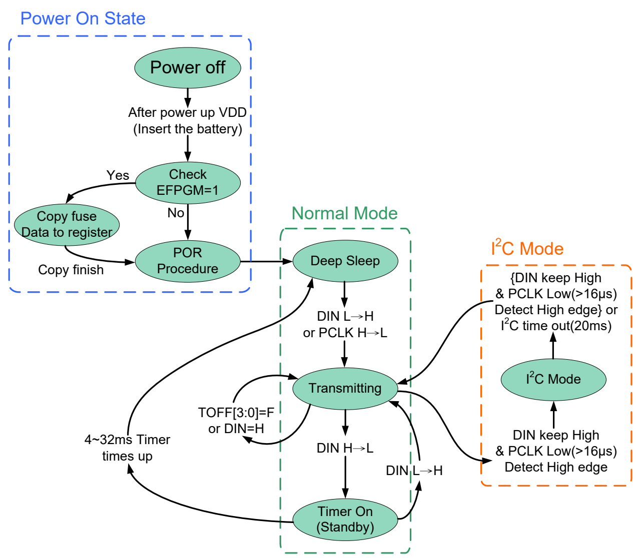


State Control

The BC2102 has integrated state machines that control the state transition between modes.



State Machine when Connected with Encoder



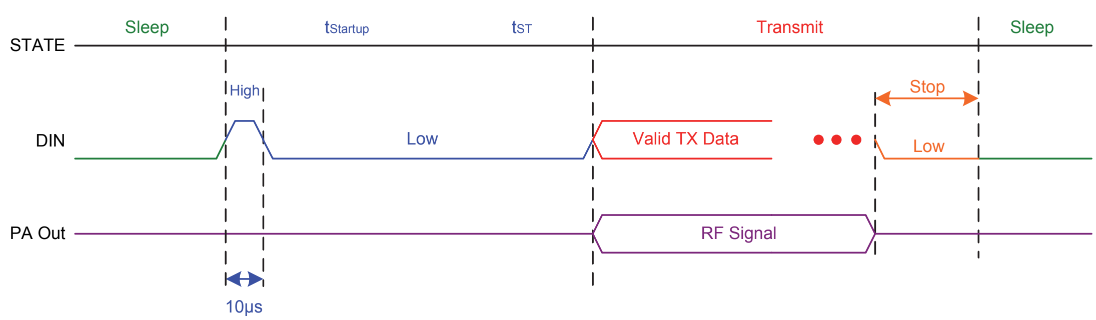
State Machine when Connected with MCU

Power On State

After power-on, if the EFPGM bit state is high, the FUSE data will be automatically copied to the corresponding registers. When completed the device will enter the Deep Sleep Mode after a delay time. Note that the device will directly enter the Deep Sleep Mode after a delay time if the EFPGM bit is low.

Normal Mode

After a power-on reset operation, the device enters the Deep Sleep Mode. Data will be transmitted if the DIN pin is pulled high or the pulse on the PCLK pin changes from high to low. When data transmission is finished and the DIN pin state changes from high to low, the device will enter the Standby state and the Timer, whose timeout period is determined by DLY_TOFF bits in the CFG1 register, will turn on and start to count. The device will return to the Deep Sleep Mode when the Timer overflows. However, it should be noted that when the DLY_TOFF[3:0] bit value is "1111", the device will start to transmit again without entering the Deep Sleep Mode once the DIN pin state changes from low to high.



TX Enabled by DIN Pin

I^{2}C Mode

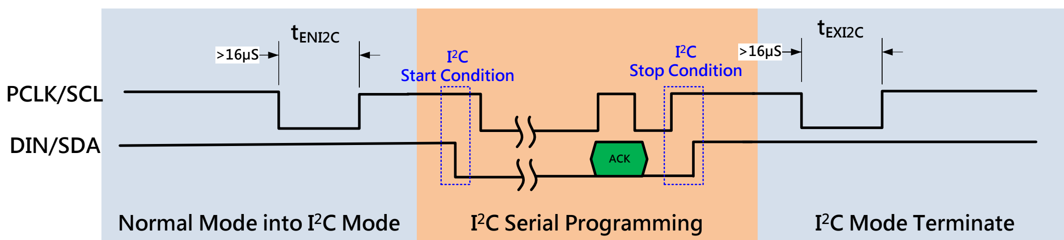
If the device is connected to an external MCU, then the I^{2}C mode can be used. When the SCL line (Pin 5) is pulled low for more than 16μs (t_{ENI2C}), the device will enter the I^{2}C Mode from the Normal Mode, during which the external control register can configure the special function registers in the device using I^{2}C commands. When the device receives a correct I^{2}C STOP signal followed by the SCL line being pulled low for more than 16μs, the device will return to the Normal Mode.

In the I^{2}C Mode, the MCU can configure the internal relevant registers using I^{2}C serial programming. The transmitter only supports the I^{2}C format for byte write, page write, byte read and page read format. The transmission procedure is shown as below.

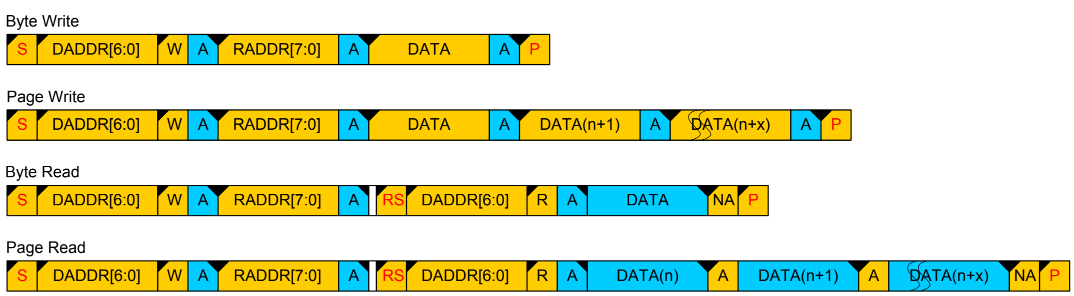
It should be noted that the I^{2}C is a non-standard I^{2}C interface, which only supports a single device for connection.

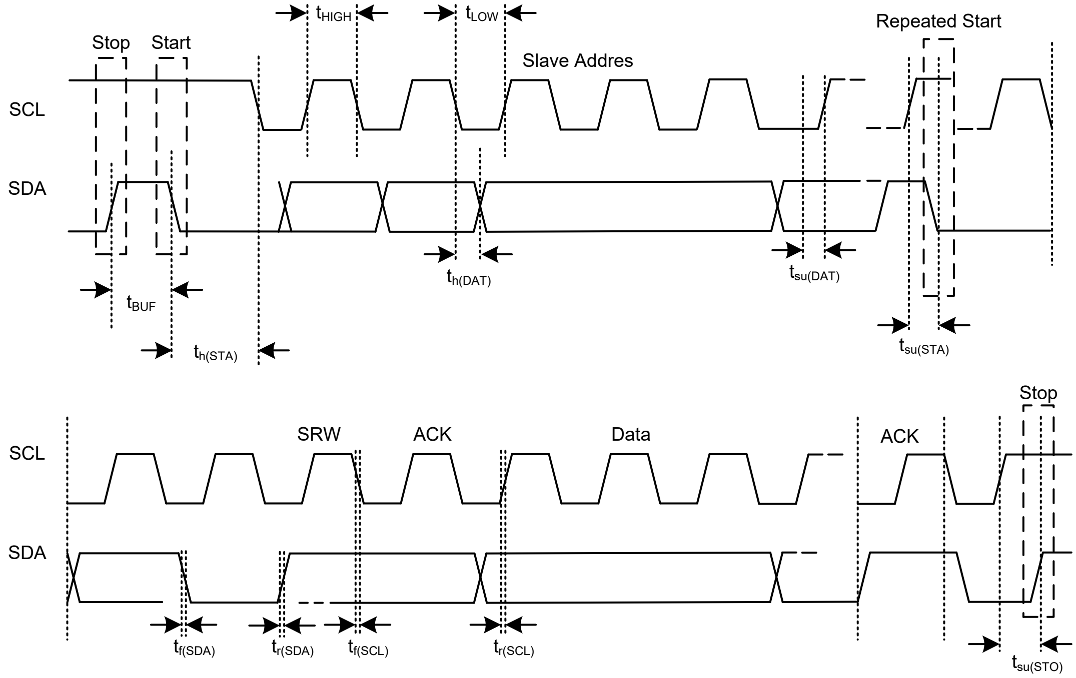
Symbol definition:

- S: Start symbol
- RS: Repeat Start
- P: Stop symbol
- DADDR[6:0]: device address, 21h
- R/W: read write select, R(0): write, (1): read
- RADDR[7:0]: register address
- ACK: A(0):ACK, NA(1):NAK
- Bus Direction:
  host to device:
  device to host:



I^{2}C Serial Programming





S = Start (1 bit)
SA = Slave Address (7 bits)
SR = SRW bit (1 bit)
M = Slave device send acknowledge bit (1 bit)
D = Data (8 bits)
A = ACK (RXAK bit for transmitter, TXAK for receiver, 1 bit)
P = Stop (1 bit)

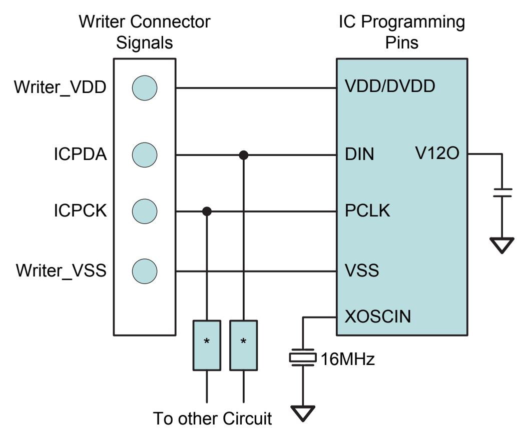
I^2C Communication Timing Diagram

Programming Methodology

The device programming interface should utilise an adaptor with an integrated 16MHz crystal.

Program Function	Pin Name	Pin Description
ICPCK	PCLK (Pin5)	ICP clock
ICPDA	DIN (Pin)	ICP Data/Address
VDD	VDD (Pin3) DVDD (Pin8)	Power supply
VSS, EP	VSS (Pin2), Exposed-Pad	Ground
XTAL IN (Adaptor)	XOSCIN (Pin4)	IC system clock

When programming, the device needs to be located on a Socket with a 16MHz crystal connected between Pin XOSCIN and ground. Holtek provides an e-link or e-WriterPro tool for communication with the PC. Between the e-link and the device there are four interconnecting lines, namely VDD, VSS, PCLK and DIN pins.



Note: * may be resistor or capacitor – the resistance of * must be greater than 1kΩ and the capacitance of * must be less than 1nF.

Register Map

When connected to an external MCU, the device can be setup and operated using a series of internal registers. Device commands and data are written to and read from the device using its internal I^2C bus. This list provides a summary of all internal registers. Their detailed operation is described under their relevant section in the functional description.

Address	Register Name	Bit 7	6	5	4	3	2	1	0
00h	CFG0	Setting0		XO_TRIM[5:0]					
01h	CFG1	DLY_TOFF[3:0]				Setting1			
02h	CFG2	FDEV[7:0]							
03h	CFG3	FSK_SEL	Setting2			TXPWR[3:0]			
04h	CFG4	D_N[5:0]						BAND_SEL[1:0]	
05h	CFG5	D_K[11:4]							
06h	CFG6	D_K[19:12]							
07h	CFG7	EFPGM	Setting3						

If the Fuse is un-programmed, the BC2102 device will have a default state described in the following, determined by register initial values.

Modulation Mode: OOK

Operating Frequency: 433.92MHz

TX Output Power: 10dBm

XTAL Capacitor Load: 16.651pF

Power Off Delay Time: 32ms

CFG0: Configuration Control Register 0

Address	Bit	7	6	5	4	3	2	1	0
00h	Name	Setting0		XO_TRIM[5:0]					
	R/W	R/W	R/W	R/W					
	Initial Value	1	0	1	0	0	0	0	0

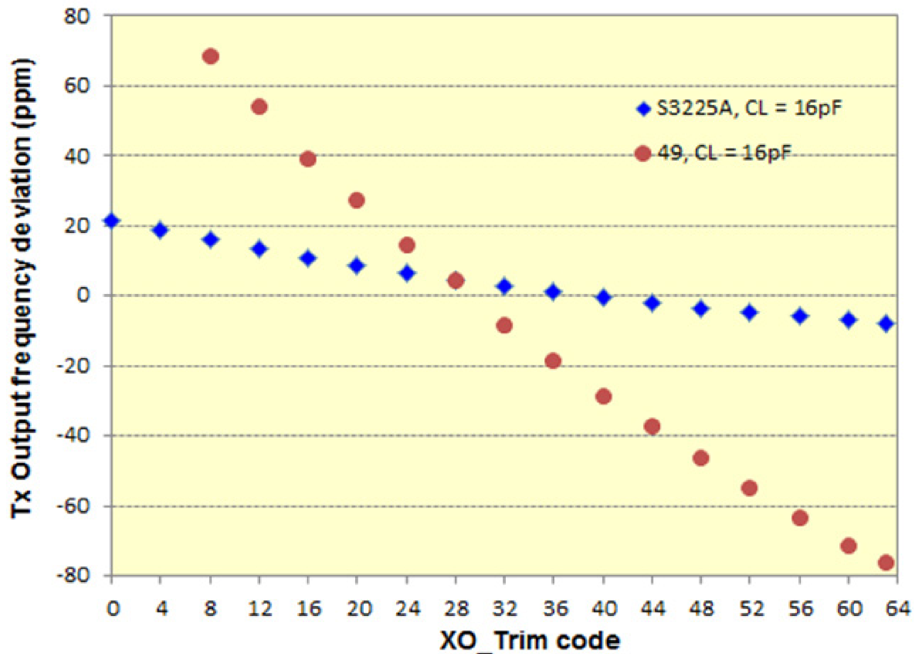
Bit 7~6 **Setting0**: Must be [0b10]

Bit 5~0 **XO_TRIM[5:0]**: Trim value of the internal capacitor array for different crystal C_{LOAD}

Based on XO fabricated by YOKETAN corporation.

49US 16MHz XO w/ 16pF Cload: The default setting is 1B. Within ±40ppm frequency error, 1 trim code shift -2.88ppm.

3225SMD 16MHz XO w/ 16pF Cload: The default setting is 28. Within ±20ppm frequency error, 1 trim code shift -0.37ppm.



CFG1: Configuration Control Register 1

Address	Bit	7	6	5	4	3	2	1	0
01h	Name	DLY_TOFF[3:0]				Setting1			
	R/W	R/W				R/W			
	Initial Value	1	1	1	0	0	0	0	1

Bit 7~4 **DLY_TOFF[3:0]**: Transmitter Auto Power Off Delay Time

t = 2ms × (DLY_TOFF[3:0]+2)

0000: 4ms
0001: 6ms
0010: 8ms
:
1110: 32ms
1111: Infinite – Never enter the Deep Sleep Mode

Bit 3~0 **Setting1**: Must be [0b0001]

CFG2: Configuration Control Register 2

Address	Bit	7	6	5	4	3	2	1	0
02h	Name	FDEV[7:0]							
	R/W	R/W							
	Initial Value	0	1	1	0	0	1	1	0

Bit 7~0 **FDEV[7:0]**: Frequency deviation for FSK

External Crystal = 16MHz, FDEV = (f_{DEV}×2^{15}/Fxtal); f_{XTAL} = 16MHz

Examples are as follows:

Default FDEV[7:0] = 01100110 → Decimal 102

External Crystal = 16MHz

f_{DEV} (Frequency deviation) = f_{DEV}×(16M/2^{15})

f_{DEV} (Frequency deviation) = 102×(16M/32768)=49.8kHz

CFG3: Configuration Control Register 3

Address	Bit	7	6	5	4	3	2	1	0
03h	Name	FSK_SEL	Setting2			TXPWR[3:0]			
	R/W	R/W	R/W			R/W			
	Initial Value	0	1	0	0	1	0	0	0

Bit 7 **FSK_SEL**: FSK Mode Enable

0: OOK

1: FSK

Bit 6~4 **Setting 2**: Must be [0b100]

Bit 3~0 **TXPWR[3:0]**: RF Output Power

The device has several output power values which are 0, 5, 10, and 13dBm.

TXPWR[3:0]	RF Output Power
0000	0dBm
0100	5dBm
1000	10dBm
1100	13dBm

TXPWR[3:0]	RF Output Power Fine Tune Level
XX00	0
XX01	1
XX10	2
XX11	3

Note that the adjust range: Level 3 > Level 2 > Level 1 > Level 0.

Note: Output power level could vary due to different matching components and placement on the PCB. The matching variation could significantly impact the output power level below +5dBm setting.

CFG4: Configuration Control Register 4

Address	Bit	7	6	5	4	3	2	1	0
04h	Name	D_N[5:0]						BAND_SEL[1:0]	
	R/W	R/W						R/W	
	Initial Value	0	1	0	1	1	0	0	1

Bit 7~2 **D_N[5:0]**: Integer of dividend for MMD

Bit 1~0 **BAND_SEL[1:0]**: Band Frequency Coarse Control

BAND_SEL	Frequency
00	315MHz
01	433MHz
10	868MHz
11	915MHz

Note that the BAND_SEL only select an approximate frequency range while the exact frequency value is determined by the D_N and D_K bit fields.

CFG5: Configuration Control Register 5

Address	Bit	7	6	5	4	3	2	1	0
05h	Name	D_K[11:4]							
	R/W	R/W							
	Initial Value	0	1	1	1	0	0	0	0

CFG6: Configuration Control Register 6

Address	Bit	7	6	5	4	3	2	1	0
06h	Name	D_K[19:12]							
	R/W	R/W							
	Initial Value	0	0	1	1	1	1	0	1

D_K[19:4]: 16-bit Fractional of dividend for MMD

D_N&D_K example.

X'TAL=16MHz and TX band =433MHz

1. D_N → (433M×Divider)/16M=54.125
   Take the integer part → D_N=54-32=22 → 010110
2. D_K → (433M×Divider)/16M=54.125
   Take the fractional part → D_K=0.125×2^{20}=131072 → 0010-0000-0000-0000
3. The example frequency can be referred in the following table.

Band_SEL	Frequency	Divider	X'TAL	D_N[5:0]	D_K[19:4]
315MHz	315MHz	2	16MHz	000111	0110-0000-0000-0000
433MHz	433MHz	2	16MHz	010110	0010-0000-0000-0000
433MHz	433.92MHz	2	16MHz	010110	0011-1101-0111-0000
868MHz	868MHz	1	16MHz	010110	0100-0000-0000-0000
915MHz	915MHz	1	16MHz	011001	0011-0000-0000-0000

CFG7: Configuration Control Register 7

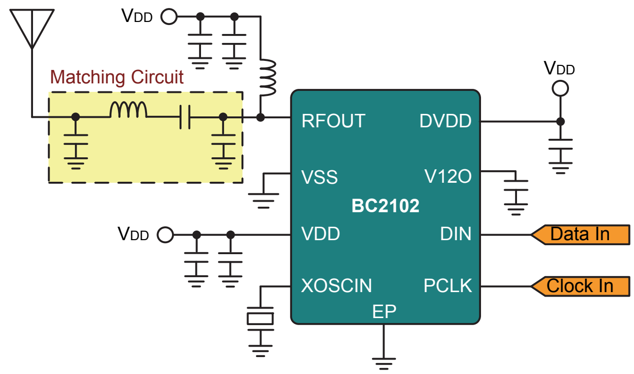
Address	Bit	7	6	5	4	3	2	1	0
07h	Name	EFPGM	Setting3						
	R/W	R	R/W						
	Initial Value	0	1	0	0	1	0	1	1

Bit 7 **EFPGM**: Fuse programmed, read only for I^2C
0: FUSE is not programmed – FUSE data is not mapped to the configuration register
1: FUSE is programmed – FUSE data is mapped to the configuration register

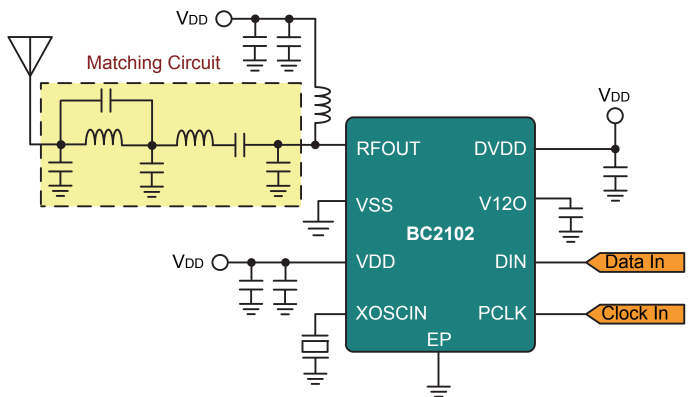
Bit 6~0 **Setting3**: Must be [0b1001011]

Application Circuits

433MHz Application Example



Evaluation Board Circuit



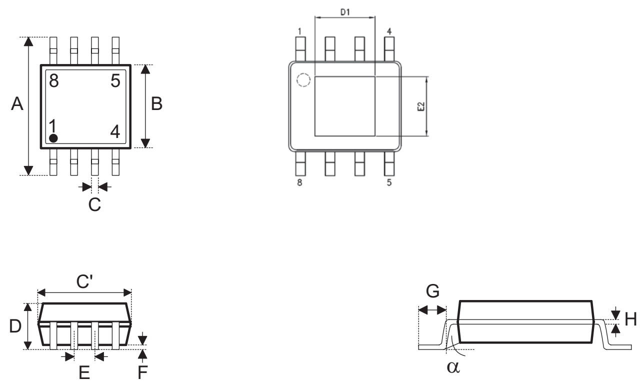
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/ Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

8-pin SOP-EP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.020
C'	—	0.193 BSC	—
D	—	—	0.069
D1	0.076	—	0.090
E	—	0.050 BSC	—
E2	0.076	—	0.090
F	0.000	—	0.006
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.00 BSC	—
B	—	3.90 BSC	—
C	0.31	—	0.51
C'	—	4.90 BSC	—
D	—	—	1.75
D1	1.94	—	2.29
E	—	1.27 BSC	—
E2	1.94	—	2.29
F	0.00	—	0.15
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°

Note: For this package type, refer to the package information provided here, which will not be updated by the Holtek website.