

Features

- Frequency band: 315/433/470/868/915MHz
- FSK/GFSK modulation
- Supports 3-wire or 4-wire SPI interface
- Wide input voltage range of 1.9V~3.6V
- Programmable data rate: 2Kbps~250Kbps
- Programmable TX output power: up to 13dBm
- Low current consumption
 - ♦ 0.4 μ A deep sleep mode current with data retention
 - ♦ RX current consumption (AGC on & low data rate) @ 433.92MHz: 4.2mA
 - ♦ RX current consumption (AGC on & low data rate) @ 868.3MHz: 5.5mA
 - ♦ TX current consumption @ 433.92MHz: 22mA @10dBm P_{OUT}
 - ♦ TX current consumption @ 868.3MHz: 24mA @10dBm P_{OUT}
- High RX sensitivity (433.92MHz)
 - ♦ -120dBm at 2Kbps on-air data rate
 - ♦ -110dBm at 50Kbps on-air data rate
 - ♦ -103dBm at 250Kbps on-air data rate
- High RX sensitivity (868.3MHz)
 - ♦ -119dBm at 2Kbps on-air data rate
 - ♦ -109dBm at 50Kbps on-air data rate
 - ♦ -103dBm at 250Kbps on-air data rate
- On-chip VCO and Fractional-N synthesizer with integrated loop filter
- Supports low cost 16MHz crystal with integrated load capacitor
- Programmable digital channel filter for optimum performance at various data rates
- AGC (Auto Gain Control) to achieve wide input range, up to +10dBm
- AFC (Auto Frequency Compensation) for frequency drift due to X^{tal} aging
- On-chip low power RC oscillator for WOR (Wake-on-RX) and WOT (Wake-on-TX) functions
- Physical TX/RX FIFO buffers: TX 64 bytes, RX 64 bytes
- Simple FIFO/Block FIFO/Extend FIFO (up to 255 bytes)/Infinite FIFO modes
- Programmable threshold for carrier detection
- Frame synchronization recognition for both FIFO mode and Direct mode
- Packet handling
 - ♦ FEC (Forward Error Correction)
 - ♦ Data whitening
 - ♦ Manchester encoding
 - ♦ CRC-16 checking
- ATR (Auto-Transmit-Receive)
 - ♦ Auto-resend
 - ♦ Auto-acknowledgment
 - ♦ WOT + Auto-resend
 - ♦ WOR + Auto-acknowledgment
- Packet filtering
 - ♦ CRC filtering
 - ♦ Address filtering
- Package type: 24-pin QFN (3mm×3mm)

General Description

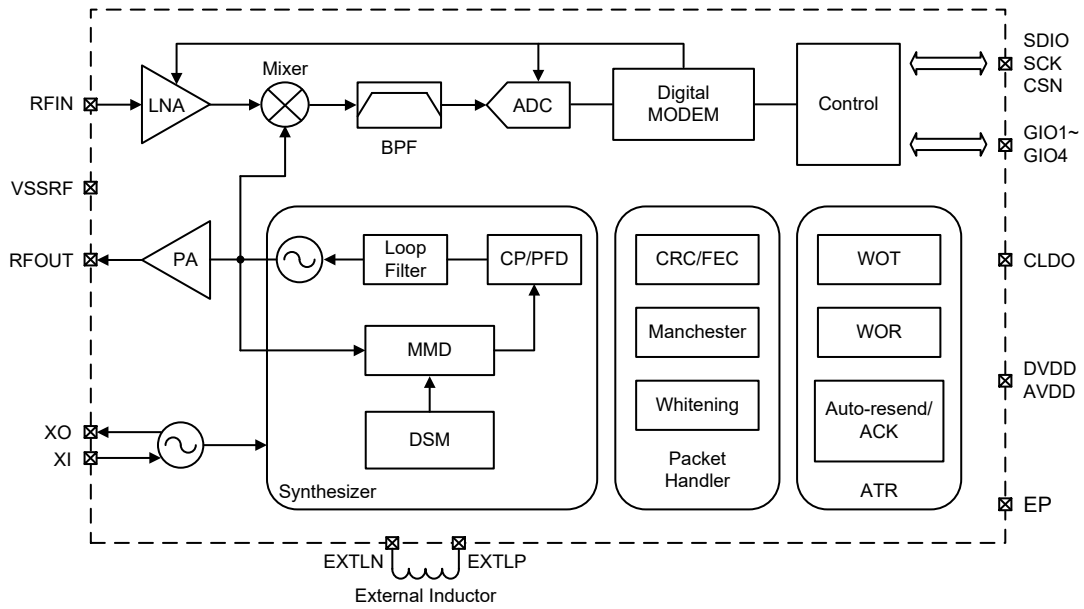
The BC3602 is a high performance and low cost FSK/GFSK transceiver for wireless applications in the 315MHz, 433MHz, 470MHz, 868MHz and 915MHz frequency bands. It incorporates a highly integrated sub-1GHz transceiver and a baseband modem with programmable data rates from 2Kbps to 250Kbps. Data handling features include 64-byte TX/RX FIFO and packet handling such as CRC generation, Forward Error Correction, Data whitening and Manchester encoding.

The BC3602 is optimized for the low power consumption applications. At 433MHz band, its RX mode is operated at 4.2mA and it delivers +10dBm TX output power at 22mA current consumption. A low-noise low-IF receiver can achieve -119dBm sensitivity of 2Kbps data rate at 433/868MHz bands. A Class-E Power Amplifier can deliver up to +13dBm output power at 433/868MHz bands. A fully integrated Fractional-N synthesizer can support a wide frequency range with a fine resolution. Both loop filter and XO load capacitors are integrated to on-chip to minimize the requirement for external components.

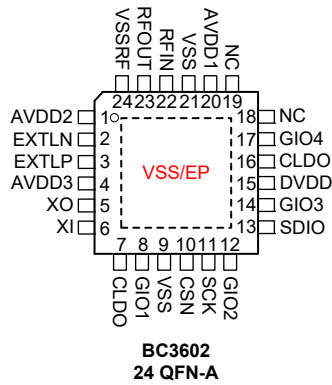
External host MCU can access the BC3602 through a 3-wire or 4-wire SPI interface. The device supports short strobe commands to reduce the loading of the host MCU while maintaining wireless communication link.

Additional link layer features like RSSI for channel assessment, auto-acknowledgement and auto-resend, WOT and WOR, etc., facilitate microcontroller based ISM bands wireless link applications.

Block Diagram



Pin Assignment



Pin Description

Pin No.	Pin Name	Type	Description
1	AVDD2	PWR	Analog power supply
2	EXTLN	AI	Connected to an external inductor
3	EXTLP	AI	Connected to an external inductor
4	AVDD3	PWR	Analog power supply
5	XO	AO	Crystal oscillator output
6	XI	AI	Crystal oscillator input
7	CLDO	PWR	LDO output, connected to a bypass capacitor
8	GIO1	DI/O	Multi-function I/O 1
9	VSS	PWR	Ground
10	CSN	DI	SPI chip select input, low active
11	SCK	DI	SPI clock input
12	GIO2	DI/O	Multi-function I/O 2
13	SDIO	DI/O	SPI data input/output
14	GIO3	DI/O	Multi-function I/O 3
15	DVDD	PWR	Digital power supply
16	CLDO	PWR	LDO output, connected to a bypass capacitor
17	GIO4	DI/O	Multi-function I/O 4
18	NC	—	Not connected
19	NC	—	Not connected
20	AVDD1	PWR	Analog power supply
21	VSS	PWR	Ground
22	RFIN	AI	RF LNA input
23	RFOUT	AO	RF power amplifier output
24	VSSRF	PWR	RF ground
EP	GND	PWR	Exposed pad, must be connected to ground

Legend: DI: Digital Input; DI/O: Digital Input/Output; AI: Analog Input; AO: Analog Output; PWR: Power/Ground
 The backside plate of EP shall be well soldered to ground on PCB, otherwise it will downgrade RF performance.

Absolute Maximum Ratings

Supply Voltage	$V_{SS}-0.3V$ to $V_{SS}+3.6V$	Operating Temperature	$-40^{\circ}C$ to $85^{\circ}C$
Voltage on I/O Ports	$V_{SS}-0.3V$ to $V_{DD}+0.3V$	ESD HBM	$\pm 2kV$
Storage Temperature	$-60^{\circ}C$ to $150^{\circ}C$		

The device is ESD sensitive. HBM (Human Body Mode) is based on MIL-STD-883.

Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

T_a=25°C, V_{DD}=3.3V, f_{X_{TAL}}=16MHz, FSK modulation with matching circuit and low/high pass filter, RF output is powered by V_{DD} (3.3V), unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T _{OP}	Operating Temperature	—	-40	—	85	°C
V _{DD}	Supply Voltage	—	1.9	3.3	3.6	V
Digital I/Os						
V _{IH}	High Level Input Voltage	—	0.7×V _{DD}	—	V _{DD}	V
V _{IL}	Low Level Input Voltage	—	0	—	0.3×V _{DD}	V
V _{OH}	High Level Output Voltage	I _{OH} =-5mA	0.8×V _{DD}	—	V _{DD}	V
V _{OL}	Low Level Output Voltage	I _{OL} =5mA	0	—	0.2×V _{DD}	V
Current Consumption						
I _{Sleep}	Deep Sleep Mode Current Consumption	—	—	0.4	1.0	µA
I _{IL}	Idle Mode Current Consumption	LIRC on, X'tal off	—	1.8	—	µA
	Light Sleep Mode Current Consumption	X'tal on	—	0.55	—	mA
I _{Standby}	Standby Mode Current Consumption @ 315/433MHz	X'tal on, Synthesizer on	—	2.2	—	mA
	Standby Mode Current Consumption @ 868/915MHz		—	3.0	—	
I _{RX} or I _{TX}	315MHz Band Current Consumption	RX mode @ 50Kbps	—	4.1	—	mA
		RX mode @ 250Kbps	—	4.4	—	
		TX mode @ 0dBm P _{OUT}	—	14	—	
		TX mode @ 10dBm P _{OUT}	—	24	—	
		TX mode @ 13dBm P _{OUT}	—	30	—	
	433MHz Band Current Consumption	RX mode @ 50Kbps	—	4.2	—	mA
		RX mode @ 250Kbps	—	4.6	—	
		TX mode @ 0dBm P _{OUT}	—	14	—	
		TX mode @ 10dBm P _{OUT}	—	22	—	
		TX mode @ 13dBm P _{OUT}	—	30	—	
	868MHz Band Current Consumption	RX mode @ 50Kbps	—	5.5	—	mA
		RX mode @ 250Kbps	—	6.1	—	
		TX mode @ 0dBm P _{OUT}	—	15	—	
		TX mode @ 10dBm P _{OUT}	—	24	—	
		TX mode @ 13dBm P _{OUT}	—	32	—	
	915MHz Band Current Consumption	RX mode @ 50Kbps	—	6	—	mA
		RX mode @ 250Kbps	—	6.5	—	
		TX mode @ 0dBm P _{OUT}	—	18	—	
		TX mode @ 10dBm P _{OUT}	—	24	—	
		TX mode @ 13dBm P _{OUT}	—	32	—	
R _{PH}	Pull-high Resistance for I/O Ports	3.3V	—	33	—	kΩ

A.C. Characteristics

Ta=25°C, V_{DD}=3.3V, f_{X_{TAL}}=16MHz, FSK modulation with matching circuit and low/high pass filter, RF output is powered by V_{DD} (3.3V), unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
RF Characteristics						
f _{RF}	RF Frequency Band	315MHz band	—	315	—	MHz
		433MHz band	—	433.92	—	
		470~510MHz band	—	490	—	
		868MHz band	—	868.3	—	
		915MHz band	—	915	—	
DR	Data Rate	GFSK modulation	2	—	250	Kbps
Transmitter						
P _{OUT}	TX Output Power	433MHz band	0	—	13	dBm
		868MHz band	0	—	13	
S.E. _{TX}	TX Spurious Emission (P _{OUT} =10dBm)	f < 1GHz	—	—	-36	dBm
		47MHz<f<74MHz	—	—	-54	
		87.5MHz<f<118MHz				
		174MHz<f<230MHz				
		470MHz<f<862MHz	—	—	-30	
2 nd , 3 rd Harmonic						
Receiver						
t _{ST,RX}	RX Settling Time	Light Sleep mode to RX mode	—	150	—	μs
P _{Sens}	315MHz RX Sensitivity @ BER=0.1%	2Kbps (f _{DEV} =8kHz)	—	-120	—	dBm
		10Kbps (f _{DEV} =40kHz)	—	-114	—	
		50Kbps (f _{DEV} =18.75kHz)	—	-110	—	
		125Kbps (f _{DEV} =46.875kHz)	—	-106	—	
		250Kbps (f _{DEV} =93.75kHz)	—	-103	—	
	433MHz RX Sensitivity @ BER=0.1%	2Kbps (f _{DEV} =8kHz)	—	-120	—	dBm
		10Kbps (f _{DEV} =40kHz)	—	-113	—	
		50Kbps (f _{DEV} =18.75kHz)	—	-110	—	
		125Kbps (f _{DEV} =46.875kHz)	—	-106	—	
		250Kbps (f _{DEV} =93.75kHz)	—	-103	—	
	868MHz RX Sensitivity @ BER=0.1%	2Kbps (f _{DEV} =8kHz)	—	-119	—	dBm
		10Kbps (f _{DEV} =40kHz)	—	-113	—	
		50Kbps (f _{DEV} =18.75kHz)	—	-109	—	
		125Kbps (f _{DEV} =46.875kHz)	—	-106	—	
		250Kbps (f _{DEV} =93.75kHz)	—	-103	—	
	915MHz RX Sensitivity @ BER=0.1%	2Kbps (f _{DEV} =8kHz)	—	-119	—	dBm
		10Kbps (f _{DEV} =40kHz)	—	-113	—	
		50Kbps (f _{DEV} =18.75kHz)	—	-109	—	
		125Kbps (f _{DEV} =46.875kHz)	—	-106	—	
		250Kbps (f _{DEV} =93.75kHz)	—	-103	—	
P _{IN,max}	Maxmum Input Power	@ BER<0.1%	—	—	10	dBm
IR	Image Rejection	—	—	25	—	dB
S.E. _{RX}	RX Spurious	25MHz~1GHz	—	—	-57	dBm
		Above 1GHz	—	—	-47	
	RSSI Range	AGC on	-110	—	-10	dBm

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
LO Characteristics						
f _{LO}	RF Frequency Coverage Range	315MHz band	290	—	335	MHz
		433MHz band	415	—	490	
		470~510MHz band	470	—	510	
		868MHz band	830	—	1000	
		915MHz band	870	—	1050	
f _{STEP}	LO Frequency Resolution	—	—	—	1	kHz
PN _{LO}	315MHz Phase Noise	@ 100kHz offset	—	-86	—	dBc/Hz
		@ 1MHz offset	—	-107	—	
	433MHz Phase Noise	@ 100kHz offset	—	-85	—	
		@ 1MHz offset	—	-106	—	
	868MHz Phase Noise	@ 100kHz offset	—	-82	—	
		@ 1MHz offset	—	-103	—	
	915MHz Phase Noise	@ 100kHz offset	—	-82	—	
		@ 1MHz offset	—	-103	—	
Crystal Oscillator						
f _{XTAL}	X'tal Frequency	—	—	16	—	MHz
ESR	X'tal Equivalent Series Resistance	—	—	—	100	Ω
C _{LOAD}	X'tal Capacitor Load	—	12	16	20	pF
TOL	X'tal Tolerance ^(Note)	—	-20	—	+20	ppm
t _{SU}	X'tal Startup Time	49US XO	—	—	1	ms

Note: When the data rate is 2Kbps at 315/433.92MHz, an X'tal with a tolerance of ±10ppm should be used.

When the data rate is 2Kbps at 868/915MHz, an X'tal with a tolerance of ±5ppm should be used.

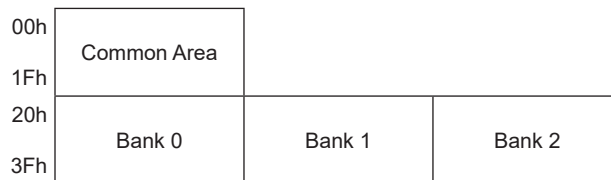
SPI Characteristics

T_a=-40°C~85°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f _{SCK}	SCK frequency	—	—	4	—	MHz
t _{SCKH}	SCK high time	—	1/f _{XCLK}	—	—	s
t _{SCKL}	SCK low time	—	1/f _{XCLK}	—	—	s
t _{S_SDIO}	SDIO input setup time	—	20	—	—	ns
t _{H_SDIO}	SDIO input hold time	—	20	—	—	ns
t _{S_CSN}	CSN to SCK active	—	30	—	—	ns
t _{H_CSN}	SCK inactive to CSN inactive	—	30	—	—	ns

Note: f_{XCLK}=f_{XTAL}/(XODIV2+1)

Memory Mapping

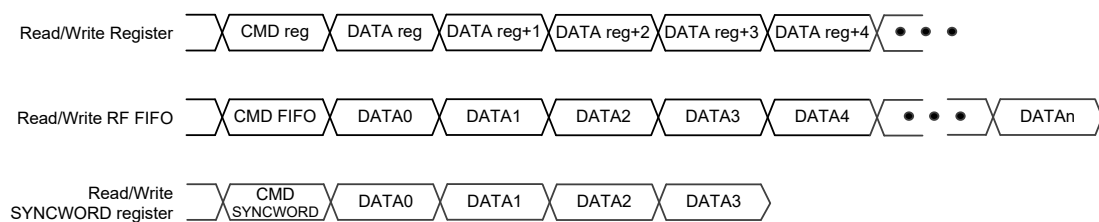


Common Area: It contains 32 bytes space. Accessing addresses 00h~1Fh always means to access the Common Area regardless of Bank Pointer configuration.

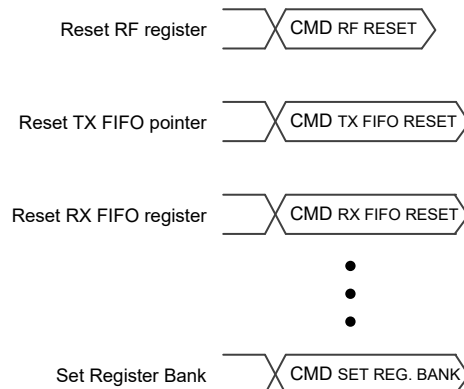
Bank 0~2: Each bank contains 32 bytes space. They are selected by the Bank Pointer.

The Bank Pointer, BANK[1:0], which is defined in the Common Area, can be set directly by the Set Register Bank command and read/written by the Control Register command.

Control Register Access



Strobe Command Followed by n-byte Data (CmdD)



Strobe Command Only (CmdO)

SFR Mapping and Bit Definition

Common Area Control Register

All control registers will be set to their initial value by power-on reset (POR). The software reset will set the control registers to their initial value except the FSYCK_EN, FSYCK_DIV[1:0], PWRON, GIO1S[2:0], GIO2S[2:0], PADDS[1:0], GIO3S[3:0], GIO4S[3:0], GIOPU[4:1], SPIPU, SDO_TEN bits in the RC1, IO1, IO2 and IO3 registers. These bits keep unchanged after software reset.

Addr.	Name	Bit							
		7	6	5	4	3	2	1	0
00h	CFG1	—	AGC_EN	RXCON_EN	DIR_EN	—	—	BANK[1:0]	
01h	RC1	PWRON	FSYCK_RDY	XCLK_RDY	XCLK_EN	FSYCK_DIV[1:0]		FSYCK_EN	RST_LL
02h	IRQ1	RXTO	RXFFOW	—	—	RXDETS[1:0]		IRQCPOR	IRQPOR
03h	IRQ2	ARKTFIE	ATRCTIE	FIFOLTIE	RXERRIE	RXDETIE	CALCMPIE	RXCMPIE	TXCMPIE
04h	IRQ3	ARKTFIF	ATRCTIF	FIFOLTIF	RXERRIF	RXDETIF	CALCMPIF	RXCMPIF	TXCMPIF
06h	IO1	PADDS[1:0]		GIO2S[2:0]		GIO1S[2:0]			
07h	IO2	GIO4S[3:0]			GIO3S[3:0]				
08h	IO3	SDO_TEN	SPIPU	—	GIOPU[4:1]				—
09h	FIFO1	—	—	TXFFSA[5:0]					
0Ah	FIFO2	—	—	—	RXPL2F_EN	FFINF_EN	FFMG_EN	FFMG[1:0]	
0Bh	PKT1	TXPMLN[7:0]							
0Ch	PKT2	PID[1:0]		TRAILER_EN	WHTFMT	SYNCLN[1:0]		RXPMLN[1:0]	
0Dh	PKT3	MCH_EN	FEC_EN	CRC_EN	CRCFMT	PLLEN_EN	PLHAC_EN	PLHLEN	PLH_EN
0Eh	PKT4	WHT_EN	WHTSD[6:0]						
0Fh	PKT5	TXDLEN[7:0]							
10h	PKT6	RXDLEN[7:0]							
11h	PKT7	RXPID[1:0]		DLY_RXS[2:0]			DLY_TXS[2:0]		
12h	PKT8	—	PLHA[5:0]						
13h	PKT9	PLHEA[7:0]							
14h	MOD1	DTR[7:0]							
15h	MOD2	RXIFOS[11:8]				DITHER[1:0]		—	DTR[8]
16h	MOD3	RXIFOS[7:0]							
17h	DM1	—	—	MDIV[5:0]					
18h	DM2	PREAMBLE_CFO_EN1	PREAMBLE_CFO_EN0	SDR[5:0]					
19h	DM3	CSF_SW_EN	FD_MOD[6:0]						
1Ah	DM4	THOLD[3:0]				CFO_DSEL	—	PH_DIFF_MOD	PRE_CSF_EN
1Bh	DM5	FD_HOLD[7:0]							
1Eh	DM8	M_RATIO[7:0]							

Note: Addresses 05h, 1Ch, 1Dh and 1Fh, which are not listed in this table are reserved for future use, it is suggested not to change their initial values by any methods.

The reset value shown in the following register description tables means the software reset results of strobe command.

• **CFG1: Configuration Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	—	AGC_EN	RXCON_EN	DIR_EN	—	—	BANK[1:0]	
R/W	—	R/W	R/W	R/W	—	—	R/W	
Reset	0	0	0	0	0	0	0	0

Bit 7 Reserved, must be “0”

Bit 6 **AGC_EN**: AGC enable
 0: Disable
 1: Enable

Bit 5 **RXCON_EN**: RX continue mode enable
 0: Disable
 1: Enable

Note that this bit only affects normal RX mode and ATR RX mode without ARK function.

Bit 4 **DIR_EN**: Direct mode enable
 0: TX/RX data from packet handling hardware
 1: TX/RX data from/to external MCU directly

Bit 3~2 Reserved, must be “00”

Bit 1~0 **BANK[1:0]**: Control register bank selection
 00: Bank 0
 01: Bank 1
 10: Bank 2
 11: Reserved

This selection can be set by both the Set Register Bank command and Control Register command.

• RC1: Reset/Clock Control Register 1

Bit	7	6	5	4	3	2	1	0
Name	PWRON	FSYCK_RDY	XCLK_RDY	XCLK_EN	FSYCK_DIV[1:0]		FSYCK_EN	RST_LL
R/W	R/W	R	R	R/W	R/W		R/W	R/W
POR	1	—	—	—	0	0	0	—
Reset	—	0	0	1	—	—	—	0

Bit 7 PWRON: 3.3V power on flag

This bit is only set to 1 by power on reset and not affected by software reset of strobe command. After being set high, this bit should be cleared by application program. The firmware can check this flag status and determine whether to execute auto calibration in the Light Sleep mode.

Bit 6 FSYCK_RDY: FSYCK clock ready flag (ready only)

0: Not ready

1: Ready

This bit is used to indicate that whether the FSYCK clock is ready for operation. This bit will be automatically cleared when FSYCK_EN=0, when power on reset occurs or when a Deep Sleep command or an Idle command is received.

Bit 5 XCLK_RDY: XCLK clock ready flag (ready only)

0: Not ready

1: Ready

This bit is used to indicate whether the XCLK debounce counter is full and XCLK is ready for operation. Note that when exiting the Deep Sleep state, this flag may need a certain period before being set high. This bit will be automatically cleared to zero when XCLK_EN=0, when RST_LL=1, when power on reset occurs or when a software reset command, a Deep Sleep command or an Idle command is received.

Bit 4 XCLK_EN: XCLK clock enable

0: Disable

1: Enable

Setting this bit high will enable the XCLK path to the baseband block while clearing this bit to zero can save power if required. The XCLK clock should be enabled when writing data to the FIFO.

Bit 3~2 FSYCK_DIV[1:0]: FSYCK clock (XCLK division) selection

00: 1/1 XCLK

01: 1/2 XCLK

10: 1/4 XCLK

11: 1/8 XCLK

Bit 1 FSYCK_EN: FSYCK clock enable

0: Disable

1: Enable

Bit 0 RST_LL: Low voltage (1.2V) logic reset control

0: Release reset

1: Reset

• IRQ1: Interrupt Control Register 1

Bit	7	6	5	4	3	2	1	0
Name	RXTO	RXFFOW	—	—	RXDETS[1:0]		IRQCPOR	IRQPOR
R/W	R	R	—	—	R/W		R/W	R/W
Reset	0	0	0	0	1	0	0	1

Bit 7 **RXTO**: RX time-out flag

0: RX time-out does not occur

1: RX time-out occurs

This flag will be set high by hardware when the RX time-out condition occurs and automatically cleared when a Light Sleep strobe command is received, when the device enters the RX continuous mode, when WOR/WOT wake up occurs or when the device enters the ARK TX/RX mode.

Bit 6 **RXFFOW**: RX FIFO overwrite flag

0: RX FIFO overwrite does not occur

1: RX FIFO overwrite occurs

This flag will be set high by hardware when the RX FIFO overwrite condition occurs and automatically cleared when a RX FIFO reset strobe command or a RX strobe command is received.

Bit 5~4 Reserved, must be “00”

Bit 3~2 **RXDETS[1:0]**: RX detect selection

00: Detect carry

01: Detect preamble

10/11: Detect SYNCWORD

Bit 1 **IRQCPOR**: IRQ flags clearing polarity selection

0: IRQ flags are cleared by writing 0 to the corresponding bits

1: IRQ flags are cleared by writing 1 to the corresponding bits

Bit 0 **IRQPOR**: IRQ signal polarity selection

0: Active low

1: Active high

When an IRQ flag in the IRQ3 register is set high and the corresponding IRQ function is enabled, the active level of the IRQ signal is determined by this configuration.

• IRQ2: Interrupt Control Register 2

Bit	7	6	5	4	3	2	1	0
Name	ARKTFIE	ATRCTIE	FIFOLTIE	RXERRIE	RXDETIE	CALCMPIE	RXCMPPIE	TXCMPPIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 **ARKTFIE**: ARK TX Failure IRQ Enable

0: Disable

1: Enable

Bit 6 **ATRCTIE**: ATR Cycle Timer IRQ Enable

0: Disable

1: Enable

Bit 5 **FIFOLTIE**: FIFO Low Threshold IRQ Enable

0: Disable

1: Enable

- Bit 4 **RXERRIE**: RX Error IRQ Enable
 0: Disable
 1: Enable
- Bit 3 **RXDETIE**: RX Event Detected IRQ Enable
 0: Disable
 1: Enable
- Bit 2 **CALCMPIE**: Calibration Complete IRQ Enable
 0: Disable
 1: Enable
- Bit 1 **RXCMPPIE**: RX Complete IRQ Enable
 0: Disable
 1: Enable
- Bit 0 **TXCMPPIE**: TX Complete IRQ Enable
 0: Disable
 1: Enable

• **IRQ3: Interrupt Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	ARKTFIF	ATRCTIF	FIFOLTIF	RXERRIF	RXDETIF	CALCMPIF	RXCMPPIF	TXCMPPIF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

When the individual flag within this register is set high by the hardware, the corresponding IRQ will be generated. These flags can be cleared by writing 0 or 1 to the corresponding flag which is determined by the IRQCPOR bit configuration.

- Bit 7 **ARKTFIF**: ARK TX Failure IRQ Flag
 0: No request
 1: Interrupt request
- Bit 6 **ATRCTIF**: ATR Cycle Timer IRQ Flag
 0: No request
 1: Interrupt request
 This flag will be set high when the ATRCT timer is full.
- Bit 5 **FIFOLTIF**: FIFO Low Threshold IRQ Flag
 0: No request
 1: Interrupt request
 When in the Burst TX mode, if this flag is set high, it means that TX FIFO data length is less than FFMG setting threshold and there are TX data to be written into the FIFO. When in the Burst RX mode, if this flag is set high, it means that RX FIFO remaining space is less than FFMG setting threshold and the remaining RX data length is longer than FFMG setting threshold.
- Bit 4 **RXERRIF**: RX Error IRQ Flag
 0: No request
 1: Interrupt request
 The RX error conditions include RX failure, CRC failure (CRC_EN=1) or RX FIFO overwrite.

- Bit 3 **RXDETIF**: RX Event Detected IRQ Flag
 0: No request
 1: Interrupt request
 The RX events include carry, preamble and syncword and the actual trigger source is determined by the RXDETS[1:0] configuration.
- Bit 2 **CALCMPIF**: Calibration Complete IRQ Flag
 0: No request
 1: Interrupt request
 If ACAL_EN=0, the LIRC calibration is enabled by its individual calibration enable bit and the calibration completion will trigger IRQ. If ACAL_EN=1, VCO and RC calibrations are enabled and both completion will trigger IRQ.
- Bit 1 **RXCMPPIF**: RX Complete IRQ Flag
 0: No request
 1: Interrupt request
 When the RX operation is completed without any error, this flag will be set high by hardware.
- Bit 0 **TXCMPIF**: TX Complete IRQ Flag
 0: No request
 1: Interrupt request

• **IO1: I/O Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	PADDS[1:0]		GIO2S[2:0]			GIO1S[2:0]		
R/W	R/W		R/W			R/W		
POR	0	1	0	0	0	0	0	0

- Bit 7~6 **PADDS[1:0]**: PAD driving strength selection (only reset by POR)
 00: 0.5mA
 01: 1mA
 10: 5mA
 11: 10mA

- Bit 5~3 **GIO2S[2:0]**: GIO2 pin function selection (only reset by POR)
 000/111: No function, input
 001: SDO, 4-wire SPI data, output
 010: TRXD, direct mode TXD/RXD, input/output
 011: TXD, direct mode TXD, input
 100: RXD, direct mode RXD, output
 101: IRQ, interrupt request, output
 110: ROSCi, ATR clock external input

- Bit 2~0 **GIO1S[2:0]**: GIO1 pin function selection (only reset by POR)
 000/111: No function, input
 001: SDO, 4-wire SPI data, output
 010: TRXD, direct mode TXD/RXD, input/output
 011: TXD, direct mode TXD, input
 100: RXD, direct mode RXD, output
 101: IRQ, interrupt request, output
 110: ROSCi, ATR clock external input

• IO2: I/O Control Register 2

Bit	7	6	5	4	3	2	1	0
Name	GIO4S[3:0]				GIO3S[3:0]			
R/W	R/W				R/W			
POR	0	0	0	0	0	0	0	0

Bit 7~4 **GIO4S[3:0]**: GIO4 pin function selection (only reset by POR)

- 0000/0111/1111: No function, input
- 0001: SDO, 4-wire SPI data, output
- 0010: TRXD, direct mode TXD/RXD, input/output
- 0011: TXD, direct mode TXD, input
- 0100: RXD, direct mode RXD, output
- 0101: IRQ, interrupt request, output
- 0110: ROSCi, ATR clock external input
- 1000: TBCLK, TX bit (data) clock, output
- 1001: RBCLK, RX bit (recovery) clock, output
- 1010: FSYCK, i.e. XCLK 1/1, 1/2, 1/4, 1/8 output
- 1011: LIRCCLK, internal LIRC clock with debounce, output
- 1100: EPA_EN, external PA enable, output
- 1101: ELAN_EN, external LNA enable, output
- 1110: TRBCLK, TBCLK in TX mode or RBCLK in RX mode, output

Bit 3~0 **GIO3S[3:0]**: GIO3 pin function selection (only reset by POR)

- 0000/0111/1111: No function, input
- 0001: SDO, 4-wire SPI data, output
- 0010: TRXD, direct mode TXD/RXD, input/output
- 0011: TXD, direct mode TXD, input
- 0100: RXD, direct mode RXD, output
- 0101: IRQ, interrupt request, output
- 0110: ROSCi, ATR clock external input
- 1000: TBCLK, TX bit (data) clock, output
- 1001: RBCLK, RX bit (recovery) clock, output
- 1010: FSYCK, i.e. XCLK 1/1, 1/2, 1/4, 1/8 output
- 1011: LIRCCLK, internal LIRC clock with debounce, output
- 1100: EPA_EN, external PA enable, output
- 1101: ELAN_EN, external LNA enable, output
- 1110: TRBCLK, TBCLK in TX mode or RBCLK in RX mode, output

• IO3: I/O Control Register 3

Bit	7	6	5	4	3	2	1	0
Name	SDO_TEN	SPIPU	—	GIOPU[4:1]				—
R/W	R/W	R/W	—	R/W				—
POR	0	1	1	1	1	1	1	1

Bit 7 **SDO_TEN**: SDO tri-state enable (only reset by POR)

0: Disable

1: Enable

Bit 6 **SPIPU**: 3-wire SPI pull-up enable (only reset by POR)

0: Disable

1: Enable

When this bit is set high, it only controls the pull-up function for the CSN, SCK and SDIO pins. Note that the pull-up function of the SDO pin for the 4-wire SPI is configured using the GIOPU[4:1] bits.

Bit 5 Reserved, must be “1”

Bit 4~1 **GIOPU[4:1]**: GIO pin function pull-up enable control (only reset by POR)

These bits control the pull-high function of the GIO4~GIO1 pins respectively.

Bit 0 Reserved, must be “1”

• FIFO1: FIFO Control Register 1

Bit	7	6	5	4	3	2	1	0
Name	—	—	TXFFSA[5:0]					
R/W	—	—	R/W					
Reset	0	0	0	0	0	0	0	0

Bit 7~6 Reserved, must be “00”

Bit 5~0 **TXFFSA[5:0]**: TX FIFO start address, used for Block FIFO mode

• FIFO2: FIFO Control Register 2

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	RXPL2F_EN	FFINF_EN	FFMG_EN	FFMG[1:0]	
R/W	—	—	—	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	1

Bit 7~5 Reserved, must be “000”

Bit 4 **RXPL2F_EN**: RX payload length byte to FIFO enable

0: Disable

1: Enable

Setting this bit high will place the payload length byte in the packet to RX FIFO. In the RX continue mode (RXCON_EN=1), this bit should be set to 1 to support multiple payload in single RX FIFO.

Bit 3 **FFINF_EN**: FIFO infinite length mode enable

0: Disable

1: Enable

Bit 2 **FFMG_EN**: FIFO length margin detect enable

0: Disable

1: Enable

Bit 1~0 **FFMG[1:0]**: FIFO length margin selection

Threshold of remaining data in TX FIFO:

00: 4 bytes

01: 8 bytes

10: 16 bytes

11: 32 bytes

Threshold of remaining space in RX FIFO:

00: 4 bytes

01: 8 bytes

10: 16 bytes

11: 32 bytes

After the FIFO length margin detect function has been enabled by setting the FFMG_EN bit high and the required FIFO length margin has been selected by setting these bits, when the selected condition occurs the FIFOLTIF flag will be set high. In this case, an interrupt signal will also be generated if the corresponding interrupt function has been enabled.

• **PKT1: Packet Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	TXPMLN[7:0]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	1

Bit 7~0 **TXPMLN[7:0]**: TX preamble length

Transmit preamble length = (TXPMLN[7:0]+1) bytes

• **PKT2: Packet Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	PID[1:0]		TRAILER_EN	WHTFMT	SYNCLEN[1:0]		RXPMLN[1:0]	
R/W	R/W		R/W	R/W	R/W		R/W	
Reset	0	0	1	0	0	1	1	0

Bit 7~6 **PID[1:0]**: TX Packet ID

This ID will be placed in the highest two bits of the payload header field when the header option is enabled using the PLH_EN bit.

Bit 5 **TRAILER_EN**: Trailer field enable

0: Disable

1: Enable

Bit 4 **WHTFMT**: Whitening format selection

0: $P(X)=X^7+X^6+X^5+X^4+1$

1: $P(X)=X^7+X^4+1$ (PN7)

Bit 3~2 **SYNCLEN[1:0]**: TX/RX mode SYNCWORD length selection

00: Reserved

01: 4 bytes

10: 6 bytes

11: 8 bytes

Bit 1~0 **RXPMLN[1:0]**: RX preamble detection length selection

00: 0 byte – no preamble detection

01: 1 byte

10: 2 bytes

11: 4 bytes

• PKT3: Packet Control Register 3

Bit	7	6	5	4	3	2	1	0
Name	MCH_EN	FEC_EN	CRC_EN	CRCFMT	PLEN_EN	PLHAC_EN	PLHLEN	PLH_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	0	0	0	0	0

Bit 7 **MCH_EN**: Manchester code enable

0: Disable

1: Enable

Bit 6 **FEC_EN**: FEC enable

0: Disable

1: Enable

Bit 5 **CRC_EN**: CRC field enable

0: Disable

1: Enable

Bit 4 **CRCFMT**: CRC format selection

0: CCITT-16-CRC $G(X) = X^{16} + X^{12} + X^5 + 1$

1: IBC-16-CRC $G(X) = X^{16} + X^{15} + X^2 + 1$

Bit 3 **PLEN_EN**: Payload length field enable

0: Disable

1: Enable

Bit 2 **PLHAC_EN**: Payload header address correction enable control

0: Disable, PLHA[5:0] in the PKT8 register can be used as software flags defined by users.

1: Enable, PLHA[5:0] of TX/RX devices must include the same address, otherwise the packet will be regarded as a failed packet.

Note: If PLHLEN = 1 and PLHAC_EN = 1, the PLHEA[7:0] is still used as the address function.

Bit 1 **PLHLEN**: Payload header length

0: 1 byte

1: 2 bytes

Bit 0 **PLH_EN**: Payload header field enable

0: Disable

1: Enable

• PKT4: Packet Control Register 4

Bit	7	6	5	4	3	2	1	0
Name	WHT_EN	WHTSD[6:0]						
R/W	R/W	R/W						
Reset	0	0	1	1	0	1	1	0

Bit 7 **WHT_EN**: Data whitening enable

0: Disable

1: Enable

Bit 6~0 **WHTSD[6:0]**: Data whitening seed

• PKT5: Packet Control Register 5

Bit	7	6	5	4	3	2	1	0
Name	TXDLEN[7:0]							
R/W	R/W							
Reset	0	1	0	0	0	0	0	0

Bit 7~0 **TXDLEN[7:0]**: TX data length (unit: byte, used in burst mode only)

• PKT6: Packet Control Register 6

Bit	7	6	5	4	3	2	1	0
Name	RXDLEN[7:0]							
R/W	R/W							
Reset	0	1	0	0	0	0	0	0

Bit 7~0 **RXDLEN[7:0]**: RX data length (unit: byte; used in burst mode only)

When the PLEN_EN bit is cleared to 0, the received data length is determined by this field.

When this register is read, the read value indicates the RX data length in FIFO. The default read value is 00h.

• PKT7: Packet Control Register 7

Bit	7	6	5	4	3	2	1	0
Name	RXPID[1:0]		DLY_RXS[2:0]			DLY_TXS[2:0]		
R/W	R		R/W			R/W		
Reset	0	0	1	0	0	0	0	0

Bit 7~6 **RXPID[1:0]**: Received packet PID (read only)

Bit 5~3 **DLY_RXS[2:0]**: RX block stable time after RX is enabled

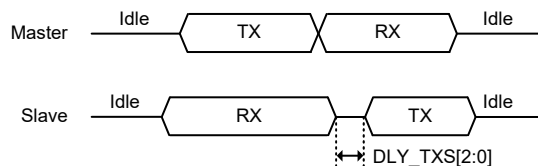
- 000: 4 μ s
- 001: 8 μ s
- 010: 12 μ s
- 011: 16 μ s
- 100: 20 μ s
- 101: 32 μ s
- 110: 64 μ s
- 111: 100 μ s

These bits are used to select the waiting time between RX enable and RX stable. This time should be configured to a value greater than the default RX DCOC turbo mode delay time of 6 μ s.

Bit 2~0 **DLY_TXS[2:0]**: TX start (delay) time before entering the TX mode

- 000: 0 μ s
- 001: 10 μ s
- 010: 20 μ s
- 011: 40 μ s
- 100: 60 μ s
- 101: 80 μ s
- 110: 100 μ s
- 111: 120 μ s

It is used to align the timing between transmitter and receiver in ARK mode.



• **PKT8: Packet Control Register 8**

Bit	7	6	5	4	3	2	1	0
Name	—	—	PLHA[5:0]					
R/W	—	—	R/W					
Reset	0	0	0	0	0	0	0	0

Bit 7~6 Reserved, must be “00”

Bit 5~0 **PLHA[5:0]**: Payload header address to support broadcast

Address=0 in RX mode means not doing correction check.

Write: write data to TX PLHA[5:0]. Read: read data from RX PLHA[5:0].

• **PKT9: Packet Control Register 9**

Bit	7	6	5	4	3	2	1	0
Name	PLHEA[7:0]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **PLHEA[7:0]**: Payload header extended address to support broadcast

Address=0 in RX mode means not doing correction check.

• **MOD1: Modulator Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	DTR[7:0]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	1

Bit 7~0 **DTR[7:0]**

DTR[8:0]: Data rate divider, DTR[8] is located in the MOD2 register.

Data Rate= $f_{XTAL}/[(XODIV2+1) \times 32 \times (DTR[8:0]+1)]$, XODIV2=0, here data rate indicates TBCLK. Note that DTR[8:0] can only be an odd number.

• **MOD2: Modulator Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	RXIFOS[11:8]				DITHER[1:0]		—	DTR[8]
R/W	R/W				R/W		—	R/W
Reset	1	0	0	1	0	0	0	0

Bit 7~4 **RXIFOS[11:8]**

RXIFOS[11:0]: RX intermediate frequency offset, RXIFOS[7:0] is located in the MOD3 register.

Write to RXIFOS[11:8] first and then write to RXIFOS[7:0] to fully update RXIFOS[11:0].

$RXIFOS[11:0] = \text{floor}\{f_{IF}/[f_{XTAL}/(XODIV2+1)] \times 2^{17}\}$, XODIV2=0

Bit 3~2 **DITHER[1:0]**: Dither value

Bit 1 Reserved, must be “0”

Bit 0 DTR[8]

DTR[8:0]: Data rate divider, DTR[7:0] is located in the MOD1 register.

Data Rate= $f_{XTAL}/[(XODIV2+1) \times 32 \times (DTR[8:0]+1)]$, XODIV2=0, here data rate indicates TBCLK. Note that DTR[8:0] can only be an odd number.

• MOD3: Modulator Control Register 3

Bit	7	6	5	4	3	2	1	0
Name	RXIFOS[7:0]							
R/W	R/W							
Reset	1	0	0	1	1	0	1	0

Bit 7~0 RXIFOS[7:0]

RXIFOS[11:0]: RX intermediate frequency offset, RXIFOS[11:8] is located in the MOD2 register.

Write to RXIFOS[11:8] first and then write to RXIFOS[7:0] to fully update RXIFOS[11:0].

$RXIFOS[11:0] = \text{floor}\{f_{IF}/[f_{XTAL}/(XODIV2+1)] \times 2^{17}\}$, XODIV2=0

• DM1: Demodulator Control Register 1

Bit	7	6	5	4	3	2	1	0
Name	—	—	MDIV[5:0]					
R/W	—	—	R/W					
Reset	0	0	0	0	0	0	1	1

Bit 7~6 Reserved, must be “00”

Bit 5~0 MDIV[5:0]: Demodulator operation clock divider

$DMCLK = ADCLK / (MDIV[5:0] + 1)$

• DM2: Demodulator Control Register 2

Bit	7	6	5	4	3	2	1	0
Name	PREAMBLE_CFO_EN1	PREAMBLE_CFO_EN0	SDR[5:0]					
R/W	R/W	R/W	R/W					
Reset	0	1	0	0	0	0	0	0

Bit 7 PREAMBLE_CFO_EN1: Enable 2nd stage CFO correction in preamble

0: Disable

1: Enable

Note that this bit can only be set if the preamble length is 4 bytes, i.e., RXPMLN[1:0]=11b.

Bit 6 PREAMBLE_CFO_EN0: Enable 1st stage CFO correction in preamble

0: Disable

1: Enable

Bit 5~0 SDR[5:0]: Decimator operation clock after phase extract

$SDR[5:0]+1 = DMCLK / (8 \times DATA_RATE)$, here DATA_RATE indicates RBCLK.

• DM3: Demodulator Control Register 3

Bit	7	6	5	4	3	2	1	0
Name	CSF_SW_EN	FD_MOD[6:0]						
R/W	R/W	R/W						
Reset	1	1	1	0	0	0	0	0

Bit 7 **CSF_SW_EN**: Channel selection filter auto bandwidth switch enable

0: Disable

1: Enable

Bit 6~0 **FD_MOD[6:0]**: Frequency deviation modifier

$FD_MOD = \text{Round}((h / (SDR[5:0] + 1)) \times 128)$; h=modulation index

$SDR[5:0] + 1 = DMCLK / (8 \times DATA_RATE)$

• DM4: Demodulator Control Register 4

Bit	7	6	5	4	3	2	1	0
Name	THOLD[3:0]			CFO_DSEL	—	PH_DIFF_MOD	PRE_CSF_EN	
R/W	R/W			R/W	—	R/W	R/W	
Reset	0	0	0	1	1	0	0	

Bit 7~4 **THOLD[3:0]**: Detection errors threshold

THOLD[3:2]: Preamble detection errors bit number threshold

THOLD[1:0]: SYNCWORD detection errors bit number

Bit 3 **CFO_DSEL**: CFO correction domain selection

0: Analog domain

1: Digital domain

Bit 2 Reserved, must be “0”

Bit 1 **PH_DIFF_MOD**: Phase difference extract mode setting

0: Phase extract range $[-\pi/2, \pi/2]$

1: Phase extract range $[-\pi, \pi]$

Bit 0 **PRE_CSF_EN**: Switch receiver filter bandwidth when preamble is matched

0: Disable

1: Enable

• DM5: Demodulator Control Register 5

Bit	7	6	5	4	3	2	1	0
Name	FD_HOLD[7:0]							
R/W	R/W							
Reset	0	0	1	1	0	0	0	0

Bit 7~0 **FD_HOLD[7:0]**: Frequency deviation threshold for preamble detection

• DM8: Demodulator Control Register 8

Bit	7	6	5	4	3	2	1	0
Name	M_RATIO[7:0]							
R/W	R/W							
Reset	0	1	0	0	0	0	0	0

Bit 7~0 **M_RATIO[7:0]**: For CFO calculation

$M_RATIO = \text{round}(1 / (MDIV[5:0] + 1) \times 2^8)$

Bank 0 Control Registers

All control registers will be set to their initial value by power-on reset (POR). The software reset will set the control registers to their initial value except the LIRC_EN, LIRC_OP[4:0], LIRC_OW and LIRCCAL_EN bits in the XO3 register. These bits keep unchanged after software reset.

Addr.	Name	Bit								
		7	6	5	4	3	2	1	0	
20h	OM	PWR_SOFT	BAND_SEL[1:0]		—	ACAL_EN	RTX_EN	RTX_SEL	SX_EN	
22h	SX1	—	D_N[6:0]							
23h	SX2	D_K[7:0]								
24h	SX3	D_K[15:8]								
25h	SX4	—	—	—	—	D_K[19:16]				
26h	STA1	—	—	—	CD_FLAG	—	OMST[2:0]			
28h	RSSI2	—				RSSI_CTHD[3:0]				
29h	RSSI3	RSSI_NEGDB[7:0]								
2Ah	RSSI4	RSSI_SYNC_OK[7:0]								
2Bh	ATR1	ATRCLK_DIV[1:0]		ATRCLKS	ARTTU	ATRCTM	ATRM[1:0]		ATR_EN	
2Ch	ATR2	ATRCYC[7:0]								
2Dh	ATR3	ATRCYC[15:8]								
2Eh	ATR4	ATRRXAP[7:0]								
2Fh	ATR5	ATRRXEP[7:0]								
30h	ATR6	ATRRXEP[15:8]								
31h	ATR7	ARKNM[3:0]				—	ATR_WDLY[1:0]		ARK_EN	
32h	ATR8	ARKRXAP[7:0]								
33h	ATR9	ATRCT[7:0]								
34h	ATR10	ATRCT[15:8]								
35h	ATR11	—				ATRRXAP[10:8]				
3Ch	XO1	XSHIFT[1:0]		—	XO_TRIM[4:0]					
3Dh	XO2	—	—	—	—	XODIV2	—			
3Eh	XO3	LIRCCAL_EN	LIRC_OW	LIRC_OP[4:0]				LIRC_EN		
3Fh	TX2	—				CT_PAD[3:0]				

Note: Addresses 21h, 27h and 36h~3Bh which are not listed in this table are reserved for future use, it is suggested not to change their initial values by any methods.

The reset value shown in the following register description tables means the software reset results of strobe command.

• OM: Operation Mode Control Register

Bit	7	6	5	4	3	2	1	0
Name	PWR_SOFT	BAND_SEL[1:0]		—	ACAL_EN	RTX_EN	RTX_SEL	SX_EN
R/W	R/W	R/W		—	R/W	R/W	R/W	R/W
Reset	0	0	1	0	0	0	0	0

Bit 7 **PWR_SOFT**: RF operation mode selection

- 0: RF normal operation mode
- 1: RF engineering mode

Bit 6~5 **BAND_SEL[1:0]**: Band selection (when PWR_SOFT=0)

- 00: 315MHz band
- 01: 433MHz band
- 10: 470~510MHz band
- 11: 868/915MHz band

- Bit 4 Reserved, must be “0”
- Bit 3 **ACAL_EN**: Auto calibration enable
 0: Disable
 1: Enable
 When this bit is set high, both the VCO and RC calibrations will be enabled. When the VCO and RC calibrations are completed, this bit will be cleared to zero by hardware.
- Bit 2 **RTX_EN**: RX or TX mode enable
 0: Disable
 1: Enable
 After the RX or TX mode has been selected by the RTX_SEL bit, setting this bit high will enable the selected mode.
- Bit 1 **RTX_SEL**: RX or TX mode selection
 0: RX mode
 1: TX mode
- Bit 0 **SX_EN**: Synthesizer enable (standby mode enable control)
 0: Disable
 1: Enable
 Setting this bit high will enable the PFD, CP and VCO functions.

• **SX1: Fractional-N Synthesizer Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	D_N[6:0]							
R/W	R/W							
Reset	0	0	0	1	1	0	1	1

- Bit 7 Reserved, must be “0”
- Bit 6~0 **D_N[6:0]**: RF channel integer number code
 $D_N[6:0] = \text{floor}\{f_{RF}/[f_{XTAL}/(XODIV2+1)]\}$
 For example, XO=16MHz and RF band=433.92MHz which are initial setup:
 → $433.92\text{MHz}/16\text{MHz}=27.12$
 → $D_N=27$
 → $\text{Dec2Hex}(27)=1B$
 → $\text{Dec2Bin}(27)=001_1011$

• **SX2: Fractional-N Synthesizer Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	D_K[7:0]							
R/W	R/W							
Reset	1	0	0	0	0	1	0	1

- Bit 7~0 **D_K[7:0]**: RF channel fractional number code lowest byte

• **SX3: Fractional-N Synthesizer Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	D_K[15:8]							
R/W	R/W							
Reset	1	1	1	0	1	0	1	1

- Bit 7~0 **D_K[15:8]**: RF channel fractional number code medium byte

• SX4: Fractional-N Synthesizer Control Register 4

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	D_K[19:16]			
R/W	—	—	—	—	R/W			
Reset	0	0	0	0	0	0	0	1

Bit 7~4 Reserved, must be “0000”

Bit 3~0 **D_K[19:16]**: RF channel fractional number code highest byte

$$D_K[19:0]=\text{floor}\left\{\left(\frac{f_{RF}}{f_{XTAL}/(XODIV2+1)}\right)-D_N[6:0]\right\}\times 2^{20}$$

For example, XO=16MHz and RF band=433.92MHz which are initial setup:

$$\rightarrow 433.92\text{MHz}/16\text{MHz}=27.12$$

$$\rightarrow D_K=0.12\times 2^{20}=125829$$

$$\rightarrow \text{Dec2Hex}(125829)=1\text{EB}85$$

$$\rightarrow \text{Dec2Bin}(125829)=0001_1110_1011_1000_0101$$

• STA1: Status Control Register 1

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	CD_FLAG	—	OMST[2:0]		
R/W	—	—	—	R	—	R		
Reset	0	0	0	0	0	0	0	0

Bit 7~5 Reserved, must be “000”

Bit 4 **CD_FLAG**: Carrier detection flag (read only)

This flag will be set high by hardware when carrier detection is okay after pulling DEMOD_EN high. Here DEMOD_EN high level is an internal signal which is generated by the internal state machine when in the Direct mode (DIR_EN=1) or after the RX strobe command is received when in the Burst mode (DIR_EN=0). The flag will be automatically cleared when RX_EN rising edge occurs. Here RX_EN rising edge is generated after setting RTX_SEL=0 and RTX_EN=1 when in the Direct mode or by the internal state machine after the RX strobe command is received when in the Burst mode.

Bit 3 Reserved, must be “0”

Bit 2~0 **OMST[2:0]**: Operation mode state indication (read only)

000: Deep Sleep mode

001: Idle mode

010: Light Sleep mode

011: Standby mode

100: TX mode

101: RX mode

110: VCO calibration mode

111: Undefined

• RSSI2: RSSI Control Register 2

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	RSSI_CTHD[3:0]			
R/W	—	—	—	—	R/W			
Reset	0	0	0	0	1	0	1	0

Bit 7~4 Reserved, must be “0000”

Bit 3~0 **RSSI_CTHD[3:0]**: RSSI threshold for carrier detection

$$(\text{RSSI_CTHD}[3:0]\times 2+1)+74=\text{RSSI threshold for carrier detection}$$

• RSSI3: RSSI Control Register 3

Bit	7	6	5	4	3	2	1	0
Name	RSSI_NEGDB[7:0]							
R/W	R							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **RSSI_NEGDB[7:0]**: RSSI value (unit: -dB)

It is a real time measurement value.

• RSSI4: RSSI Control Register 4

Bit	7	6	5	4	3	2	1	0
Name	RSSI_SYNC_OK[7:0]							
R/W	R							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **RSSI_SYNC_OK[7:0]**: RSSI snapshot when SYNCWORD is detected correct

• ATR1: Auto TX/RX Control Register 1

Bit	7	6	5	4	3	2	1	0
Name	ATRCLK_DIV[1:0]		ATRCLKS	ARTTU	ATRCTM	ATRM[1:0]		ATR_EN
R/W	R/W		R/W	R/W	R/W	R/W		R/W
Reset	1	1	0	0	1	0	0	0

Bit 7~6 **ATRCLK_DIV[1:0]**: ATR clock frequency selection

00: 1/1, ATRCLK=32768Hz

01: 1/4, ATRCLK=8192Hz

10: 1/8, ATRCLK=4096Hz

11: 1/16, ATRCLK=2048Hz

Bit 5 **ATRCLKS**: ATRCLK clock source selection

0: From the internal LIRC clock

1: From the external ROSCi clock input on the GIO_n pin

Bit 4 **ARTTU**: Auto TRX unit time selection

0: 250μs

1: 1ms, used to support low data rate applications

This bit is used to select the unit time for the ATR RX active period (ATRRXAP[10:0]), ATR RX extended period (ATRRXEP[15:0]) and ARK RX active period (ARKRXAP[7:0]).

Bit 3 **ATRCTM**: Auto TRX timer mode selection

0: Single mode, restart ATRCT timer when every ATR transaction occurs.

1: Continuous mode, start ATRCT timer upon receiving Idle command; stop ATRCT timer when ATR_EN=0 or ATRCTM=0 and exit the ATR active period.

Bit 2~1 **ATRM[1:0]**: Auto TRX mode selection

00: ATR WOT mode

01: ATR WOR mode

10/11: ATR WTM mode

Bit 0 **ATR_EN**: Auto TRX enable

0: Disable

1: Enable

Note that the ATR functions are activated by operation state transition from Deep Sleep/Light Sleep mode to Idle mode.

• ATR2: Auto TX/RX Control Register 2

Bit	7	6	5	4	3	2	1	0
Name	ATRCYC[7:0]							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

Bit 7~0 **ATRCYC[7:0]**: ATRCT timer expire value low byte

• ATR3: Auto TX/RX Control Register 3

Bit	7	6	5	4	3	2	1	0
Name	ATRCYC[15:8]							
R/W	R/W							
Reset	0	0	0	0	1	1	1	1

Bit 7~0 **ATRCYC[15:8]**: ATRCT timer expire value high byte

Wake-up period = ATRCLK period×ATRCYC[15:0]+LIRCCLK period, ATRCYC[15:0]≠0. Default wake-up period is 2 seconds.

• ATR4: Auto TX/RX Control Register 4

Bit	7	6	5	4	3	2	1	0
Name	ATRRXAP[7:0]							
R/W	R/W							
Reset	0	0	1	0	0	1	1	1

Bit 7~0 **ATRRXAP[7:0]**: ATR RX active period low byte

ATR RX active period high byte ATRRXAP[10:8] is located in the ATR11 register.

Active period=unit time×(ATRRXAP[10:0]+1); the unit time can be 250μs or 1ms which is determined by the ATRTU bit. The default ATR RX active period is 10ms with a default time unit of 250μs.

• ATR5: Auto TX/RX Control Register 5

Bit	7	6	5	4	3	2	1	0
Name	ATRRXEP[7:0]							
R/W	R/W							
Reset	1	0	0	0	1	1	1	1

Bit 7~0 **ATRRXEP[7:0]**: ATR RX extend period low byte

• ATR6: Auto TX/RX Control Register 6

Bit	7	6	5	4	3	2	1	0
Name	ATRRXEP[15:8]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	1

Bit 7~0 **ATRRXEP[15:8]**: ATR RX extended period high byte

Extend period=unit time×(ATRRXEP[15:0]+1); the unit time can be 250μs or 1ms which is determined by the ATRTU bit. The default ATR RX extended period is 100ms with a default time unit of 250μs.

• ATR7: Auto TX/RX Control Register 7

Bit	7	6	5	4	3	2	1	0
Name	ARKNM[3:0]				—	ATR_WDLY[1:0]		ARK_EN
R/W	R/W				—	R/W		R/W
Reset	0	1	1	1	0	0	1	0

Bit 7~4 **ARKNM[3:0]**: ARK repeat cycle number
 Maximum repeat cycle number=ARKNM[3:0]+1

Bit 3 Reserved, must be “0”

Bit 2~1 **ATR_WDLY[1:0]**: Auto wake up delay time
 00: 244μs
 01: 488μs
 10: 732μs
 11: 976μs

Bit 0 **ARK_EN**: Auto-Resend/ACK enable
 0: Disable
 1: Enable

• ATR8: Auto TX/RX Control Register 8

Bit	7	6	5	4	3	2	1	0
Name	ARKRXAP[7:0]							
R/W	R/W							
Reset	0	0	1	0	0	1	1	1

Bit 7~0 **ARKRXAP[7:0]**: ARK RX active period
 Active period=unit time×(ARKRXAP[7:0]+1); the unit time can be 250μs or 1ms which is determined by the ATRTU bit. The default ARK RX active period is 10ms with a default time unit of 250μs.

• ATR9: Auto TX/RX Control Register 9

Bit	7	6	5	4	3	2	1	0
Name	ATRCT[7:0]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **ATRCT[7:0]**: ATR cycle timer low byte

• ATR10: Auto TX/RX Control Register 10

Bit	7	6	5	4	3	2	1	0
Name	ATRCT[15:8]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **ATRCT[15:8]**: ATR cycle timer high byte
 Reading ATRCT[15:0] will get the current count value. Due to the limitation of SPI 8-bit data length, reading the ATR9 register will take a snapshot of the whole 16-bit data into the read register buffer. Users should read ATR9 and ATR10 continuously (non-interrupted) to get correct data.
 Writing to ATRCT[15:0] will update the count value. Write to ATR9 first and then write to ATR10 to trigger the ATRCT write function. This timer update mechanism is used to align the time slot for the master and slave in a two-way RF system.

• ATR11: Auto TX/RX Control Register 11

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	ATTRXAP[10:8]		
R/W	—	—	—	—	—	R/W		
Reset	0	0	0	0	0	0	0	0

Bit 7~3 Reserved, must be “00000”

Bit 2~0 **ATTRXAP[10:8]**: ATR RX active period high byte

ATR RX active period low byte ATTRXAP[7:0] is located in the ATR4 register.

Active period=unit time×(ATTRXAP[10:0]+1); the unit time can be 250μs or 1ms which is determined by the ATRTU bit. The default ATR RX active period is 10ms with a default time unit of 250μs.

• XO1: XO Control Register 1

Bit	7	6	5	4	3	2	1	0
Name	XSHIFT[1:0]		—	XO_TRIM[4:0]				
R/W	R/W		—	R/W				
Reset	0	0	0	1	0	0	0	0

Bit 7~6 **XSHIFT[1:0]**: Coarse tune of XO load capacitor for different crystal C_{LOAD}

Bit 5 Reserved, must be “0”

Bit 4~0 **XO_TRIM[4:0]**: Fine tune of XO load capacitor

The recommended values for the XO1 register are listed below (based on XO fabricated by YOKETAN corporation).

C_{LOAD}	12pF	16pF	20pF
49US 16MHz XO	1Bh	52h	8Fh
3225MD 16MHz XO	40h	5Dh	90h

49US 16MHz XO

12pF CLOAD: The default setting is 1Bh. Within ±40ppm frequency error, 1 trim code shifts -3.9ppm.

16pF CLOAD: The default setting is 52h. Within ±40ppm frequency error, 1 trim code shifts -2.25ppm.

20pF CLOAD: The default setting is 8Fh. Within ±40ppm frequency error, 1 trim code shifts -1.4ppm.

3225SMD 16MHz XO

12pF CLOAD: The default setting is 40h. Within ±20ppm frequency error, 1 trim code shifts -0.7ppm.

16pF CLOAD: The default setting is 5Dh. Within ±20ppm frequency error, 1 trim code shifts -0.46ppm.

20pF CLOAD: The default setting is 90h. Within ±20ppm frequency error, 1 trim code shifts -0.34ppm.

• XO2: XO Control Register 2

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	XODIV2	—	—	—
R/W	—	—	—	—	R/W	—	—	—
Reset	0	0	0	0	0	0	1	1

Bit 7~4 Reserved, must be “0000”

Bit 3 **XODIV2**: XO output divided by 2 enable

0: Disable

1: Enable

Note: f_{XTAL} =16MHz, XODIV2 must be “0”.

Bit 2~0 Reserved, must be “011”

• XO3: XO Control Register 3

Bit	7	6	5	4	3	2	1	0
Name	LIRCCAL_EN	LIRC_OW	LIRC_OP[4:0]				LIRC_EN	
R/W	R/W	R/W	R/W				R/W	
POR	0	0	0	1	1	0	1	0

Bit 7 **LIRCCAL_EN**: LIRC calibration enable

0: Disable

1: Enable

Bit 6 **LIRC_OW**: LIRC overwrite control

0: LIRC_OP[4:0] from calibration engine

1: LIRC_OP[4:0] from control register

Bit 5~1 **LIRC_OP[4:0]**: LIRC trim

After writing data to LIRC_OP[4:0], this trim will become active when the LIRC_OW bit is set high. When reading data from LIRC_OP[4:0], the actual data source is determined by the LIRC_OW bit setting.

Bit 0 **LIRC_EN**: LIRC enable

0: Disable

1: Enable

• TX2: TX Control Register 2

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	CT_PAD[3:0]			
R/W	—	—	—	—	R/W			
Reset	0	0	0	0	1	0	0	0

Bit 7~4 Reserved, must be “0000”

Bit 3~0 **CT_PAD[3:0]**: RF Output Power Control

RF Output Power	CT_PAD[3:0]	
	433MHz	868MHz
13dBm	Dh	Fh
10dBm	9h	Ah

The device offers several power level setting for 10dBm and 13dBm, respectively.

Note: The output power level could vary due to different matching components and the placement on the PCB. These matching variations could significantly impact the output power level below 5dBm.

Bank 1 Control Registers

All control registers will be set to their initial value by power-on reset (POR). The software reset will set the control registers to their initial value.

Addr.	Name	Bit						
		7	6	5	4	3	2	1
21h	AGC2	SAT_SEL[1:0]		—			AGC_CMP_THD[1:0]	
22h	AGC3	CDRST_THD_SEL[1:0]		ENAVG_SEL[1:0]		—	IF_DETOK_THD[2:0]	
23h	AGC4	GAIN_SEL[3:0]			—		AGC_ST[2:0]	
24h	AGC5	—				AGC_FSEL[1:0]		
26h	AGC7	GAIN_STB[7:0]						
2Ch	FCF1	—	—	SFRATIO[1:0]		—		
2Dh	FCF2	FSCALE[7:0]						

Addr.	Name	Bit							
		7	6	5	4	3	2	1	0
2Eh	FCF3	—				FSCALE[11:8]			
2Fh	FCF4	CF_B12[7:0]							
30h	FCF5	—				CF_B12[9:8]			
31h	FCF6	CF_B13[7:0]							
32h	FCF7	—				CF_B13[9:8]			
33h	FCF8	CF_A12[7:0]							
34h	FCF9	—				CF_A12[9:8]			
35h	FCF10	CF_A13[7:0]							
36h	FCF11	—				CF_A13[9:8]			
37h	FCF12	CF_B22[7:0]							
38h	FCF13	—				CF_B22[9:8]			
39h	FCF14	CF_B23[7:0]							
3Ah	FCF15	—				CF_B23[9:8]			
3Bh	FCF16	CF_A22[7:0]							
3Ch	FCF17	—				CF_A22[9:8]			
3Dh	FCF18	CF_A23[7:0]							
3Eh	FCF19	—				CF_A23[9:8]			

Note: Addresses 20h, 25h, 27h~2Bh and 3Fh which are not listed in this table are reserved for future use, it is suggested not to change their initial values by any methods.

The reset value shown in the following register description tables means the software reset results of strobe command.

• **AGC2: AGC Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	SAT_SEL[1:0]		—	—	—	—	AGC_CMP_THD[1:0]	
R/W	R/W		—	—	—	—	R/W	
Reset	0	1	0	0	0	0	0	0

Bit 7~6 **SAT_SEL[1:0]**: Saturation detection threshold selection

00: -6 dBFS

01: -8 dBFS

10: -10 dBFS

11: -12 dBFS

Note: “FS” indicates the ADC output full-scale.

Bit 5~2 Reserved, must be “0000”

Bit 1~0 **AGC_CMP_THD[1:0]**: AGC comparison number threshold

00: Continuous AGC comparison until SYNCWORD is detected

01~11: Comparison number threshold

• AGC3: AGC Control Register 3

Bit	7	6	5	4	3	2	1	0
Name	CDRST_THD_SEL[1:0]		ENVAVG_SEL[1:0]		—	IF_DETOK_THD[2:0]		
R/W	R/W		R/W		—	R/W		
Reset	0	0	1	0	0	1	0	0

Bit 7~6 **CDRST_THD_SEL[1:0]**: Carrier signal threshold to reset AGC

CDRST_THD_SEL[1:0]	GAIN_SEL[3:0]		
	0010b	0011b	Other Values
00b	-32 dBFS	-41 dBFS	-48 dBFS
01b	-35 dBFS	-44 dBFS	-48 dBFS
10b	-38 dBFS	-47 dBFS	-48 dBFS
11b	-41 dBFS	-48 dBFS	-48 dBFS

If the AGC completion state is reached and the signal strength detected is below the preset threshold, the AGC flow will be reset and then restarted.

Bit 5~4 **ENVAVG_SEL[1:0]**: Envelop detection average ratio selection

00: 1/16

01: 1/32

10: 1/64

11: 1/128

Bit 3 Reserved, must be “0”

Bit 2~0 **IF_DETOK_THD[2:0]**: IF detection OK threshold

After the gain stable time which determined by the AGC7 register, the AGC circuit will wait for (IF_DETOK_THD[2:0]×8) ADCLK cycles before starting to detect the IF signal strength.

• AGC4: AGC Control Register 4

Bit	7	6	5	4	3	2	1	0
Name	GAIN_SEL[3:0]				—	AGC_ST[2:0]		
R/W	R				—	R		
Reset	0	0	0	1	0	0	0	1

Bit 7~4 **GAIN_SEL[3:0]**: Gain curve selection

0000: Gain curve is not selected

0001: Maximum gain is selected

0111: Minimum gain is selected

The available field value is from 0000 to 0111. The gain will automatically be selected by the hardware. This bit field and the CDRST_THD_SEL[1:0] bit field together determine the carrier signal strength threshold to reset AGC, refer to the AGC3 register.

Bit 3 Reserved, must be “0”

Bit 2~0 **AGC_ST[2:0]**: AGC state machine state

000~001: AGC is not completed

111: AGC is completed

• AGC5: AGC Control Register 5

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	AGC_FSEL[1:0]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	0	0

Bit 7~2 Reserved, must be “000000”

Bit 1~0 **AGC_FSEL[1:0]**: AGC filter configuration

AGC_FSEL[1]: HPF pass band set point

0: 5/32 ADCLK

1: 6/32 ADCLK

AGC_FSEL[0]: LPF pass band set point

0: 17/320 ADCLK

1: 17/256 ADCLK

ADCLK=0.5×XCLK. It is recommended to set AGC_FSEL[1:0]=00b for XCLK=16MHz.

• AGC7: AGC Control Register 7

Bit	7	6	5	4	3	2	1	0
Name	GAIN_STB[7:0]							
R/W	R/W							
Reset	0	0	1	1	0	0	0	0

Bit 7~0 **GAIN_STB[7:0]**: Gain stable count

Gain stable count delay in ADCLK period=GAIN_STB[7:0]×2

• FCF1: Filter Coefficient Control Register 1

Bit	7	6	5	4	3	2	1	0
Name	—	—	SFRATIO[1:0]		—	—	—	—
R/W	—	—	R/W		—	—	—	—
Reset	0	0	0	0	0	1	1	0

Bit 7~6 Reserved, must be “00”

Bit 5~4 **SFRATIO[1:0]**: Smooth filter ratio selection

00: 1/1

01: 1/16

10: 1/64

11: 1/128

Bit 3~0 Reserved, must be “0110”

• FCF2: Filter Coefficient Control Register 2

Bit	7	6	5	4	3	2	1	0
Name	FSCALE[7:0]							
R/W	R/W							
Reset	0	1	0	0	0	1	0	0

Bit 7~0 **FSCALE[7:0]**: Frequency deviation scale parameter low byte

• FCF3: Filter Coefficient Control Register 3

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	FSCALE[11:8]			
R/W	—	—	—	—	R/W			
Reset	0	0	0	0	0	1	0	0

Bit 7~4 Reserved, must be “0000”

Bit 3~0 **FSCALE[11:8]**: Frequency deviation scale parameter high byte

If the Data Rate is 100Kbps~250Kbps, then the FSCALE value can refer to the Lookup Table recommended settings.

If the Data Rate<100Kbps, then the FSCALE value is calculated as follows:

$$FSCALE[11:0] = \text{round}((h \times f_s / f_{XTAL} / (XODIV2 + 1)) \times 2^{15}),$$

where $h = (2 \times \text{frequency deviation}) / (\text{data symbol rate})$.

Here “h” is the modulation index calculated from frequency deviation and data symbol rate.

• FCF4: Filter Coefficient Control Register 4

Bit	7	6	5	4	3	2	1	0
Name	CF_B12[7:0]							
R/W	R/W							
Reset	1	0	0	0	0	1	0	1

• FCF5: Filter Coefficient Control Register 5

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_B12[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	1	0

• FCF6: Filter Coefficient Control Register 6

Bit	7	6	5	4	3	2	1	0
Name	CF_B13[7:0]							
R/W	R/W							
Reset	1	0	0	0	1	0	1	0

• FCF7: Filter Coefficient Control Register 7

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_B13[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	0	0

• FCF8: Filter Coefficient Control Register 8

Bit	7	6	5	4	3	2	1	0
Name	CF_A12[7:0]							
R/W	R/W							
Reset	0	0	0	1	0	0	1	0

• FCF9: Filter Coefficient Control Register 9

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_A12[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	0	0

When the data rate is in the range of 49Kbps~2Kbps, the following smooth filter is needed.

$$CF_A12[9:0]=\text{mod}(2^{10}+[(SFRATIO[1:0]-1)\times 2^8], 2^{10})$$

• FCF10: Filter Coefficient Control Register 10

Bit	7	6	5	4	3	2	1	0
Name	CF_A13[7:0]							
R/W	R/W							
Reset	0	0	1	0	1	0	1	1

• FCF11: Filter Coefficient Control Register 11

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_A13[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	1	1

• FCF12: Filter Coefficient Control Register 12

Bit	7	6	5	4	3	2	1	0
Name	CF_B22[7:0]							
R/W	R/W							
Reset	0	0	0	1	0	1	0	0

• FCF13: Filter Coefficient Control Register 13

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_B22[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	0	1

• FCF14: Filter Coefficient Control Register 14

Bit	7	6	5	4	3	2	1	0
Name	CF_B23[7:0]							
R/W	R/W							
Reset	0	0	1	0	0	0	0	1

• FCF15: Filter Coefficient Control Register 15

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_B23[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	0	0

• FCF16: Filter Coefficient Control Register 16

Bit	7	6	5	4	3	2	1	0
Name	CF_A22[7:0]							
R/W	R/W							
Reset	0	1	1	1	1	0	0	0

• FCF17: Filter Coefficient Control Register 17

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_A22[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	0	0

• FCF18: Filter Coefficient Control Register 18

Bit	7	6	5	4	3	2	1	0
Name	CF_A23[7:0]							
R/W	R/W							
Reset	0	0	1	0	1	0	0	0

• FCF19: Filter Coefficient Control Register 19

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_A23[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	0	0

The FCF4~FCF19 registers define eight groups of IIR coefficients, their recommended settings for different XTAL clock conditions are listed below.

f_{XTAL}	16MHz	16MHz	16MHz	16MHz	16MHz
f_s	250Kbps	125Kbps	50Kbps	10Kbps	2Kbps
f_d	93.75kHz	46.875kHz	18.75kHz	40kHz	8kHz
D_K[19:0] (H)	$f_{RF}/[f_{XTAL}/(XODIV2+1)]$, take decimal number				
D_N[6:0] (H)	$f_{RF}/[f_{XTAL}/(XODIV2+1)]$, take integer number				
SFRATIO[1:0] (D)	0	0	0	1	3
FSCALE[11:0] (H)	294	119	4C	A4	20
CF_B12[9:0] (H)	2CA	01D	0	0	0
CF_B13[9:0] (H)	062	346	0	0	0
CF_A12[9:0] (H)	358	022	0	310	302
CF_A13[9:0] (H)	3E9	331	0	0	0
CF_B22[9:0] (H)	3B3	386	0	0	0
CF_B23[9:0] (H)	03E	012	0	0	0
CF_A22[9:0] (H)	3E9	008	0	0	0
CF_A23[9:0] (H)	039	008	0	0	0

Bank 2 Control Registers

All control registers will be set to their initial value by power-on reset (POR). The software reset will set the control registers to their initial value.

Addr.	Name	Bit							
		7	6	5	4	3	2	1	0
26h	RSV1	Reserved							
27h	RSV2	Reserved							
28h	RSV3	Reserved							
29h	RSV4	Reserved							
2Dh	RSV5	Reserved							
2Eh	RSV6	Reserved							
2Fh	RVS7	Reserved							
30h	RSV8	Reserved							
31h	RSV9	Reserved							
34h	RSV10	Reserved							
3Ah	RSV11	Reserved							

Note: The addresses which are not listed in this table are reserved for future use, it is suggested not to change their initial values by any methods.

The recommended values for the Bank 2 registers are listed below:

Addr.	Name	Frequency Band	
		433MHz	868MHz
26h	RSV1	03h	
27h	RSV2	88h	
28h	RSV3	A3h	
29h	RSV4	80h	
2Dh	RSV5	16h	
2Eh	RSV6	64h	74h
2Fh	RSV7	44h/54h ($\geq 100\text{Kbps}$: 54h)	
30h	RSV8	00h	
31h	RSV9	64h	
34h	RSV10	BCh	9Ch
3Ah	RSV11	94h	

Special Function Description

Sub-1GHz RF Transceiver

The BC3602 adopts a fully-integrated, low-IF receiver architecture. The received RF signal is first amplified by a low noise amplifier (LNA), after which the frequency is down-converted to an intermediate frequency (IF) by a quadrature mixer. The mixer output is filtered by a channel-selected filter which rejects the unwanted out-of-band (OOB) interference and image signals. After filtering, the IF signal is amplified by an analog programmable gain amplifier (PGA). Then the IF signal is digitized by a 10-bit $\Sigma\Delta$ ADC.

The BC3602 features an Automatic Gain Control (AGC) unit to adjust the receiver gain according to the RSSI, generated at the digital modem. The AGC enables the BC3602 to operate from sensitivity level to +10dBm input power.

The BC3602 adopts a fully integrated fractional-N synthesizer which includes RF VCO, loop filter, digital controlled XO (DCXO) and integrated load capacitors for XO. Placing VCO load inductor on the PCB is to lower VCO resonant frequency to achieve 4.2mA RX mode current consumption. The fractional-N synthesizer architecture allows the users to extend their potential usage to a wider frequency range.

The transmit session is a VCO direct modulation architecture. Different from the conventional direct up-conversion transmitters, the GFSK modulation signal is fed into the VCO directly to take advantage of fractional-N synthesizer. As a result, both layout area and current consumption are much smaller compared with direct up-conversion transmitters. The fine resolution can generate a low FSK error GFSK signal. The modulated signal is fed into a Class-E Power Amplifier (PA) and the maximum output power can be up to +13dBm.

Serial Interface

The BC3602 communicates with a host MCU via a 3-wire SPI interface (CSN, SCK, SDIO) or a 4-wire SPI interface (SDO from GIO1 or GIO2) with a data rate up to 4Mbps. An SPI transmission is an $(8+8\times n)$ bits sequence which consists of an 8-bit command and $n\times 8$ bits of data, where n can be 0 or any natural number. If the number n is greater than the address boundary, the address will return to zero. The host MCU should pull the CSN (SPI chip select) pin low in order to access the BC3602. Using the SPI interface, user can access the control registers and issue Strobe commands. When writing data to the RF chip, the SPI data will be latched into the registers at the rising edge of the SCK signal. When reading data from the RF chip registers, the bit data will be transferred at the falling edge of the SCK signal after the target register address has been input.

Command (8 bits)								Data (8 bits)							
C7	C6	C5	C4	C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0

SPI Command Format

Two kinds of command are defined. One is 1-byte command only, named CmdO, and the other is 1-byte command followed by n -byte data, named CmdD.

C7	C6	C5	C4	C3	C2	C1	C0	Description	CmdO	CmdD
0	1	A5	A4	A3	A2	A1	A0	Write to control registers		√
1	1	A5	A4	A3	A2	A1	A0	Read from control registers		√
0	0	1	x	x	x	B1	B0	Set register bank	√	
0	0	0	1	x	x	x	0	Write SYNCWORD command		√
1	0	0	1	x	x	x	0	Read SYNCWORD command		√
0	0	0	1	x	x	x	1	TX FIFO write command		√
1	0	0	1	x	x	x	1	RX FIFO read command		√
1	0	0	1	1	1	1	1	Read Chip ID command		√
0	0	0	0	1	0	0	0	Software reset command	√	
0	0	0	0	1	0	0	1	TX FIFO address pointer reset command	√	
1	0	0	0	1	0	0	1	RX FIFO address pointer reset command	√	
0	0	0	0	1	0	1	0	Deep Sleep mode	√	
0	0	0	0	1	0	1	1	Idle mode	√	

C7	C6	C5	C4	C3	C2	C1	C0	Description	CmdO	CmdD
0	0	0	0	1	1	0	0	Light Sleep mode	√	
0	0	0	0	1	1	0	1	Standby mode	√	
0	0	0	0	1	1	1	0	TX mode	√	
1	0	0	0	1	1	1	0	RX mode	√	

A5~A0: The address of control registers.

x: Hardware doesn't care but it is recommended to set to 0 by software.

B1~B0: Bank number.

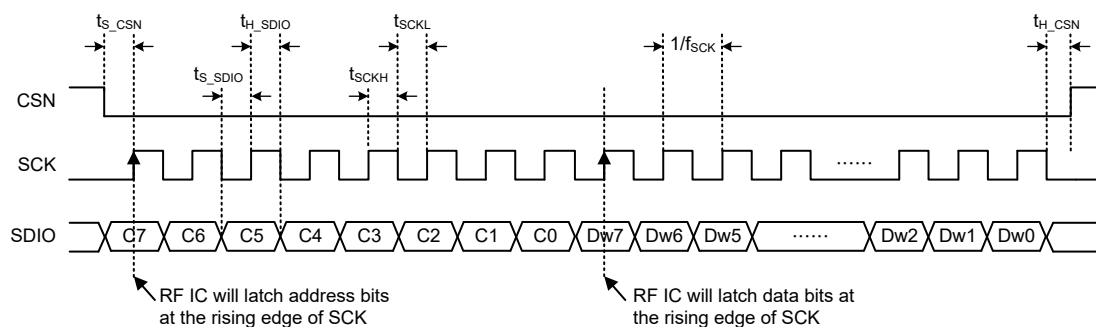
Note: 1. The chip supports multi-byte read/write operations and the address is increased automatically after each read or write operation.

2. Using software to read/write multiple bytes is allowed after one read/write command in a single CSN enabled cycle.

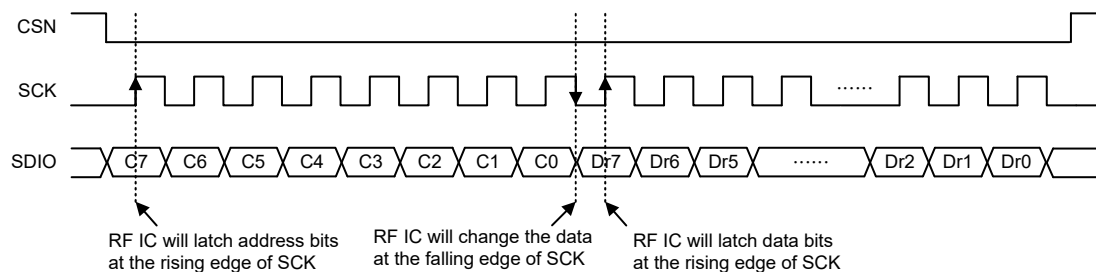
3. In the sleep mode, GIOs will keep the same level of the last operation mode.

4. Chip ID is a 2-byte data.

SPI Timing



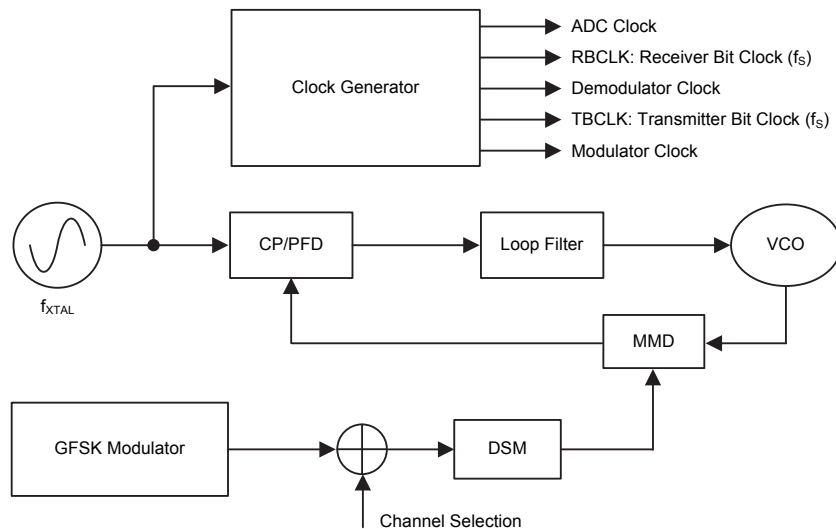
3-Wire SPI Interface Write 1-byte Data Operation



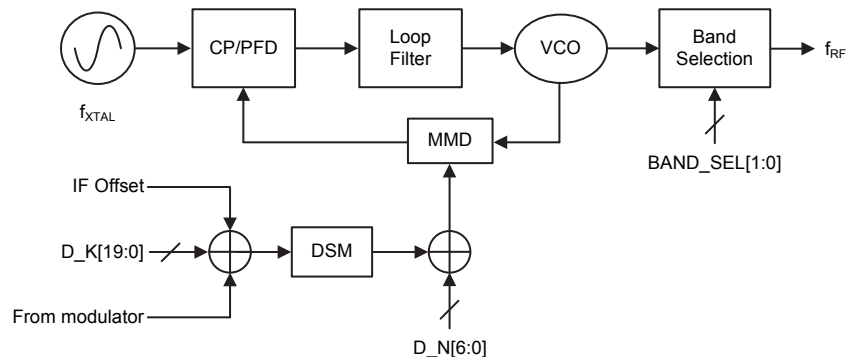
3-Wire SPI Interface Read 1-byte Data Operation

System Clock

The main system clock of the BC3602 comes from the X'tal oscillator. All internal operation clocks of various functional blocks are derived from the X'tal oscillator.



Frequency Synthesizer



The RF transceiver frequency is generated by a high resolution fractional-N Delta Sigma frequency synthesizer. By appropriate setting on the configuration parameters D_N[6:0] and D_K[19:0], a low-noise LO frequency can be generated to comply with various radio regulatory standards including ETSI EN, FCC, etc. In the RX mode, the synthesizer would generate an LO-IF frequency for the RX mixer operation, RXIFOS[11:0] is used to generate the required IF(Intermedia Frequency) offset. For data rate equal to or larger than 200Kbps, IF should be set to 300kHz, otherwise IF should be set to 200kHz. In the TX mode, there is extra input from the modulator to provide extra frequency deviation waveform of baseband data.

$$D_N[6:0]=\text{Floor}\left(\frac{f_{RF}}{f_{XTAL}/(XODIV2+1)}\right)$$

$$D_K[19:0]=\text{Floor}\left(\left(\frac{f_{RF}}{f_{XTAL}/(XODIV2+1)} - D_N[6:0]\right) \times 2^{20}\right)$$

$$RXIFOS[11:0]=\text{Floor}\left(\left(\frac{f_{IF}}{f_{XTAL}/(XODIV2+1)}\right) \times 2^{17}\right)$$

Modulator

The BC3602 supports GFSK modulation. A BT=0.5 Gaussian filter for pulse smoothing is implemented in the BC3602. The frequency deviation, f_{DEV} , of the transmitter is programmed using the FSCALE[11:0] field. The value of FSCALE[11:0] is determined by the modulation index h , the XO output divided by 2 control bit XODIV2, data rate f_s and f_{XTAL} .

$$h = \frac{2 \times f_{DEV}}{f_s}$$

$FSCALE[11:0] = \text{round} \left(\left(h \times \frac{f_s}{f_{XTAL} / (XODIV2 + 1)} \right) \times 2^{15} \right)$, take the least significant 12 bits

For low data rate applications ($\leq 10\text{Kbps}$), a modulation index of 8 is recommended. For high data rate applications ($\geq 50\text{Kbps}$), a modulation index of 0.75 is recommended. For applications where data rate is between the aforementioned boundaries, keeping the frequency deviation above 20kHz is recommended.

The FSCALE bit field needs to multiply a scaling factor for data rate equal to or larger than 100Kbps. The recommended FSCALE values for data rates equal to or larger than 100Kbps are provided in the filter coefficients tables following the Filter Coefficient Control Registers.

State Machine

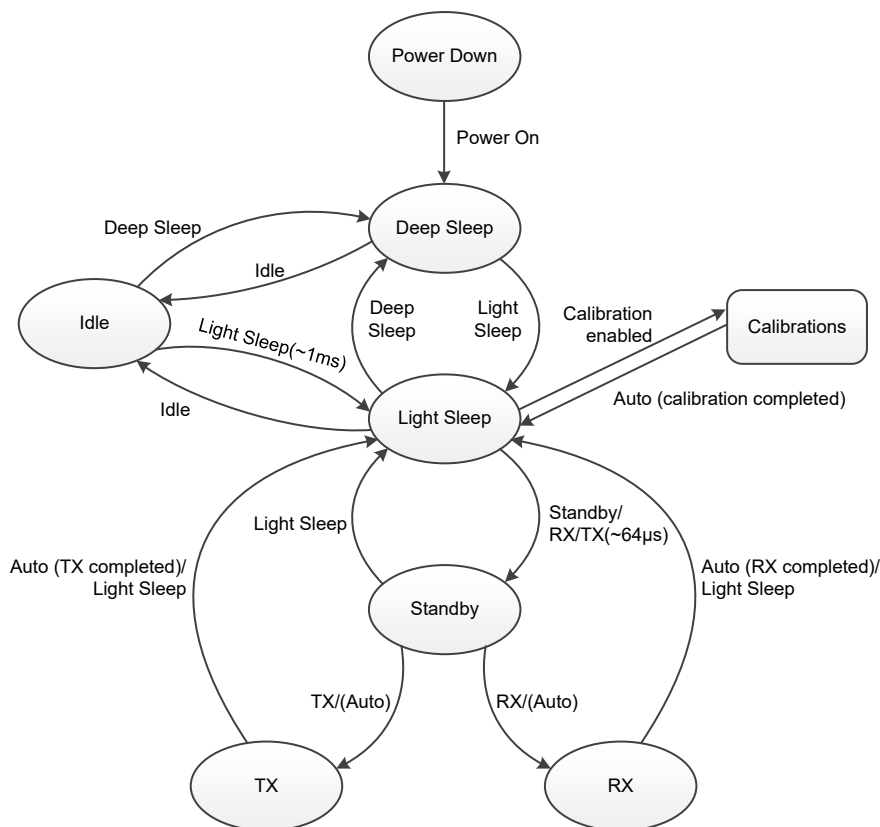
There are seven operating modes in the BC3602. The operation modes and key functions on/off state in the corresponding mode are listed below.

1. Power Down mode
2. Deep Sleep mode
3. Light Sleep mode
4. Standby mode
5. Idle mode
6. TX mode
7. RX mode

Mode	Register Retention	3.3V	LIRC	Regulator	XO	Standby+VCO	TX	RX	Strobe Command
Power Down	No	OFF	OFF	OFF	OFF	OFF	OFF	OFF	—
Deep Sleep	Yes	ON	OFF	OFF	OFF	OFF	OFF	OFF	0000_1010
Light Sleep	Yes	ON	OFF	ON	ON	OFF	OFF	OFF	0000_1100
Idle	Yes	ON	ON	OFF	OFF	OFF	OFF	OFF	0000_1011
Standby	Yes	ON	OFF	ON	ON	ON	OFF	OFF	0000_1101
TX	Yes	ON	OFF	ON	ON	ON	ON	OFF	0000_1110
RX	Yes	ON	OFF	ON	ON	ON	OFF	ON	1000_1110

TX/RX FIFO Mode (DIR_EN=0) State Machine

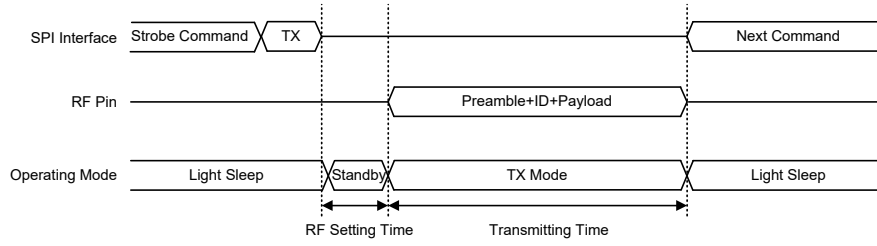
If the DIR_EN bit is cleared to 0, the device mode transactions are implemented by strobe command from the host MCU and the TX/RX data are derived from the packet handling hardware.



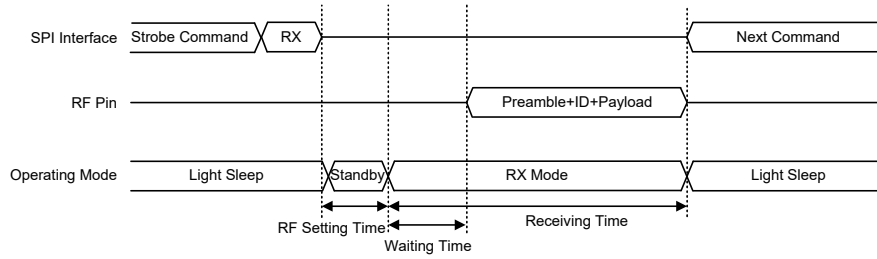
FIFO Mode State Diagram

Initially, the BC3602 is in the Power Down mode. After the device completes the internal power on reset, it will enter the Deep Sleep mode and wait for further strobe commands from the host MCU. If the Light Sleep command is received, the device will enable the internal LDO, oscillate the XO and enter the Light Sleep mode. In this state, the host MCU can have the BC3602 execute calibration process if necessary. For normal TRX operations, the host MCU can issue a RX or TX command to the BC3602. After receiving the TX or RX command, the device will first enter the Standby mode which lasts a certain period known as TX/RX settling time. After the settling time has elapsed, the device will finally enter the RX or TX mode. The device will stay in the TX/RX state until the TX/RX event is completed, after which the device will return to the Light Sleep mode automatically.

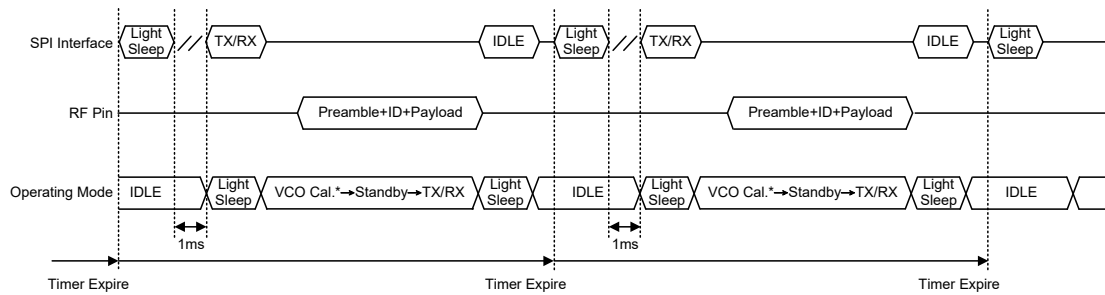
For low power periodical wireless transmission, the device supports low power Idle mode where the LIRC and wake-up timer are turned on. By appropriate timer setting and issuing the Idle mode command, the device will turn off the LDO and XO and enter the Idle mode. The device stays in the Idle mode until the timer expires and then an IRQ will be asserted on the GIO to wake-up the host MCU. Then the host MCU can have the device enter the Light Sleep mode and continue to execute normal TX/RX operations. After the TX/RX event is completed, the host MCU can issue the Idle command to have the device return to the Idle mode again.



TX Timing in FIFO Mode



RX Timing in FIFO Mode



Note: VCO Cal. (VCO Calibration) time: ~152µs@433MHz / ~96µs@868MHz.

Periodical TX/RX Timing

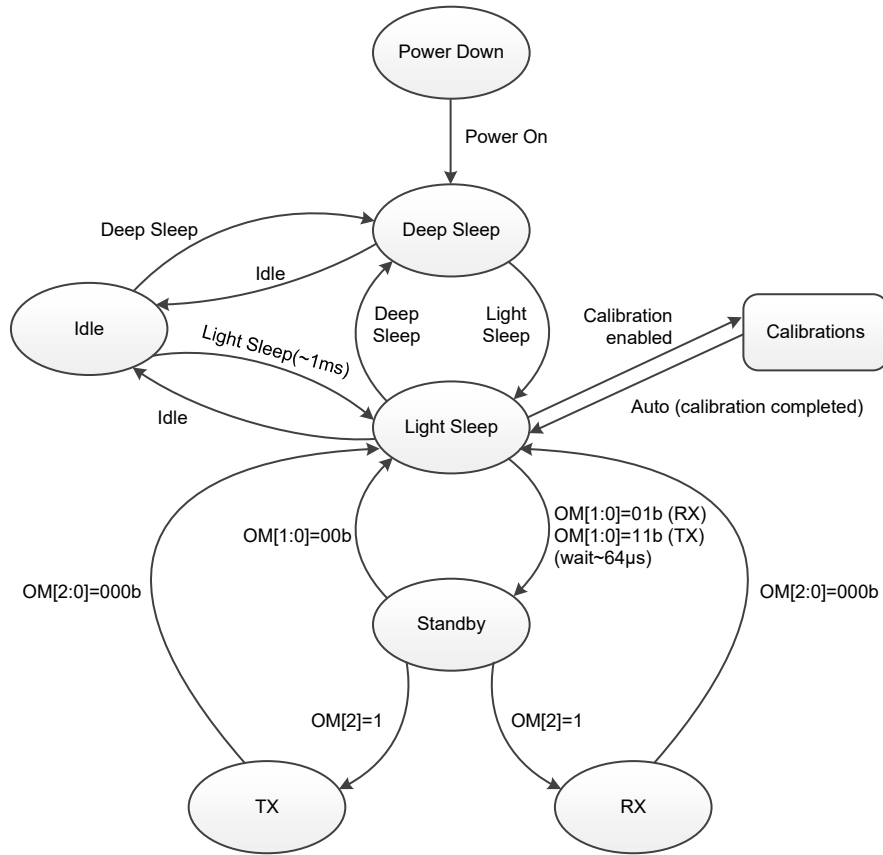
TX/RX Direct Mode (DIR_EN=1) State Machine

If the DIR_EN bit is set to 1, TX data is derived directly from the host MCU to BC3602 and RX data is sent directly from the BC3602 to the host MCU. In order to simplify the data bit clock synchronization between the BC3602 and the host MCU, the BC3602 outputs the TBCLK/RCLK from GIO3 or GIO4 by setting GIO3S[3:0] or GIO4S[3:0]. Both TBCLK and RBCLK are in 50/50 duty cycle. In the transmitting mode, the host MCU outputs bit data at the rising edge of the TBCLK signal and the BC3602 samples the TX bit data at the falling edge of the TBCLK signal. In the receiving mode, the host MCU receives data at the rising edge of the RBCLK signal and the BC3602 outputs bit data at the falling edge of the RBCLK signal. The host MCU can select GIO1 or GIO2 for the TX/RX bit data transmission by setting GIO1S[2:0] or GIO2S[2:0].

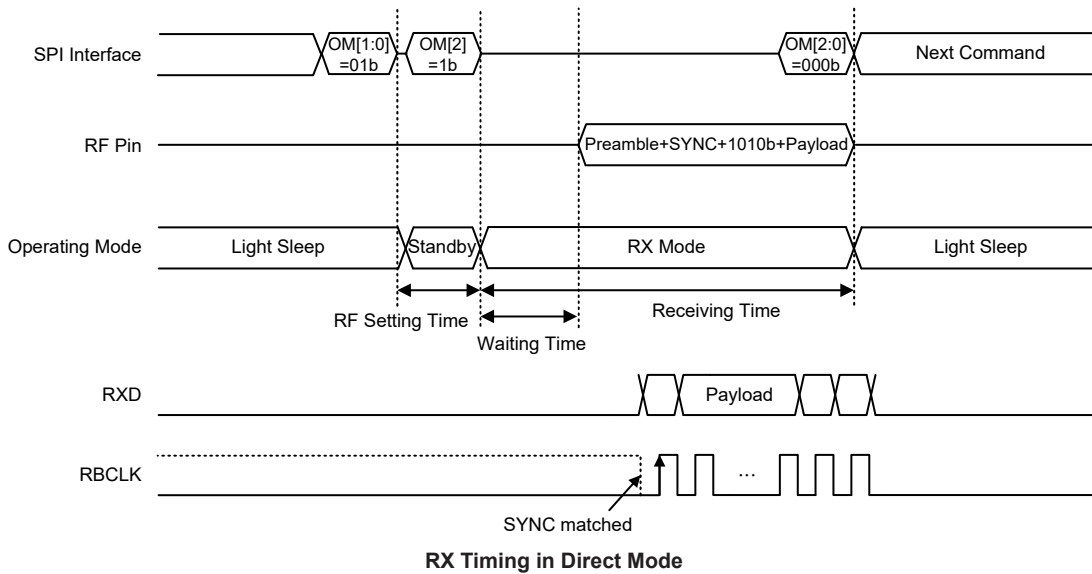
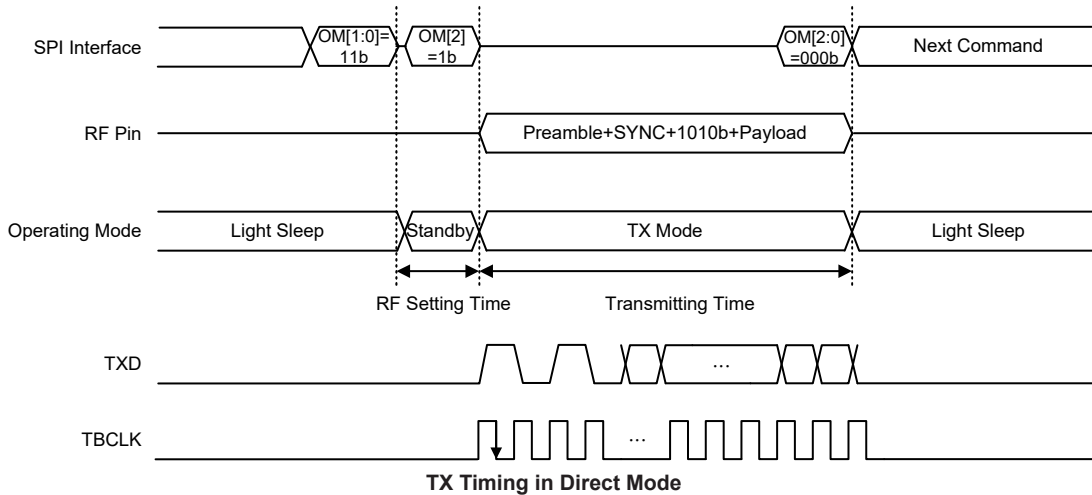
For TX operations in the direct mode, the host MCU needs to set the OM[1:0] bits, i.e. RTX_SEL and SX_EN, to 11b to select the TX mode and have the BC3602 enter standby mode first, then set the OM[2] bit, RTX_EN, to 1 to have the BC3602 start to transmit the TX data. As long as the host MCU sets OM[2:0] to 000b, the BC3602 will return to the Light Sleep mode.

For RX operations in the direct mode, the host MCU needs to set OM[1:0] to 01b first, then set OM[2] to 1 to have the BC3602 start to receive data from the air. After the BC3602 receives the matched SYNCWORD code, it will output the RBCLK clock, receive data bit (payload part) and then transmit to the host MCU.

In direct mode, the transmission data length has no limit.



Direct Mode State Diagram



Calibration

The device has three calibration functions, VCO, RC and LIRC calibrations, allowing users to auto select proper setting to compensate the PVT (Process-Voltage-Temperature) variation effect. The control bit, ACAL_EN, is used to enable the VCO and RC calibration functions at the same time and both calibration functions will be automatically implemented after this bit is set high. When the calibrations are completed, the ACAL_EN bit is cleared to zero by hardware. The host MCU can poll the ACAL_EN bit status or use the calibration complete interrupt flag CALCMPIF to check the calibration status. The device also has an independent enable bit, LIRCCAL_EN, for the LIRC calibration function, allowing to independently implementing the LIRC calibration function.

LIRC Calibration

There is an internal low frequency RC oscillator in the BC3602 providing a clock source for the wake-up timer in the Idle mode. After calibration, the internal low frequency RC oscillator supports a precision of $\pm 2\%$ for the PVT variation. The calibration process chooses the curve setting of LIRC frequency to an approximation of 32768Hz. Then an extra LIRC correction process is used to tune the wake-up timer accuracy error to be less than $\pm 1\%$.

The host MCU need to configure LIRC_OW=0 and LIRC_EN=1 before the LIRC calibration. Then the BC3602 will do LIRC calibration when LIRCCAL_EN is set to 1 by the host MCU during the Light Sleep mode. The LIRCCAL_EN bit is reset to 0 by hardware on the completion of LIRC calibration. The LIRC calibration process would take about 4ms.

AGC & RSSI

In order to enhance the receiving dynamic range and ensure the signal SNR be no less than the demodulator minimum SNR requirement, an AGC (Auto-Gain-Control) function block is embedded. The AGC would tune the receiver gain to get valid signal level before ADC staying between the set point and -26 dBFS. The set point is in the range of -6 dBFS to -12 dBFS which is adjusted by the SAT_SEL[1:0] bit field. FS is the full-scale of ADC.

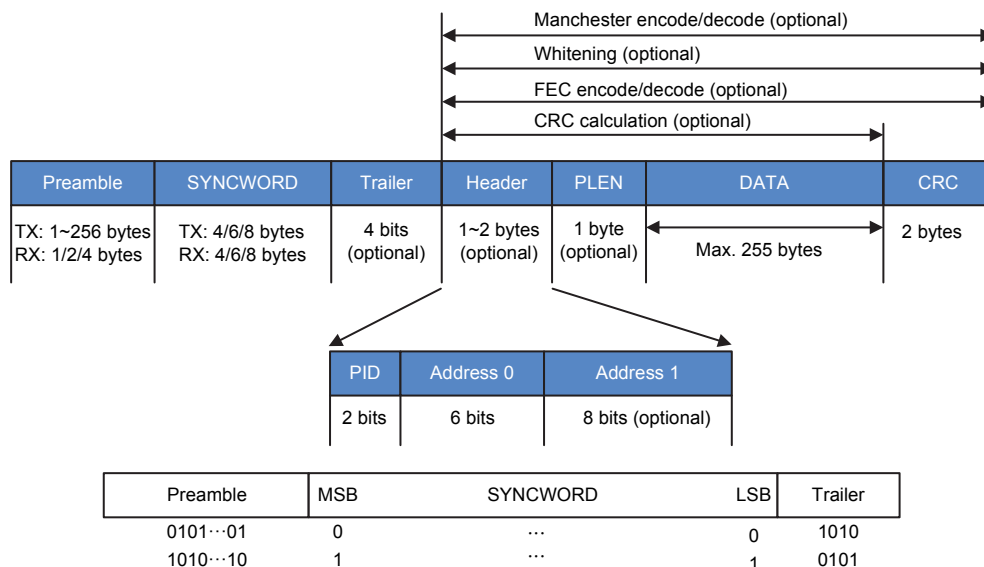
There is an integrated RSSI (Receiver Signal Strength Indicator) measurement function block in the BC3602. The RSSI calculation engine calculates the receiving signal strength after ADC. By combining the calculated ADC signal strength value and receiver chain total gain, the RSSI value is induced. The valid RSSI reading value is from -110dBm to -10dBm. The RSSI measurement error is normally below ±6dBm. The unit of the reading value is -dBm. Two RSSI reading values are available, one is RSSI_SYNC_OK[7:0] that is a RSSI measurement value snapshot when the valid SYNCWORD is detected OK, the other reading value is RSSI_NEGDB[7:0] that is a real time RSSI calculation result. In the receiving mode, the host MCU can access the RSSI_NEGDB bit field. After the receiving is completed, the host MCU should poll the RSSI_SYNC_OK[7:0] field for receiving signal strength assessment.

Packet Handler

In the TX mode, the packet handler is used to move the transmitting data out of FIFO and implement channel coding according to the packet format, then sends the packet to the modulator. In the RX mode, the packet handler is used to implement channel decoding with data from the demodulator and store the payload data into FIFO.

The packet handler performs several tasks such as Preamble and SYNCWORD insertion, Forward Error Correction, CRC calculation/checking, whitening/de-whitening and Manchester encode/decode.

Packet Format



Note: 1. Preamble format will follow SYNCWORD MSB to inverse.

If MSB=0, Preamble format=0101...01

If MSB=1, Preamble format=1010...10

2. Trailer format will follow SYNCWORD LSB to inverse.

If LSB=0, Trailer format=1010

If LSB=1, Trailer format=0101

3. The Trailer field contains 4 bits and is an optional field which is enabled by TRAILER_EN.

Preamble

The packet starts with a preamble with a length of 1~256 bytes set by TXPMLLEN[7:0] in the TX mode. In the RX mode, preamble detection length is limited to 1, 2 or 4 bytes selected by RXPMLLEN[1:0].

SYNCWORD

The SYNCWORD length which is set by SYNCLEN[1:0] can be 4, 6 or 8 bytes in the TX mode. In the RX mode, the detection length is also 4, 6 or 8 bytes. When the RX side receives a matched SYNCWORD packet, the DATA field will be stored in the FIFO.

Trailer

The trailer field length is fixed at 4 bits which is a concatenating field between SYNCWORD and the latter payload.

Header

The header (Payload Header) is optional and enabled by PLH_EN. The payload header length can be 1 or 2 bytes set by PLHLEN. When the PLHLEN bit is 0, only PID[1:0] and PLHA[5:0] (address 0) fields are used in the packet. PID[1:0] is located in bit 7~6 of the payload header field. If PLHAC_EN=0, PLHA[5:0] can be used as software flags and the actual function can be defined by users. If PLHAC_EN=1, the device will compare the local PLHA[5:0] field with the received PLHA[5:0] field. If matched, the receiving data will be moved into the RX FIFO, otherwise the following incoming data will be abandoned. The PLHA[5:0] field is used to support broadcast function and PLHA[5:0]=0 is a special preserved address permitting the BC3602 not to implement the address filtering mechanism.

When the PLHLEN bit is set to 1, the address field length is extended to 14 bits which is formed by address 0 (PLHA[5:0]) and address 1 (PLHEA[7:0]).

PLEN (Payload Length)

The PLEN field is optional and its length is fixed at 1 byte once being enabled by PLEN_EN. When this bit is set high, the DATA field length is variable and is determined by the PLEN field in each TX/RX packet.

DATA

When in the TX mode, the TX data length is determined by the TXDLEN[7:0] field. The maximum length is 255 bytes in the extend FIFO mode. In the special case of infinite FIFO mode, the length can exceed 255 with an infinite length. If PLEN_EN=1, the PLEN field in the TX packet is enabled and the PLEN content is equal to TXDLEN[7:0]. When in the RX mode, the RX data length is set by RXDLEN[7:0] if PLEN_EN=0 and by PLEN field in the receiving packet if PLEN_EN=1.

CRC

The CRC field is optional and is enabled by CRC_EN. It is recommend to always set CRC_EN to 1 for data correctness checking. There are two CRC formulas selected by setting the CRCFMT bit.

$$\text{CRCFMT}=0: \text{CCITT-16-CRC } G(X) = X^{16} + X^{12} + X^5 + 1$$

$$\text{CRCFMT}=1: \text{IBC-16-CRC } G(X) = X^{16} + X^{15} + X^2 + 1$$

Note that the CRC initial value is FFFF.

FEC

The optional data encode/decode function can be enabled by FEC_EN. Use (7,4) Hamming code to correct 1-bit error and more than 1-bit error detect for each 4-bit data. After FEC, the data length for each data will be $(4+3) \times 2 = 14$ bits.

• Hamming Code Function Table

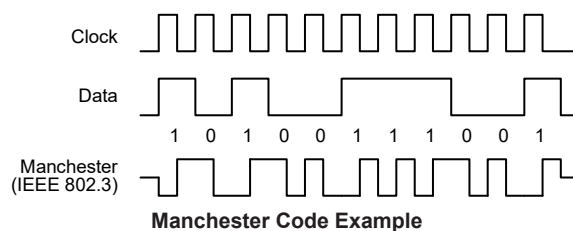
Bit	7	6	5	4	3	2	1
Transmitted Bit	D3	D2	D1	P2	D0	P1	P0
P0	Y	N	Y	N	Y	N	Y
P1	Y	Y	N	N	Y	Y	N
P2	Y	Y	Y	Y	N	N	N

Data Whitening

The optional data whitening/de-whitening function can be enabled by WHT_EN. Use PN7 code to implement XOR operation with the transmitted data. The whitening seed is set by WHTSD[6:0].

Manchester Code

The optional Manchester encode/decode function can be enabled by MCH_EN. Each bit after Manchester encoding will be extended into two bits and recovered to one bit data after decoding.



FIFO Operation Modes

In Burst mode, data transmission to the RF transmitter is derived from FIFO and is pre-written by the host MCU. There are 4 FIFO modes to support various applications. They are the Simple FIFO mode, Block FIFO mode, Extend FIFO mode and Infinite FIFO mode.

FIFO Reset

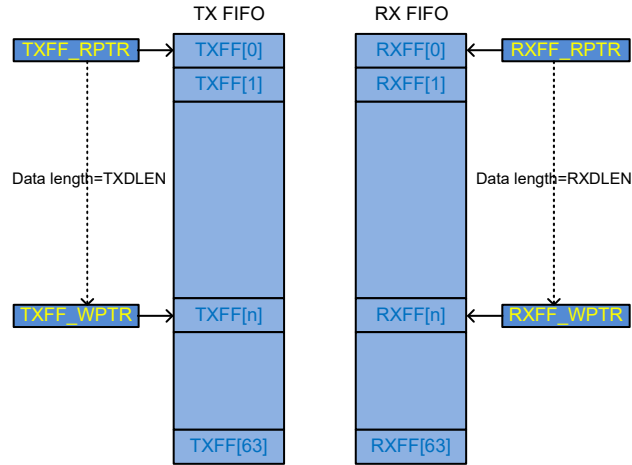
To use the FIFO in the burst mode, issue the TX FIFO address pointer reset command and RX FIFO address pointer reset command to reset the FIFO pointer and buffer first. After this, the FIFO is in the initial state same as reset.

Simple FIFO Mode

This FIFO mode is used for general applications with a TX/RX data length less than or equal to 64 bytes. The data length should not exceed 64 bytes. To use the simple FIFO mode, the host MCU must write the transmitting data to FIFO by the SPI write FIFO command. The transmitting sequence is first written byte first out and the MSB in each byte first out to the transmitter. Users should determine all transmitting data packet format including the preamble, SYNCWORD and packet encoding such as FEC, CRC, whitening. After FIFO data filling out is completed, clear the TXFFSA[5:0] field and set TXDLEN[7:0]/RXDLEN[7:0] field to the desired transmitting/receiving length in bytes. Then issue the TX command to start the transmission. After the current transmitting is completed, the data will be kept in FIFO to wait for the next transmission.

Programming procedure:

1. Reset TX FIFO by the SPI reset TX FIFO command.
2. Reset RX FIFO by the SPI reset RX FIFO command.
3. TXFFSA[5:0] must be cleared to 0.
4. Fill out TX FIFO by the SPI write FIFO command.
5. Set TXDLEN[7:0]/RXDLEN[7:0] to control the TX/RX length in bytes.
6. Issue the TX command for transmitter and RX command for receiver.
7. TX/RX completion is acknowledged by the TX/RX complete IRQ.
8. Re-transmitting TX packet with the same data will auto-reset TXFF_RPTR to 0.

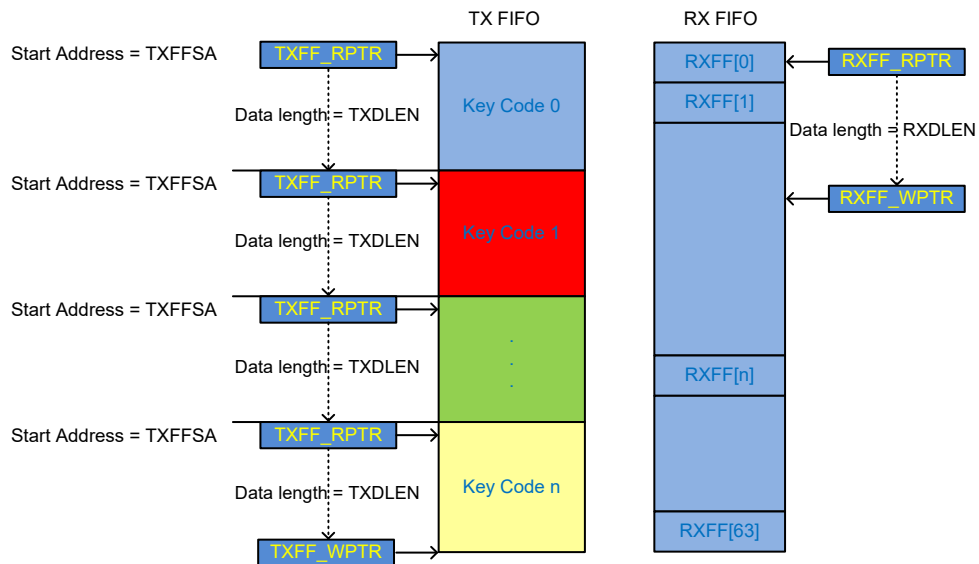


Block FIFO Mode

The Block FIFO mode is used to support multi-key code applications. Users should write all the key codes to FIFO first. When a key is pressed, the host MCU will detect the key and set TXFFSA[5:0] to the target key code start address and set TXDLEN[7:0] to indicate the key code length and issue the TX strobe command to start the transmission. The maximum FIFO length is also limited to 64 bytes.

Programming procedure:

1. TX: Write key code 0~n to TX FIFO by SPI write FIFO command.
2. TX: Set TXDLEN[7:0] for key code length.
3. TX: When a key is pressed, the host MCU will set TXFFSA[5:0] to the start address of the corresponding key code.
4. RX: Set the RXDLEN[7:0] to key code length and then enter the RX mode by SPI command.
5. TX: Issue TX command for transmitter.
6. RX: Issue RX command for receiver.
7. TX/RX completion is acknowledged by the TX/RX complete IRQ.



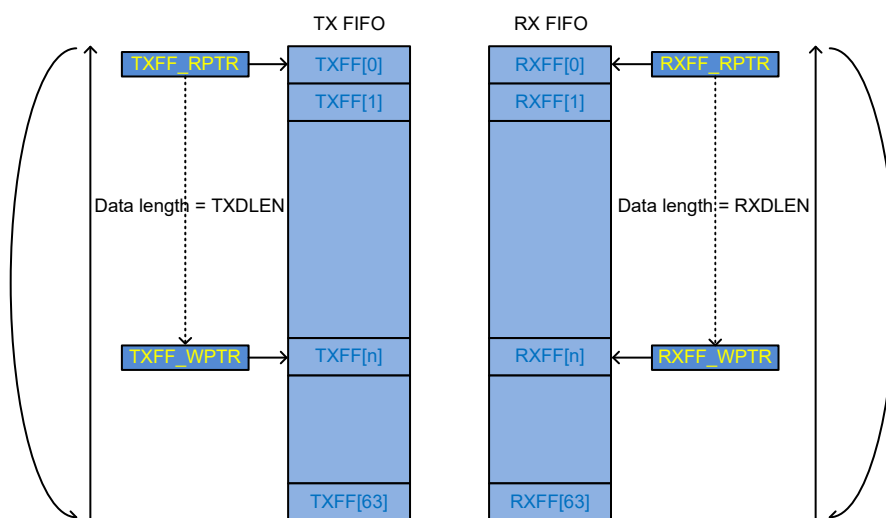
Extend FIFO Mode

The Extend FIFO mode is used for transmissions with a long payload data packet. The maximum length is 255 bytes. As the physical FIFO length is 64 bytes, to extend the available transmitting length in one packet, a handshake mechanism is needed between the host MCU and the FIFO controller.

Set FFMG[1:0] to determine the FIFO data length margin and set FFMG_EN to enable the margin detect function to inform the MCU when the TX FIFO data fullness level is less than the margin. The MCU should write data to TX FIFO fast enough when receiving this reminding signal to avoid transmission being terminated by TX FIFO underflow.

Programming procedure:

1. Set FFMG_EN to enable FIFO depth low threshold detect function and set FFMG[1:0] to select the threshold, 4, 8, 16 or 32 bytes.
2. Set the FIFOLTIE bit to 1 to enable the FIFO low threshold IRQ.
3. Set GIO_nS field (n=1~4) = 101b to output IRQ on GIO1~GIO4.
4. TX: If MCU detects the FIFO low threshold IRQ signal, it will move data into TX FIFO with a data length less than or equal to (64-FFMG[1:0]). Then the MCU clears the FIFO low threshold IRQ flag FIFOLTIF and repeats the same routine until all TX data are completely written to TX FIFO.
5. RX: If MCU detects the FIFO low threshold IRQ signal, it will read data from RX FIFO with a data length equal to FFMG[1:0]. Then the MCU clears the FIFO low threshold IRQ flag FIFOLTIF and repeats the same routine until receiving the RX completion IRQ to read the remaining data from RX FIFO.



Infinite FIFO Mode

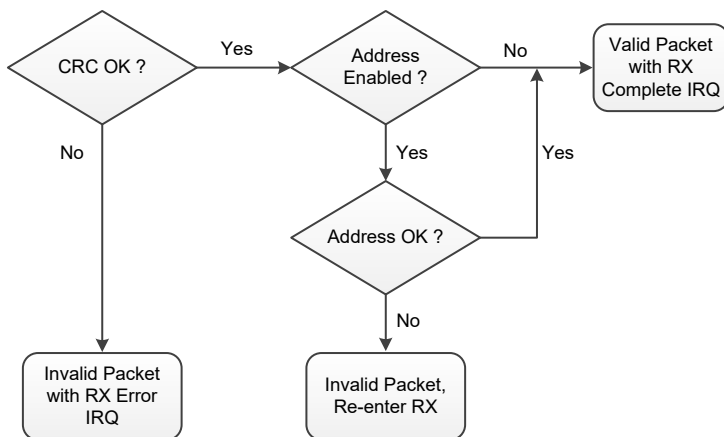
Programming procedure:

1. Set FFINF_EN to 1 to enable the Infinite FIFO mode.
2. The handshaking and IRQ function are identical with the Extend FIFO mode.
3. TX: If receiving the FIFO low threshold IRQ, the MCU continues to write TX data to TX FIFO with a data length less than or equal to (64-FFMG[1:0]). Then the MCU clears the FIFO low threshold IRQ flag and repeats the same routine until it wants to terminate the infinite FIFO mode. To terminate the infinite FIFO mode, after receiving IRQ and moving data to TX FIFO, the MCU should clear FFINF_EN to zero and set TXDLEN[7:0] to the remaining data length if the remaining transmitting length is less than 192 bytes and longer than 64 bytes. The terminating configuration should be programmed only once for one transmission. The packet will be terminated when all of the target data are transmitted completely.

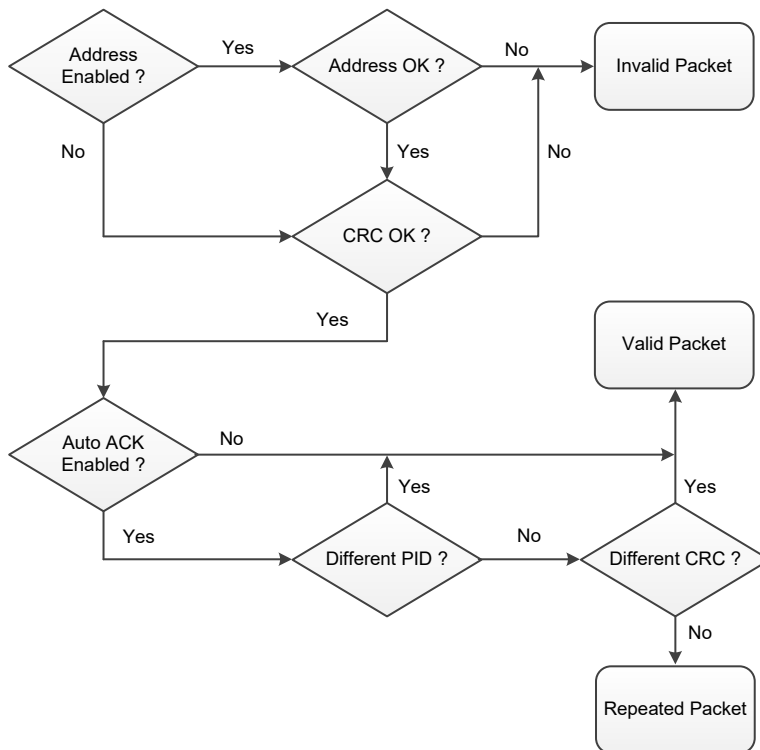
4. RX: If receiving the FIFO low threshold IRQ, the MCU reads data from RX FIFO with a data length equal to FFMG[1:0]. Then the MCU clears the FIFO low threshold IRQ flag and repeats the same routine until it wants to terminate the infinite FIFO mode. To terminate the infinite FIFO mode, after receiving IRQ and reading data from RX FIFO, the MCU should clear FFINF_EN to zero and set RXDLEN[7:0] to the remaining data length if the remaining receiving length is less than 192 bytes and longer than 64 bytes. The terminating configuration should be programmed only once for one reception. The packet will be terminated when all of the target data are received completely.

Receiving Packet Judgement

In normal RX operating mode, package reception follows the following judgement criteria.

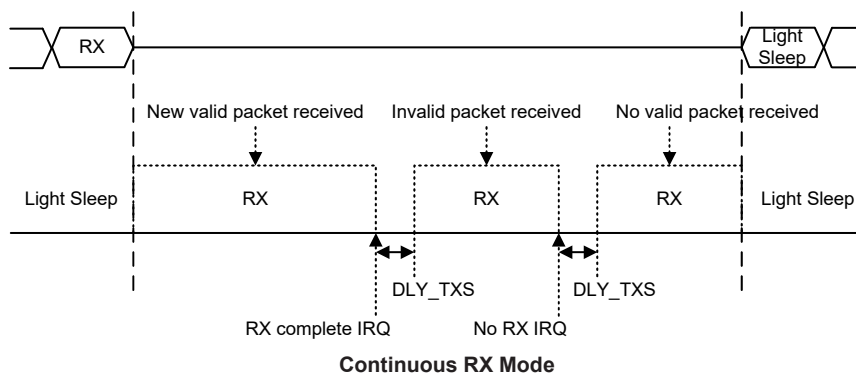


The BC3602 adopts extra receiver packet judgment for the continuous RX mode and auto-acknowledge mode. The main purpose of these special link layer functions are used to alleviate MCU loading when handling TRX packet transaction.



Continuous RX Mode

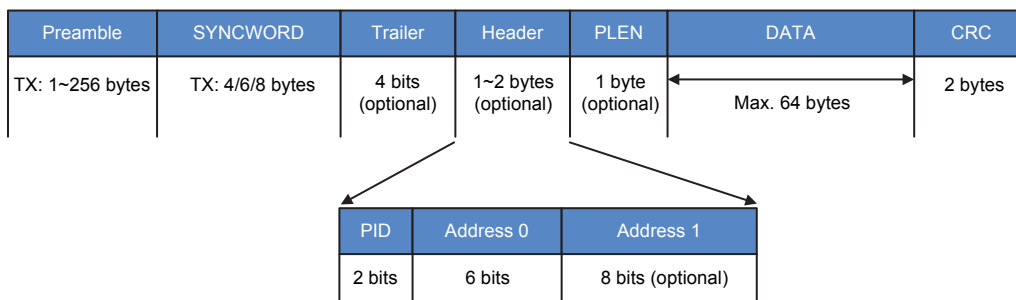
There is a special continuous RX operating mode supported in the BC3602. The MCU can enable this continuous RX mode by setting the RXCON_EN bit high and start the continuous RX mode by issuing the RX strobe command to the device. If there is a valid RX packet received, the BC3602 will issue a RX completion IRQ to the MCU. The device then repeats the RX operation after a duration defined by DLY_TXS[2:0] to keep listening for incoming packets. If an invalid packet is received, the BC3602 would only repeat the RX operation without issuing the RX completion IRQ to the MCU. The MCU stops the continuous RX by issuing the Light Sleep command to the BC3602. In the continuous RX mode, only simple FIFO mode can be used. In order to prevent the receiving packet data length field from being corrupted by new incoming packets before the MCU reads data from RX FIFO, users should set RXPL2F_EN=1 and PLEN_EN=1 to have the PLEN information stored into the RX FIFO. Because of the existence of PLEN byte, the maximum packet data length becomes 63 bytes. If a new incoming packet arrives before the MCU reads RX FIFO, a FIFO overflow error will happen, in which condition the BC3602 will issue a RX error IRQ to the MCU. At this moment, the MCU should exit the continuous RX mode and reset the RX FIFO pointer.



ARK Mode: Auto-Resend and Auto-Ack

The BC3602 supports auto-resend and auto-ack mechanism by setting the ARK_EN bit high. This mechanism enables an easy two-way communication implementation however can only be operated in the simple FIFO mode.

Set ARK_EN to 1 to enable the device to enter the auto-resend and auto-ack ready mode. Then, auto-resend is triggered by the TX strobe command from the MCU and auto-ack is triggered by RX strobe command from the MCU. Packet format transmitted from the master to the slave in the auto-resend mode are illustrated below.



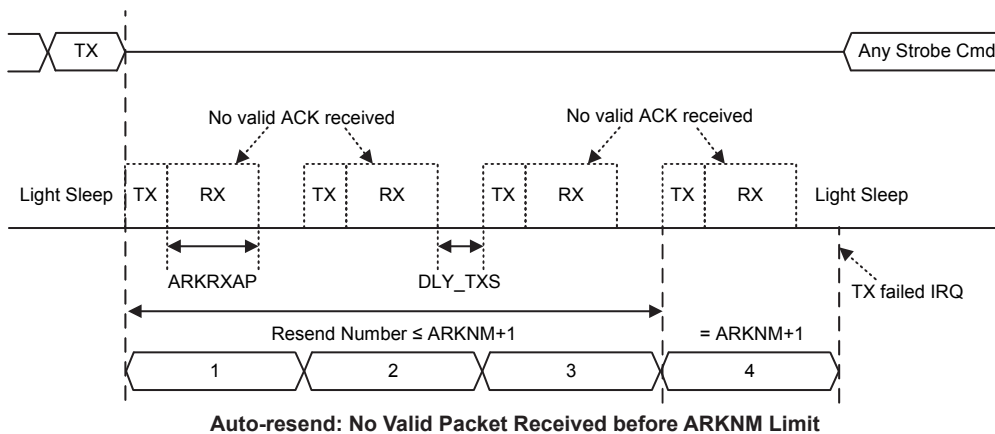
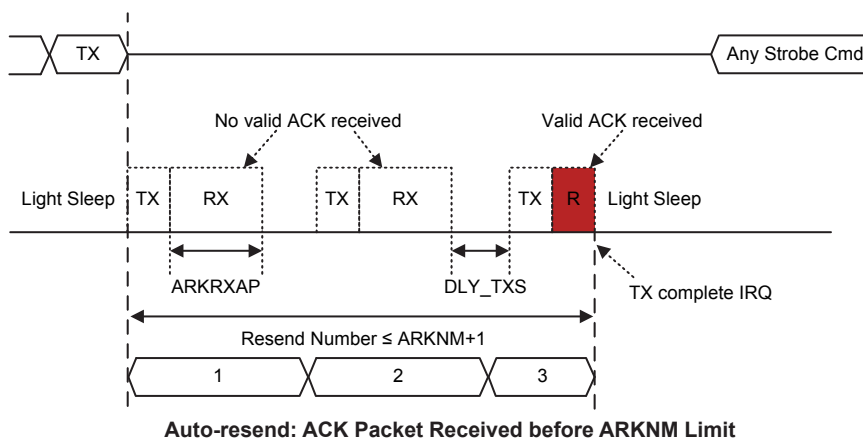
The slave side in the auto_ack mode uses the packet format as the following to be an acknowledge packet transmitted to master. Note that there is no payload data field used in the acknowledge packet.

Preamble	SYNCWORD	Trailer	Header	PLEN	CRC
TX: 1~256 bytes	TX: 4/6/8 bytes	4 bits (optional)	1~2 bytes (optional)	1 byte (optional)	2 bytes

PID	Address 0	Address 1
2 bits	6 bits	8 bits (optional)

If the address field is used for the ARK mode, the auto-resend (master) side should configure the same address as the auto-ack (slave) side.

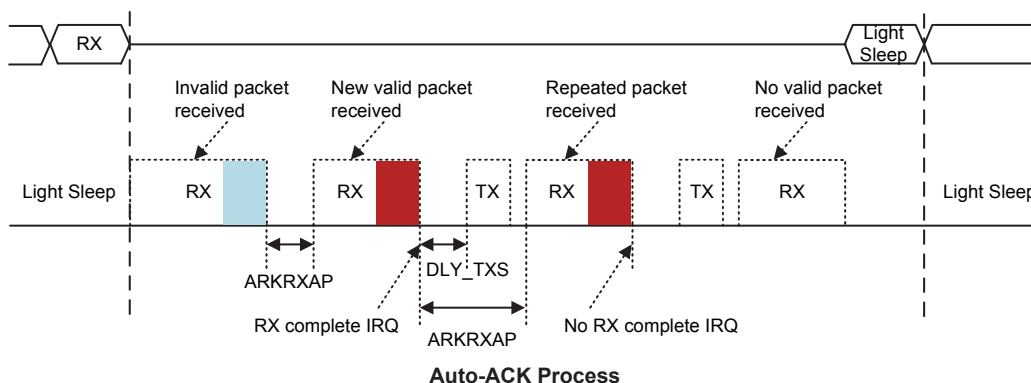
After configuring ARKNM[3:0], ARK_EN and ARKRXP[7:0], the MCU starts the auto-resend process by issuing the TX strobe command. The BC3602 starts to transmit data from the TX FIFO and then enters the RX mode after the TX completion. The RX period is in multiples of 250µs which is determined by ARKRXP[7:0] plusing one. If the BC3602 receives a valid acknowledge packet from the slave side within the RX period with CRC checked correct, it will return to the Light Sleep mode and issue a TX completion IRQ to the MCU. Otherwise, the BC3602 will check if the resend number has reached the limit set by ARKNM[3:0], if not, it will go to the TX mode to transmit the same TX data from the TX FIFO and the resend number will be increased by one.



Regarding the auto-ack in the slave side, the MCU issues the RX strobe command to start the auto-ack process and issues the Light Sleep strobe command to stop the auto-ack process. In the auto-ack mode, an extra PID/CRC filtering function will be applied for the slave side to check the packet received. If the PID/CRC of the new incoming packet is same as the stored PID/CRC of the last packet, then the newly received packet would be treated as a repeated packet.

During the auto-ack process, if the device receives a valid packet with different PID/CRC and CRC/address checked correct, it will issue a RX completion IRQ to the MCU and auto-transmit the ACK packet to the master. If the device receives a packet with the same PID/CRC and CRC/address checked correct, it will treat this packet as the repeated packet. Then the device will not issue the RX IRQ to the MCU but still auto-transmit the ACK packet to the master. If the device receives a packet with CRC/address checked failed, no IRQ is issued and the device will automatically re-do the RX operation to continually listening for incoming packets.

The gap period for the device to restart the next RX operation after the current RX completion is defined by ARKRXAP[7:0]. In general cases, the MCU should fetch the receiver FIFO data within this period after receiving the RX completion IRQ. Besides, the MCU needs to wait for a same duration if it wants to leave the ARK mode after receiving the RX completion IRQ.



ATR Mode: Auto-Transmit-Receive

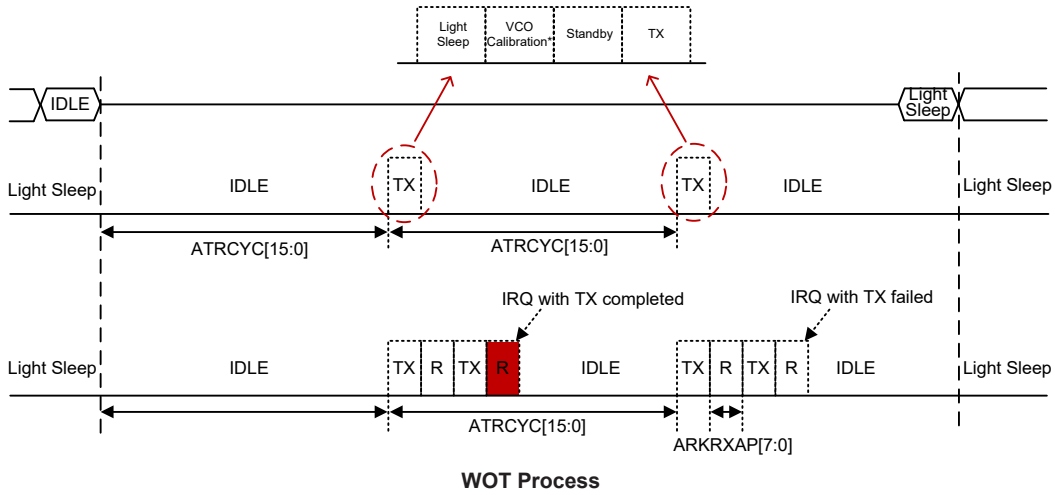
There is a special ATR operation mode in the BC3602 to reduce the external host's loading. Two ATR functions are implemented within the device, one is WOR (Wake-On-RX) and the other is WOT (Wake-On-TX). They can only be operated with simple FIFO mode. These two operating modes need to co-work with an Idle mode timer which operates at a low frequency. The low frequency clock can be sourced from the internal LIRC or from the external ROSCi clock by setting the ATRCLKS bit in the ATR1 register. There are two operation modes for the ATRCT timer which is selected using the ATRCTM bit. Clearing the ATRCTM bit to 0 will select the single mode, where the ATRCT timer will restart upon every ATR transaction when entering the Idle state. The ATRCT timer will stop and leave the ATR mode upon receiving the Light Sleep command. Setting the ATRCTM bit to 1 will select the continuous mode, where the ATRCT timer will start to operate upon receiving the Idle command and continuously run until the ATR_EN bit or the ATRCTM bit is cleared to zero.

After entering the ATR mode, only the Idle, Light Sleep, Set Register Bank and control register read/write commands can be recognized by the BC3602.

WOT (Wake-On-TX) Function

When the WOT function is enabled by setting the ATR_EN bit to 1 and the ATRM[1:0] bits to 00b, the device will periodically wake-up from the Idle mode and transmit TX FIFO contents without interaction with the host MCU. The device starts the WOT process upon receiving the Idle strobe command from the MCU and stops the WOT process upon receiving the Light Sleep strobe command from the MCU. The ATRCYC[15:0] bits are used to set the wake-up period for the WOT function. At the moment of timer expiration, the wake-up timer will trigger the device to leave the Idle state and enter the active state to transmit data, at the same time the ATRCYC[15:0] content will be reloaded into the timer's counter. After finishing the TX operation, the device will return to the Idle mode and stay in this state until next wake-up timer expiration occurs. In the active state, the device only implements wake-up transmission once by default. Users can extend the wake-up transmitting mechanism by combining with the ARK function. The repeated transmitting number is controlled by the ARKNM[3:0] bits in the ATR7 register. The time duration between the repeated transmitting packets is inserted with one RX slot and controlled by ARKRXAP[7:0] in the ATR8 register. If the device receives ACK in the RX slot, a TX completion IRQ will be issued to inform the host MCU.

Note: 1. VCO Calibration time: ~152µs@433MHz / ~96µs@868MHz
 2. Both new TX and RX need to first go through "Light Sleep→VCO Cal.→Standby"



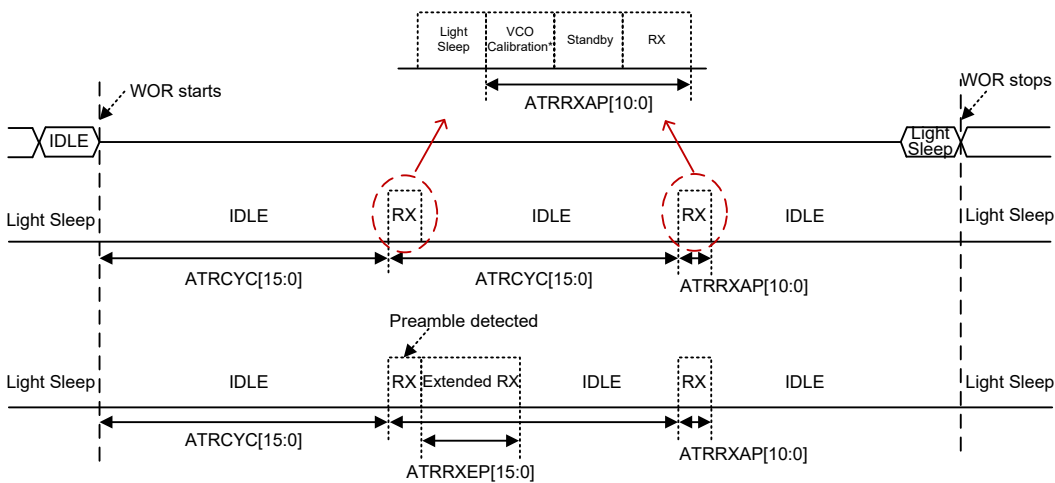
WOT Process

WOR (Wake-On-RX) Function

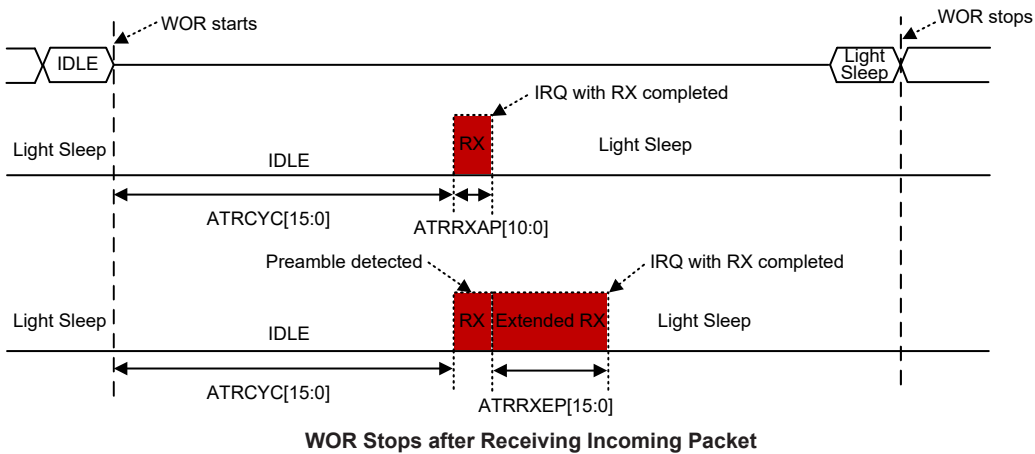
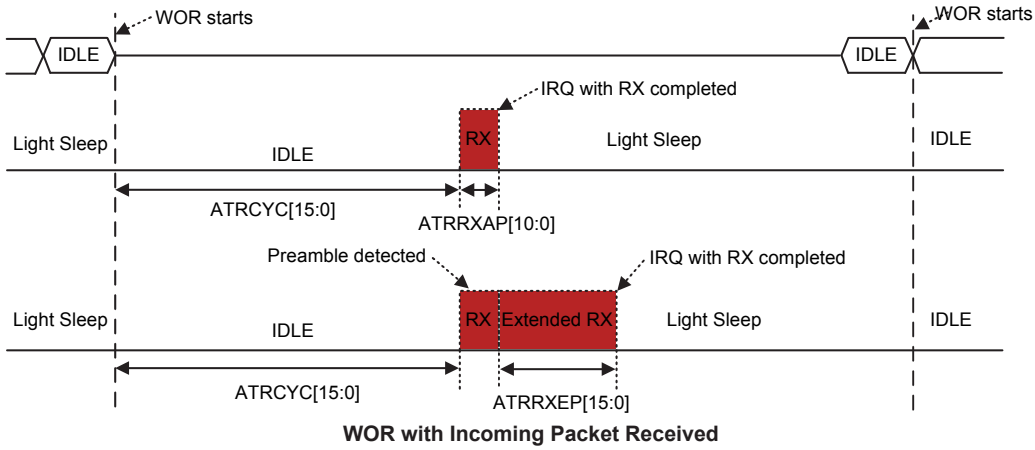
When the WOR function is enabled by setting the ATR_EN bit to 1 and the ATRM[1:0] bits to 01b, the device will periodically wake-up from the Idle mode and listen for the incoming packets without interaction with the host MCU. The device starts the WOR process upon receiving the Idle strobe command from the MCU and stops the WOR process upon receiving the Light Sleep strobe command from the MCU. The ATRCYC[15:0] bits are used to set the wake-up period for the WOR function. At the moment of ATR timer expiration, the wake-up timer will trigger the device to leave the Idle mode and enter the active state to listen for the incoming packet, at the same time the ATRCYC[15:0] content will be reloaded into the timer's counter. The receiving active period is defined by the ATRRXAP[10:0] bits. The active period is in multiples of 250µs and starts from 250µs. If there is no incoming packet received in the RX active period, the device will return to the Idle mode and wait for the next WOR cycle.

The active period is auto-extended when the preamble is detected. The extend period is defined by ATRRXEP[15:0]. The extend period is also in multiples of 250µs and starts from 250µs. Once the SYNCWORD is received, the receiving period would be auto-extended until the whole packet is completely received. After the RX receiving is done with CRC checked correct, the BC3602 would acknowledge the MCU with RX complete IRQ and stay at light sleep mode. MCU can read the incoming packet from the RX FIFO and then restart the next WOR session by issuing Idle strobe command. If MCU want to leave WOR mode, MCU still need to issue light sleep command to the BC3602.

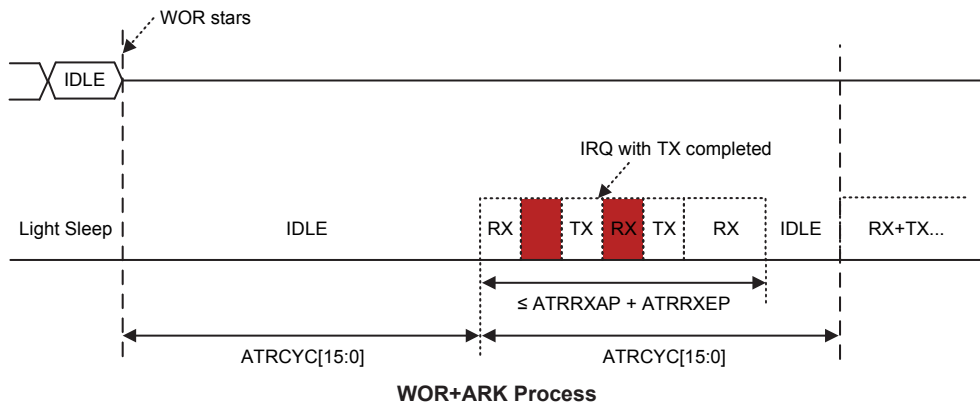
Note: 1. VCO Calibration time: ~152µs@433MHz / ~96µs@868MHz
 2. Both new RX and TX need to first go through "Light Sleep→VCO Cal.→Standby"



WOR without Incoming Packet Received



In the WOR active period, the device only implements RX operation once by default. Users can extend the wake-up receiving mechanism by combining with the ARK function. In WOR+ARK mode, the time duration between the repeated receiving packets is inserted with one TX slot for acknowledgement. The TX duration depends on the transmitting data rate. The device stays in the RX mode for a maximum period of time defined by $ATRRXAP + ATRRXEP$. If a valid incoming packet, with CRC checked OK and a different PID/CRC, is received before the timer expires, the device will issue a RX completion IRQ to the MCU and automatically enter the TX mode. If a repeated packet, with CRC checked correct and a same PID/CRC, is received, the device will automatically enter the TX mode with no IRQ to the MCU. After the TX completion, the device will return to the RX mode again and listen for the incoming packets until the timer expires if no incoming packet is received.

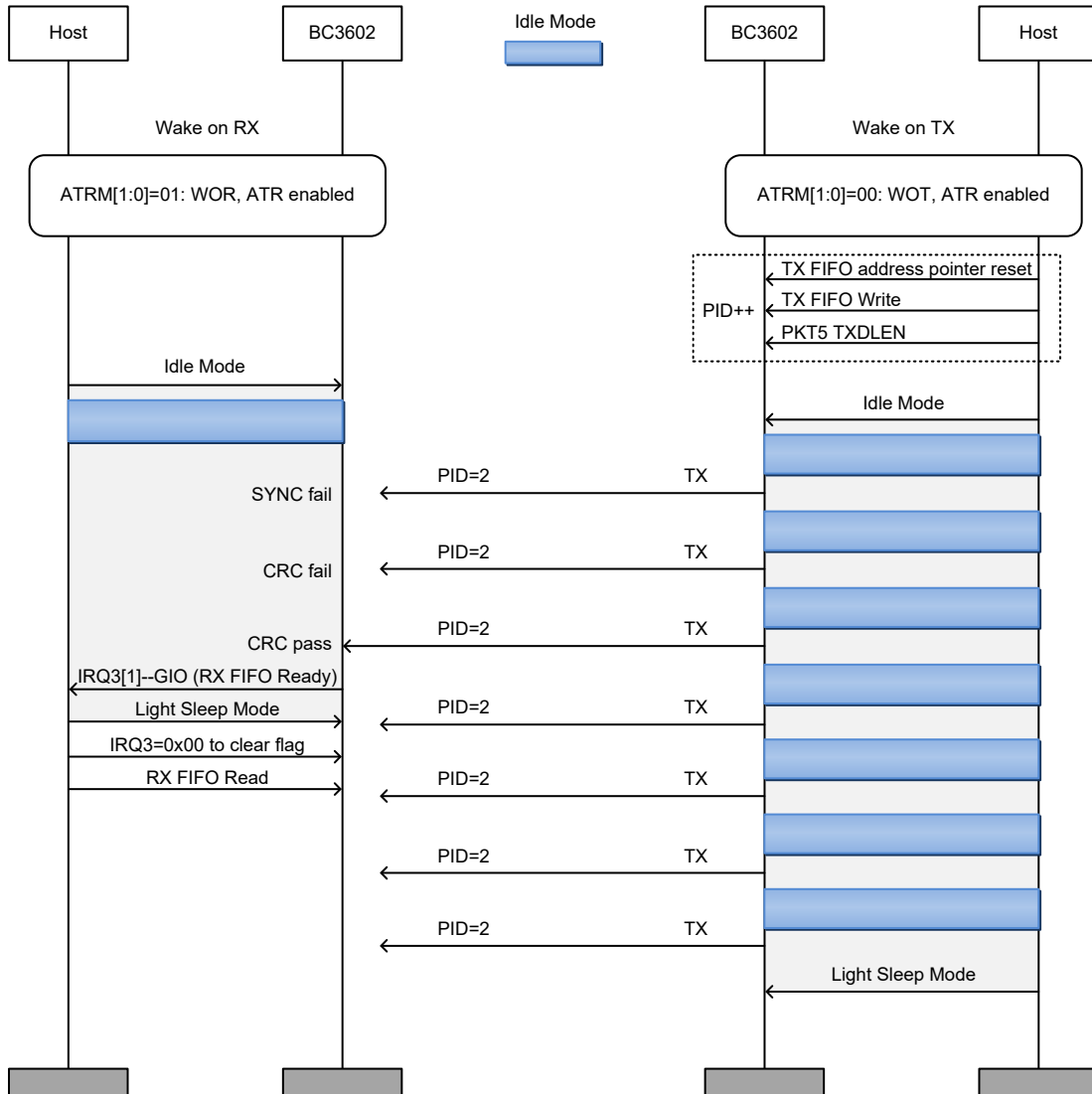


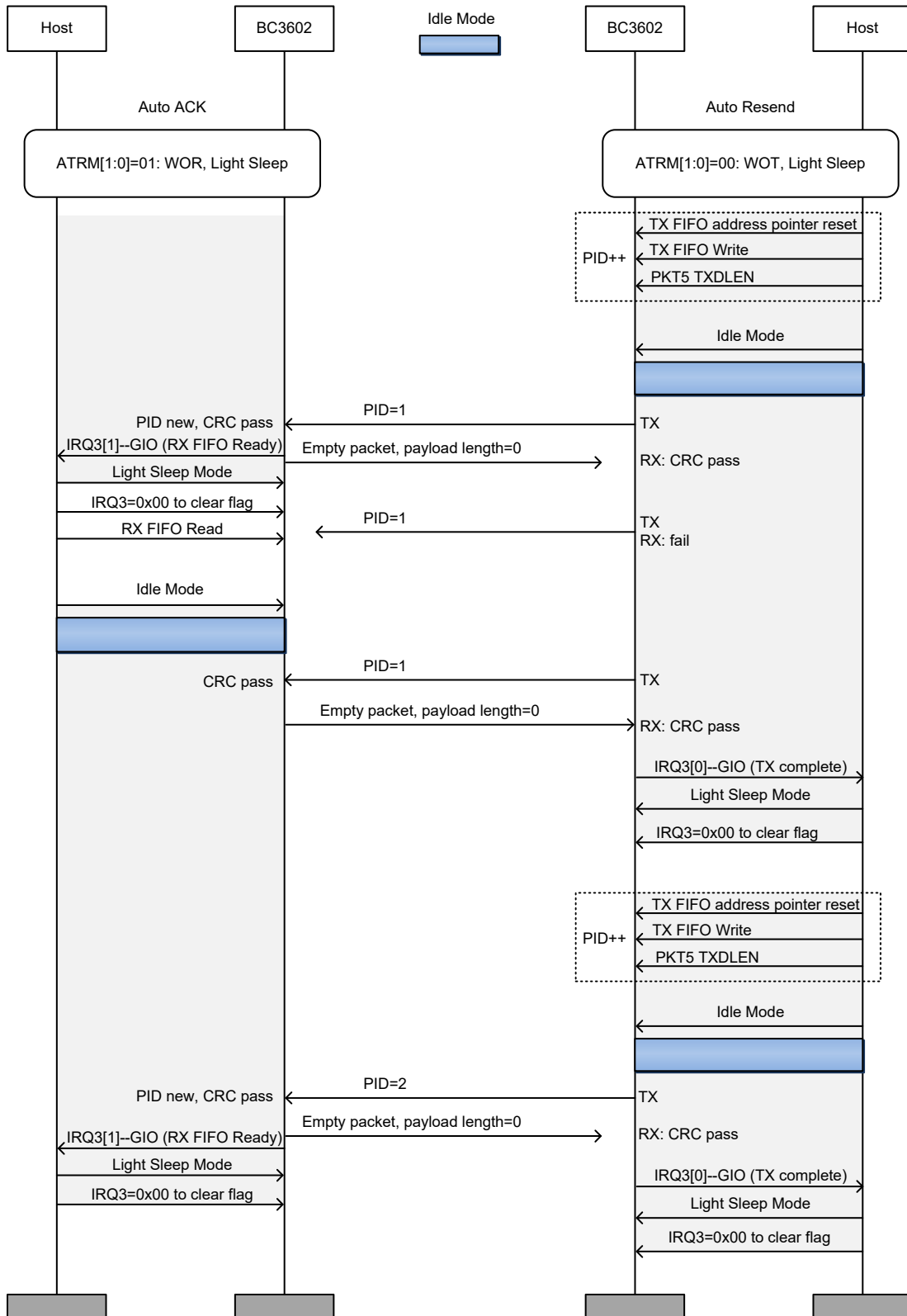
WTM (Wake up Timer Mode)

The BC3602 can be set as a programmable timer to output a periodical waveform on GIOs. User can use this signal to wake up the CPU. Set ATR_EN=1 and ATRM=10b/11b to enable the WTM mode. The device starts the WTM mode upon receiving the Idle strobe command from the MCU and stops the WTM mode upon receiving the Light Sleep strobe command. The device will stay in the Idle mode for the whole WTM process.

Message Flowchart Examples

ATR: WOT & WOR

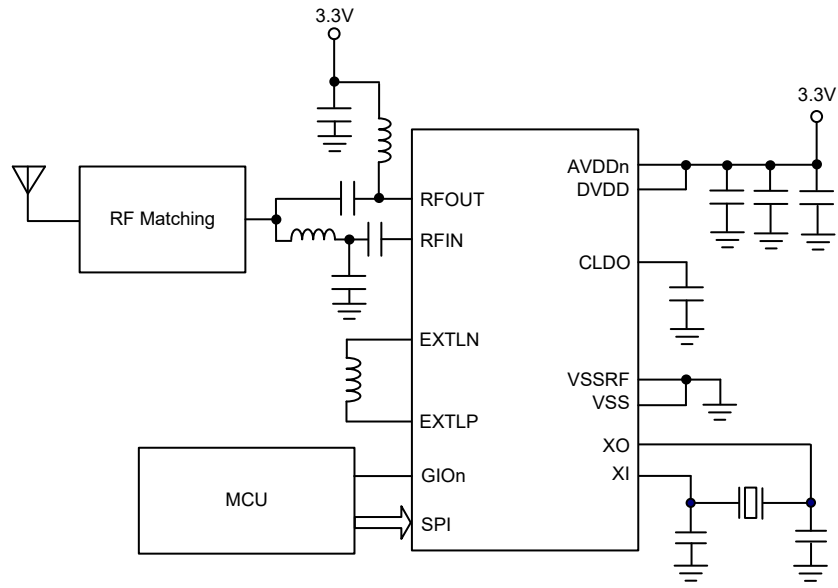




Abbreviation

ADC: Analog to Digital Converter	MMD: Multi-Mode Divider
AFC: Automatic Frequency Compensation	OW: Overwrite
AGC: Automatic Gain Control	PA: Power Amplifier
ARK: Auto-Resend and Auto-Ack	PD: Power Down
ATR: Automatic-Transmit-Receive	PFD: Phase Frequency Detector (for PLL)
BER: Bit Error Rate	PLL: Phase Lock Loop
BPF: Band Pass Filter	POR: Power On Reset
CD: Carrier Detect	PVT: Process-Voltage-Temperature
CFO: Carrier Frequency Offset	RBCLK: RX Bit Clock
CP: Charge Pump	RSSI: Received Signal Strength Indicator
CRC: Cyclic Redundancy Check	RX: Receiver
DCOC: DC Offset Correct	SNR: Signal Noise Ratio
DSM: Delta Sigma Modulator	SPI: Serial Port Interface
FEC: Forward Error Correction	SX: Synthesizer
FIFO: First In First Out	SYCK: System Clock for digital circuit
GFSK: Gaussian Frequency Shift Keying	SYNC/SYNCWORD: Synchronization Word
HPF: High Pass Filter	TBCLK: TX Bit Clock
ID: Identifier	TRX: TX/RX
IF: Intermedia Frequency	TX: Transmitter
IIR: Infinite Impulse Response	VCO: Voltage Controlled Oscillator
IRQ: Interrupt Request	WOR: Wake-on-RX
ISM: Industrial, Scientific and Medical	WOT: Wake-on-TX
LNA: Low Noise Amplifier	WTM: Wake-up Timer Mode
LO: Local Oscillator	XCLK: Crystal Clock
LPF: Low Pass Filter	XO/XOSC: Crystal Oscillator
MCU: Mico Controller Unit	XTAL: Crystal

Application Circuits

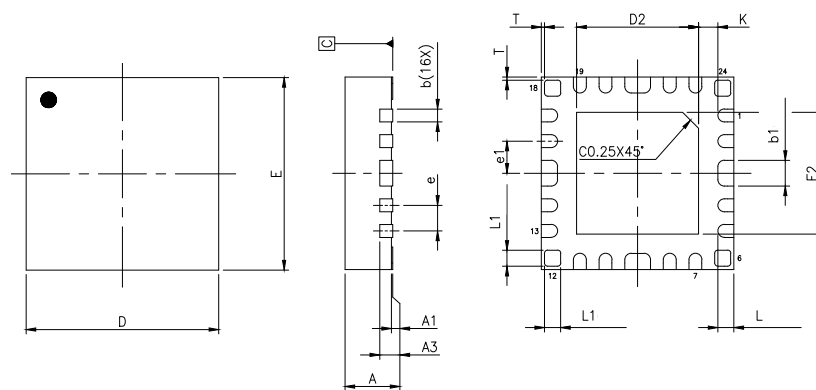


Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the [Holtek website](#) for the latest version of the [package information](#).

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Materials Information
- Carton information

SAW Type 24-pin QFN (3mm×3mm×0.55mm) Outline Dimensions


Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.020	0.022	0.024
A1	0.000	0.001	0.002
A3	—	0.006 BSC	—
b	0.006	0.008	0.010
b1	0.014	0.016	0.018
D	—	0.118 BSC	—
E	—	0.118 BSC	—
e	—	0.016 BSC	—
e1	—	0.020 BSC	—
D2	0.073	0.075	0.077
E2	0.073	0.075	0.077
L	0.006	0.010	0.014
L1	0.008	0.010	0.012
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	—	0.150 BSC	—
b	0.15	0.20	0.25
b1	0.35	0.40	0.45
D	—	3.00 BSC	—
E	—	3.00 BSC	—
e	—	0.40 BSC	—
e1	—	0.50 BSC	—
D2	1.85	1.90	1.95
E2	1.85	1.90	1.95
L	0.15	0.25	0.35
L1	0.20	0.25	0.30
K	0.20	—	—

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