Features

- Operating Voltage:
  - Receiver A_V_{DD}: 2.7V~3.6V
  - Transmitter T_V_{DD}: 2.7V~5.5V
  - Digital I/O IO_V_{DD}: 2.7V~5.5V
- Operating Temperature: -40°C~85°C
- Power Saving Modes:
  - Hard Power Down: 0.5μA
  - Soft Power Down: 4.7μA
  - Standby: 1.0mA
  - Support Card Detection mode: 10.4μA @ wakeup period=500ms
- Up to 10Mbps SPI interface speed
- 64-byte send and receive FIFO-buffer
- 64-byte addressing user-configurable registers
- Interrupt pin IRQ
- Programmable timer
- Low jitter on-chip oscillator buffer
- Ultra Low Power On-Chip 3.3V Regulator
- Low Power Card Detection
- External RF Field Detection
- Supported Protocols:
  - ISO14443A/B, all bit rates
    - 106, 212, 424 and 848kbps
  - ISO15693, all modes
    - Downlink: 1 of 4 and 1 of 256
    - Uplink: 6.6/13/26/53kbps with 1 sub-carrier
    - Uplink: 6.6/13/26kbps with 2 sub-carrier
    - Package: 24-pin QFN

Transmitter

- Modulation index adjustable by software
- Output current up to 250mA @ T_V_{DD}=5.0V
- Output impedance 3Ω @ T_V_{DD}=5.0V
- Arbitrary modulation by external signal
- Wide operating voltage for TX from 2.7V to 5.5V
- On-chip framing coder for supported standards

Receiver

- RX sensitivity down to 2mVp
- On-chip Framing decoder for supported standards
- Automatic Gain Control (AGC)

Applications

- Secure access control/door locks
- Toys
- Handheld NFC readers
- Contactless payment system

Abbreviation

AGC: Automatic gain control

CRC: Cyclic redundancy check

DPLL: Digital Phase locked Loop

EGT: Extra guard time in ISO14443B

EOF: End of Frame

ETU: Elementary Time Unit

fc: Carrier frequency

FIFO: First In, First Out Memory

SOF: Start of Frame

UID: Unique Identifier

RF: Radio Frequency

General Description

The BC45B4523 is a single-chip reader ASIC for 13.56MHz NFC/contactless standard protocols, which provides the best solution for near field wireless communication applications such as access control locks, label readers, payment machines. The device supports and compatibles with all major global secured baseband ISO standards including ISO14443 Type A, Type B, Crypto_M cards and Smart label ISO15693. The device provides a high-speed SPI controller/host interface with an integrated 64-byte FIFO for smooth data transfer. Furthermore, the embedded codec is capable of handling all bit-level coding/decoding, encrypting/decrypting as well as frame-level manipulation for transmission and reception. The device is well suited for mobile devices due to its low power consumption and low operating voltage from 2.7V to 3.6V. The ultra-low power on-chip 3.3V regulator is provided to stabilize the device power, and simultaneously supply power of up to 150mA to the external companion microcontroller.

The BC45B4523 receiver circuit has integrated a full AGC loop allowing a wide dynamic range of RF input signal levels. The excellent sensitivity performance of the device enables detection of the input signals with

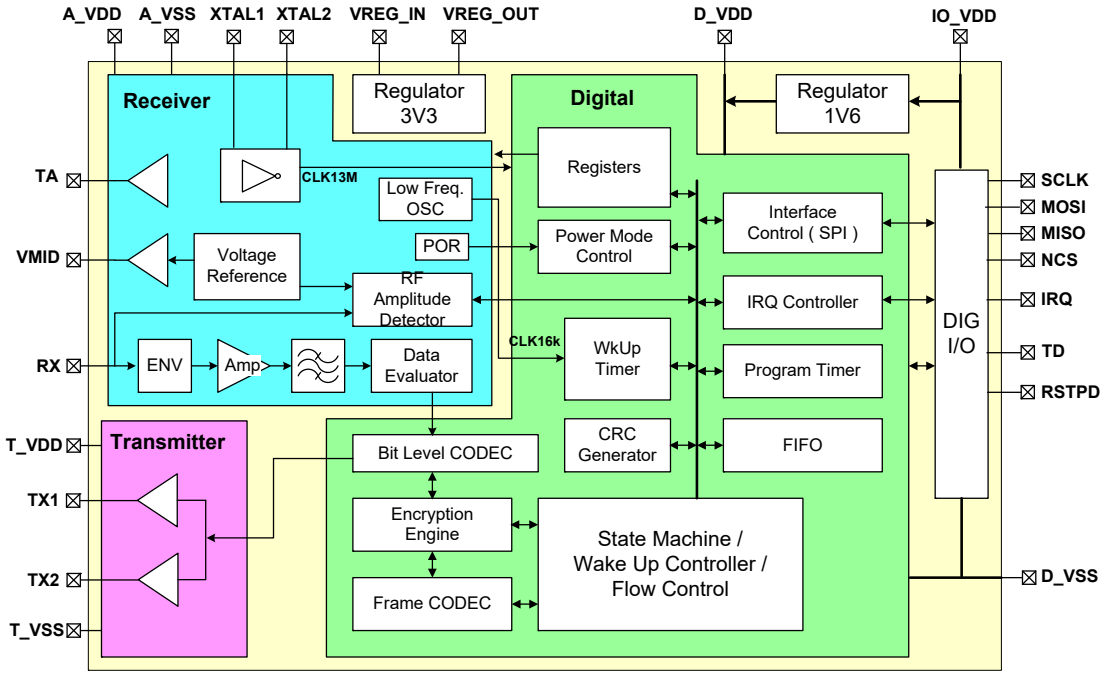
amplitudes as low as $1mV_{pp}$ without distorting the data integrity. The receiver filters can be selected optionally either to a predefined band in accordance with the generic required standard setup, or to an arbitrarily defined combination which gives flexibility to cope with various antenna variations/parameters. The baseband circuits permit the inbound/outbound configuration to accept various forms of customized protocols, incoming to the chip and outgoing to the external RF circuitry in the application specific-design system.

The transmitter is capable of accepting a wide range of operating supply voltages to serve various applications, e.g., 5V for base stations or desktop readers, and 3.3V for handheld devices. The transmission controller is entirely used to support all operation status and requests, including FIFO status full/high/low and transmission complete flag. The transmitter drivers support a wide range of power supply voltages from 2.7V to 5.5V. A high drive current up to 250mA is guaranteed for demanding item-level mid-range reader designs. The dual high-powered transmitters can be flexibly configured in various configurations, e.g. differential driving, single-ended driving and a mode to drive an external Class-E amplifier for improving the drive strength in the gate antenna setup.

The BC45B4523 contains efficient power saving modes: Hard Power Down, Soft Power Down, Standby and low-power Card Detection modes. The low-power Card Detection mode allows the device to not operate at full power continuously. The device periodically detects external card. If an external card is detected, interrupt signal will be sent to MCU to wake up the system.

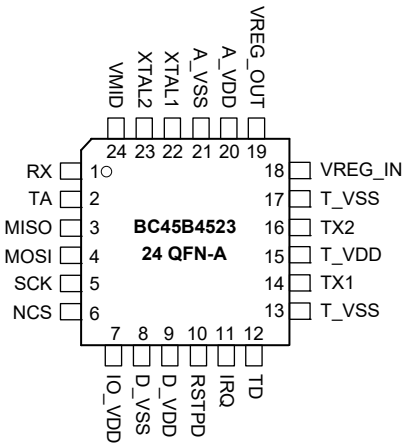
To facilitate operation of the companion microcontroller, the BC45B4523 is fully equipped with on-chip peripheral support devices such as an RF-trig timer, a host interrupt generator and a clock divider. The BC45B4523 is offered in a QFN package with excellent heat dissipation when self-mounted on PCB.

Block Diagram



Functional Block Diagram

Pin Assignment



Pin Description

Pin No.	Pin Name	Type	Description
1	RX	Analog Input	Receiver input
2	TA	Analog Output	Analog Test pin
3	MISO	Digital Output	SPI: Master In Slave Out
4	MOSI	Digital Input	SPI: Master Out Slave In
5	SCK	Digital Input	SPI: Clock input
6	NCS	Digital Input	SPI: Chip Select (Active Low)
7	IO_VDD	Power	Digital I/O power supply
8	D_VSS	Power	Digital and digital I/O ground
9	D_VDD	Power	Digital core power supply (need an external 100nF decoupling capacitor)
10	RSTPD	Digital Input	Master Reset (Active High)
11	IRQ	Digital Output	Interrupt Request output
12	TD	Digital I/O	Digital Test pin
13	T_VSS	Power	Transmitter ground
14	TX1	Output	Transmitter output # 1
15	T_VDD	Power	Transmitter power supply
16	TX2	Output	Transmitter output # 2
17	T_VSS	Power	Transmitter ground
18	VREG_IN	Power	On-chip Regulator input (5.0V)
19	VREG_OUT	Power	On-chip Regulator output (3.3V)
20	A_VDD	Power	Analog power supply (3.3V)
21	A_VSS	Power	Analog ground
22	XTAL1	Analog Input	Crystal oscillator input
23	XTAL2	Analog Output	Crystal oscillator output
24	VMID	Analog Output	Mid rail reference voltage

Electrical Characteristics

Absolute Maximum Rating

Stresses exceeding those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to the absolute maximum rating conditions for an extended period of time may affect the device reliability. Only one absolute maximum rating can be applied at a time.

Parameter	Rating
Analog Supply Voltage (A_V_{DD} to A_V_{SS})	-0.5V to 3.6V
Digital I/O Supply Voltage (IO_V_{DD} to D_V_{SS})	-0.5V to 5.5V
Transmitter Supply Voltage (T_V_{DD} to T_V_{SS})	-0.5V to 5.5V
Digital Core Output Supply Voltage (D_V_{DD} to D_V_{SS})	-0.5V to 2.4V
Analog Input Voltage)	-0.5V to A_V_{DD}+0.3V
Analog output Voltage	-0.5V to A_V_{DD}+0.3V
Digital Input Voltage	-0.5V to IO_V_{DD}+0.3V
Digital Output Voltage	-0.5V to IO_V_{DD}+0.3V
Transmitter Output Voltage	-0.5V to T_V_{DD}+0.3V
Regulator Input Voltage (V_{REG_IN} to D_V_{SS})	-0.5V to 5.5V
Regulator Output Voltage (V_{REG_OUT} to D_V_{SS})	-0.5V to 5.5V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	125°C
Thermal Impedance (θ_{JA})[Note] – QFN 4×4	34.04°C/W

Note: θ_{JA} is determined by JEDEC 2S2P (4L), PCB size 76.2×114.3mm with 2×2 vias, following JEDEC51-5, -7.

Operating Condition

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
A_V_{DD}	Analog Power Supply Voltage	—	2.7	3.3	3.6	V
IO_V_{DD}	Digital I/O Power Supply Voltage	—	2.7	3.3	5.5	V
D_V_{DD}	Digital Core Power Supply Voltage	Regulated from internal	1.54	1.65	2.20	V
T_V_{DD}	Transmitter Power Supply Voltage	—	2.7	5.0	5.5	V
ESD	Electrostatic Discharge Tolerance	HBM model	—	1.5	—	kV
V_{POR}	Reset Trigger Voltage	IO_V_{DD} & A_V_{DD}	2.3	2.4	2.6	V

Power Consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I\_A\_V_{DD}$	Analog Power Supply Current A_V_{DD}=3.3 V	Active state (receiver on)	—	5.5	6.4	mA
		Idle state (receiver off)	—	0.8	1.0	mA
		Hard Power Down (pin RSTPD=1)	—	—	0.2	μA
		Soft Power Down (bit PowerDown=1), 25°C	—	1.7	2.4	μA
		Soft Power Down (bit PowerDown=1), -40°C to 85°C	—	—	3.5	μA
		Standby (bit StandBy=1)	—	0.7	0.9	mA
		Wake Up Card Detection Mode (Bit WkUpCD=1) – Sleep phase[Note], 25°C	—	1.7	2.4	μA
		Wake Up Card Detection Mode (Bit WkUpCD=1) – Detect phase[Note]	—	3.0	3.3	mA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I\_IO\_V_{DD}$	Digital I/O Power Supply Current (Also Include Digital Core Current) IO_V_{DD}=3.3 V	Active state (CODEC on)	—	1.0	1.2	mA
		Idle state (CODEC off)	—	0.9	1.1	mA
		Hard Power Down (pin RSTPD=1)	—	—	0.2	μA
		Soft Power Down (bit PowerDown=1), 25°C	—	3.0	4.2	μA
		Soft Power Down (bit PowerDown=1), -40°C to 85°C	—	—	7.0	μA
		Standby (bit StandBy=1)	—	0.3	0.5	mA
		Wake Up Card Detection Mode (bit WkUpCD=1) – Sleep phase[Note]	—	3.0	4.2	μA
		Wake Up Card Detection Mode (bit WkUpCD=1) – Detect phase[Note]	—	0.9	1.1	mA
I_{total}	Total Power Supply Current $I\_IO\_V_{DD}$ + $I\_A\_V_{DD}$ + $I\_T\_V_{DD}$ IO_V_{DD}=A_V_{DD}=T_V_{DD}=3.3V, I_TX=100mA (Not Apply On-Chip 3.3V Regulator, VREG_IN and VREG_OUT are Not Connected)	Active state (receiver on, transmitter off)	—	6.6	7.6	mA
		Idle state (receiver off, transmitter off)	—	1.7	2.1	mA
		Hard Power Down (pin RSTPD=1)	—	—	0.8	μA
		Soft Power Down (bit PowerDown=1), 25°C	—	—	11.0	μA
		Standby (bit StandBy=1)	—	1.0	1.4	mA
		Average at Wake Up Card Detection Mode @ TwkUp=500ms, transmitter on periodically (calculated)	—	10.4	—	μA
		Average at Wake Up Card Detection Mode @ TwkUp=1000ms, transmitter on periodically (calculated)	—	7.5	—	μA

Note: Average power in Wake Up Card Detection Mode depends on duty cycle between Sleep and Detect period.

Pin Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C_{Rx}	RX Input Capacitance	—	—	4	—	pF
I_{Rx}	RX Input Leakage Current	V_{Rx}=1.65V, 25°C	—	—	0.4	μA
Cin, io	Digital Pin Input Capacitance	—	—	5	—	pF
V_{INL}	Digital Logic Input Low Voltage	—	—	—	0.8	V
V_{INH}	Digital Logic Input High Voltage	—	IO_V_{DD} - 0.8	—	—	V
V_{OL}	Digital Logic Output Low Voltage	IO_V_{DD}=3.3V, I_{sink}=3mA	—	—	0.5	V
V_{OH}	Digital Logic Output High Voltage	IO_V_{DD}=3.3V, I_{source}=3mA	2.8	—	—	V
T_r	Rise Time	IO_V_{DD}=3.3V, C_L=15pF	—	4	10	ns
T_f	Fall Time	IO_V_{DD}=3.3V, C_L=15pF	—	4	10	ns
Iin,logic1	Logic 1 Input Current	V_{INH}=IO_V_{DD}, 25°C	—	—	0.4	μA
Iin,logic0	Logic 0 Input Current	V_{INL}=0, 25°C	—	—	0.4	μA
Iout,logic1	Logic 1 Output Source Current	IO_V_{DD}=3.3V, 25°C	3	—	—	mA
Iout,logic0	Logic 0 Output Sink Current	IO_V_{DD}=3.3V, 25°C	3	—	—	mA

Transmitter Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_TX	Transmitter Current, Continuous Wave	T_V_{DD}=5V, 25°C, Average Current	—	—	250	mA
Z_TX,min	Minimum Equivalent TX Output Impedance (TxCfgCW=0x3F)	T_V_{DD}=5V, 25°C	—	3	5	Ω
I_T_V_{DD},static	Transmitter Static Power Supply Current	Pin TX1 & TX2 are unconnected TX1RFEn=1, TX2RFEn=1 T_V_{DD}=5V	—	7	—	mA
M	Adjustable Modulation Index	T_V_{DD}=5V, 100ASK=0	0	—	60	%
		T_V_{DD}=5V, 100ASK=1	—	—	100	

Receiver Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{SEN}	Receiver Input Sensitivity	A_V_{DD}=3.3V	—	2	—	mVp
PSRR	Power Supply Rejection Ratio	A_V_{DD}=3.3V + 0.2×sin(1MHz)	—	40	—	dB
V_{Rx}	RX Input Voltage Range	A_V_{DD}=3.3V, ByPassENV=0	0.0	—	3.3	V
		A_V_{DD}=3.3V, ByPassENV=1	0.5	—	2.8	
V_{Car},Min	Minimum Carrier for Envelope Detector	—	—	0.25	—	Vp
V_{VMID}	VMID Voltage	A_V_{DD}=3.3V	1.63	1.65	1.67	V
Z_{VMID}	VMID Output Impedance @ 13.56MHz	C_L=100nF, A_V_{DD}=3.3V	—	—	0.5	Ω
Gain	Gain (Measured from RX to the output of the internal last amplifier)	Gain[1:0]=11, Gain_ST3[2:0]=000	—	—	48	dB
		Gain[1:0]=00, Gain_ST3[2:0]=000	12	—	—	
Gstep	Gain Step	AGCEn=1	—	3	—	dB
		AGCEn=0 Defined by Gain[1:0]	—	12	—	
RxNoise	Intrinsic Input Referred Noise in RX	—	—	TBD	—	mVrms
FD, min	Minimum RF Amplitude at RX Pin for External RF Field Detection	RF input at RX pin is in phase with internal clock. When the phase is different this value will be more.	—	10	—	mVp
CD, min	Minimum RF Amplitude Changing at RX pin for Card Detection		—	10	—	mVp

Operation Timing

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
TPowerup[Note]	Startup Time from Power-up	From Power up till system ready for SPI communication	—	—	4	ms
TstSPD[Note]	Startup Time from Soft Power Down	From clearing Powerdown=0 until system ready for SPI communication	—	—	1.8	ms
TstHPD[Note]	Startup Time from Hard Power Down	From configuring pin RSTPD=0 until system ready for SPI communication	—	—	2.4	ms
TstSTBY	Startup Time from Standby Mode	From clearing Standby=0 until system ready for SPI communication	—	0.5	—	μs

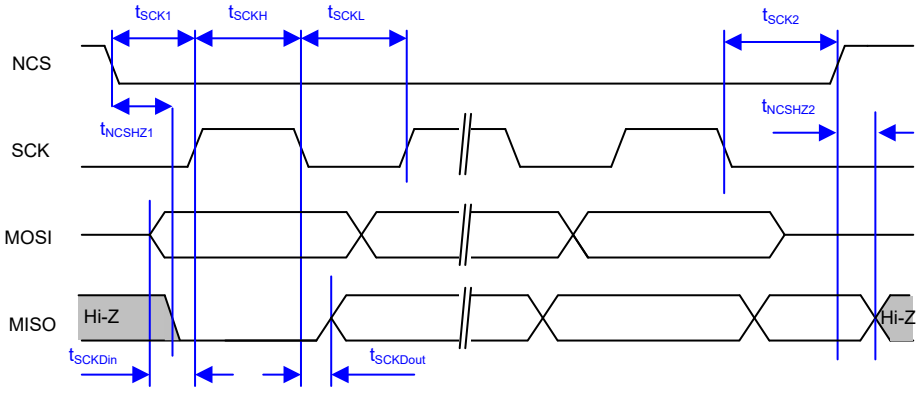
Note: Startup time is depended on the characteristic of external 27.12MHz quartz crystal.

Regulator Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{REG_IN}	Regulator Input Voltage	—	3.6	5.0	5.5	V
V_{REG_OUT}	Regulator Output Voltage	I_{OUT}=10mA, 25°C	3.25	3.30	3.35	V
I_{OUT}	Output Regulator Current	—	—	—	150	mA
$\Delta Vout_{LineReg}$	Line Regulation (ΔVout)	I_{OUT}=0mA, 3.6V < V_{REG_IN} < 5.5V	—	0.5	1.0	mV/V
$\Delta Vout_{LoadReg}$	Load Regulation (ΔVout)	V_{REG_IN}=5V, 0 < I_{OUT} < 150mA	—	0.25	—	mV/mA
I_{REGq}	Regulator Quiestcent Current	No Load, V_{REG_IN}=5V, 25°C	—	2	—	μA
		I_{OUT}=100mA, V_{REG_IN}=5V, 25°C	—	100	—	

SPI Characteristics

Symbol	Parameter	Min.	Max.	Unit
t_{SCK1}	NCS Low to 1st SCK High	12	—	ns
t_{SCK2}	Last SCK Low to NCS High	12	—	ns
t_{SCKH}	SCK High Period	25	—	ns
t_{SCKL}	SCK Low Period	25	—	ns
t_{SCKDin}	Data Change to SCK High	12	—	ns
$t_{SCKDout}$	SCK Low to Data Change	12	—	ns
t_{NCSHZ1}	NCS Low to MISO Active	12	—	ns
t_{NCSHZ2}	NCS High to MISO Hi-Impedance	12	—	ns
SPI_{clk}	SPI Clock	—	10	MHz



SPI Interface Timing

Supported Protocols

Protocol	Transmitter		Receiver	
	Rate (kbps)	Coding	Rate (kbps)	Coding
ISO14443A	106, 212, 424, 848	Miller	106	Manchester
			212, 424, 848	BPSK
ISO14443B	106, 212, 424, 848	NRZ	106, 212, 424, 848	BPSK
ISO15693	26, 1.67	1 of 4, 1 of 256	53, 26, 13, 6.7	Manchester
			26, 13, 6.7	FSK
Crypto_M	106	Miller	106	Manchester

Peripheral Specifications

Block	Properties	Min.	Typ.	Max.	Unit
FIFO	Total Size	—	64	—	Byte
Program Timer	Time Count	—	—	39.6	Sec
	Trigger Source	TxStart, TxStop, RxStart, RxStop, User			—
Wake Up Timer	Time Count (for WkUpCD)	61.0μs	—	1 day	—
	Timer Accuracy	-1.5	—	+1.5	%
	Trigger Source	User configuration			—
Interrupt	Trigger Source	—			—
	Output Level	Toggle High, Toggle Low			—

Crystal Requirement

Symbol	XTAL Spec	Min.	Typ.	Max.	Unit
f_{XTAL}	Frequency	—	27.12	—	MHz
TOL	Frequency Tolerance	—	—	±30	ppm
C_{LOAD}	Load Capacitance	—	10	—	pF
ESR	Equivalent Series Resistance	—	—	120	Ω

Functional Overview

The BC45B4523 contains a transmitter, a receiver, a baseband processor and a voltage regulator. The functional block diagram of the device is shown in the Block Diagram chapter.

The transmitter contains integrated dual drivers, supporting operating voltage from 2.7V to 5.5V. The transmitter can be configured to support various antenna topologies such as differential driving, single-ended driving and pre-driving for external Class-E amplifiers. An on-chip coder can generate a variety of line-coding, namely Miller to support ISO14443A, NRZ to support ISO14443B, and 1-of-4 and 1-of-256 to support ISO15693. Moreover, a direct modulation from pin TD is allowed.

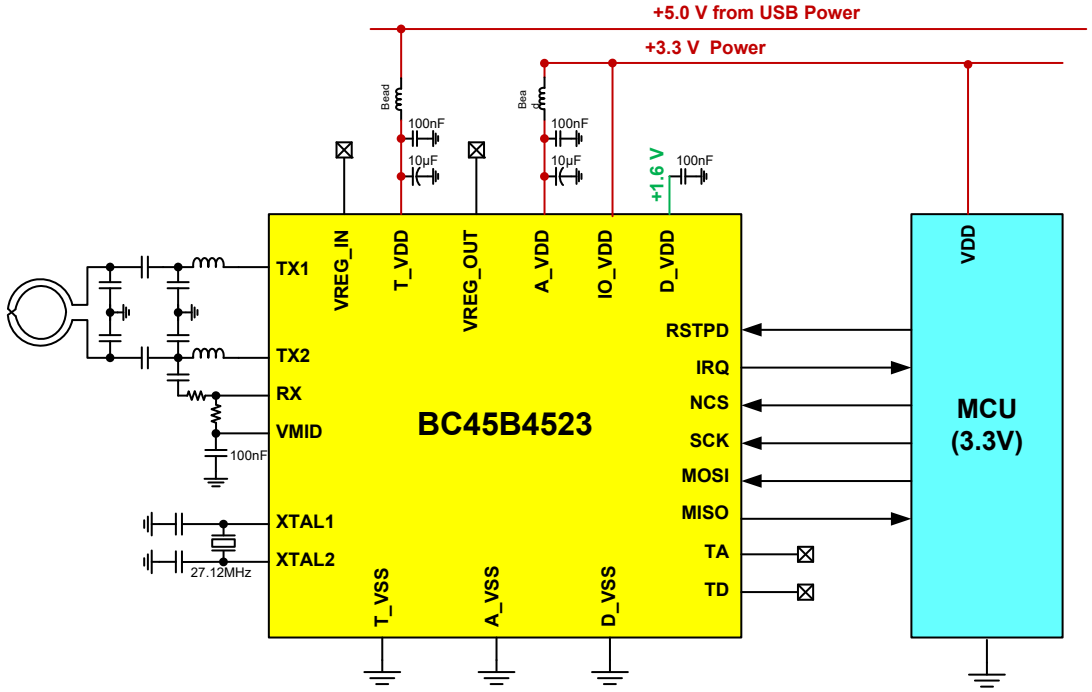
The receiver consists of an on-chip envelope detector, a voltage reference generator, an on-chip oscillator, an amplifier & filter system, a filter tuning system, a BPSK bit decoder, a Manchester-and-FSK bit decoder, a frame decoder and a timing control generator. A receiver input, pin RX, can accept a carrier modulated signal or an envelope-demodulated signal from an external envelope detector. Employing an external envelope detector can yield an extended read range. With this flexibility, it enables a wide variety of RF connection topologies. The envelope of the input signal is filtered and amplified with optional control by an automatic gain control (AGC), resulting in an amplitude control to prevent shape distortion. The BPSK bit decoder and Manchester-and-FSK bit decoder translates the amplified signal to the digital data. The bit data is then checked the validity and assembled into bytes by the digital frame decoder. Next, the complete and valid bytes are transferred into the FIFO. In case of the encryption, the Crypto_M engine is provided to encrypt and decrypt as well as execute the authentication process for the Crypto_M card.

The digital part contains an FIFO controller, a CRC generator, a programmable timer, a wake-up timer, a state machine, a wake-up controller and configurable registers in order to facilitate RF transmission and reception activities. The BC45B4523 can be controlled and accessed through a 4-wire SPI interface and register pages with the communication speed of up to 10Mbps. An interrupt system and a pin IRQ are provided to support interrupt-oriented programming after the end of RF activities.

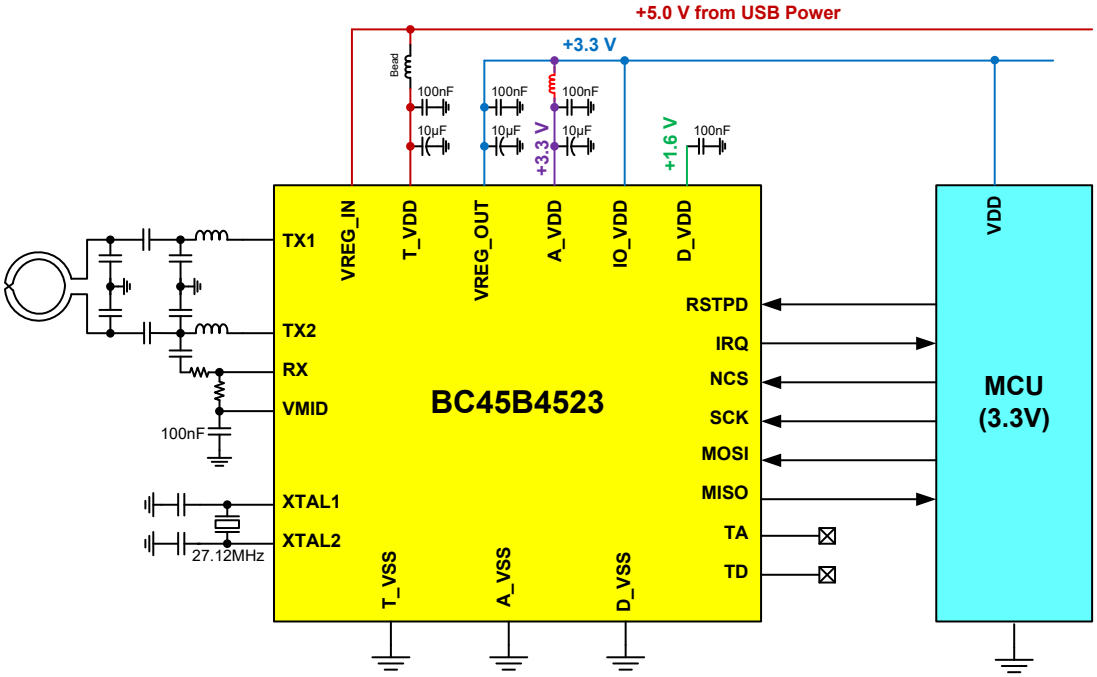
In addition, there are two regulators, 3.3V and 1.6V output. The 3.3V regulator is applied for supplying external load, MCU or analog parts itself with 150mA driving capability. The 1.6V output is regulated voltage from pin IO_VDD to D_VDD for supplying digital circuit itself.

Typical Operating Circuit

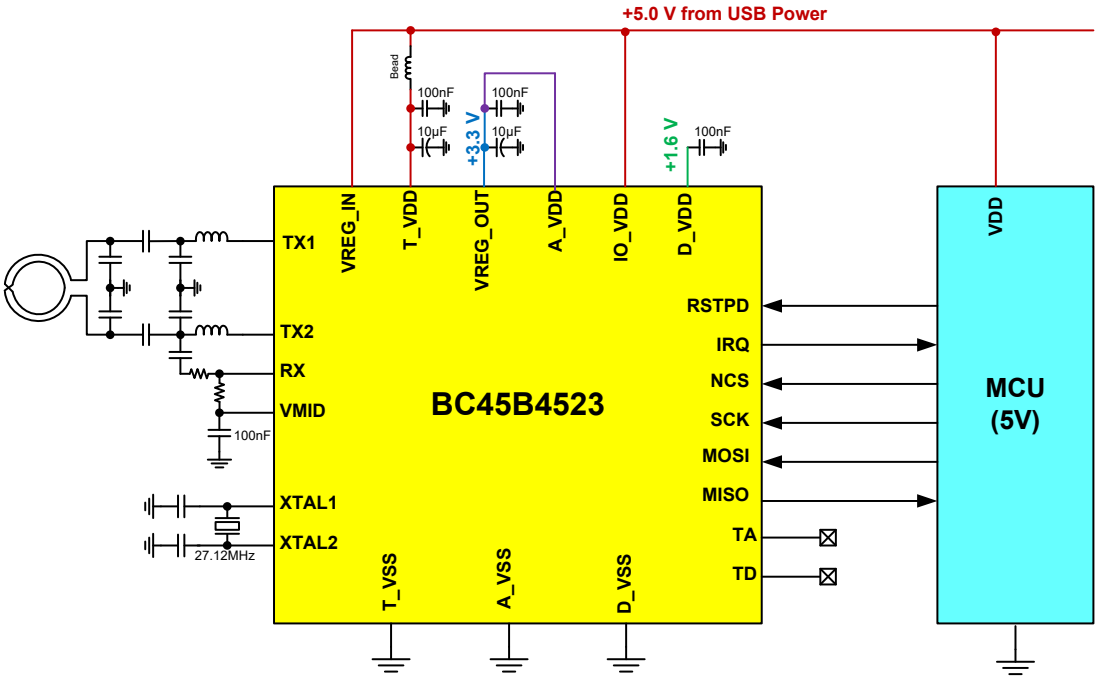
A basic operating circuit and a typical usage are illustrated in the following figures. A differential antenna is directly connected to the transmitter driver of the BC45B4523, whereas the receiver senses the tag-modulated signal from the envelope of RF carrier through the voltage divider. The device is controlled by a microcontroller via an SPI interface. In addition, other circuit configurations such as Class-E amplifiers with external envelope detectors or single-ended drivers can be implemented and will be described in the “Circuit Configuration” section.



Typical Operating Circuit for External Power Supply (Not Apply On-Chip 3.3V Regulator)



Typical Configuration Employing On-Chip Regulator for MCU with 3.3V I/O



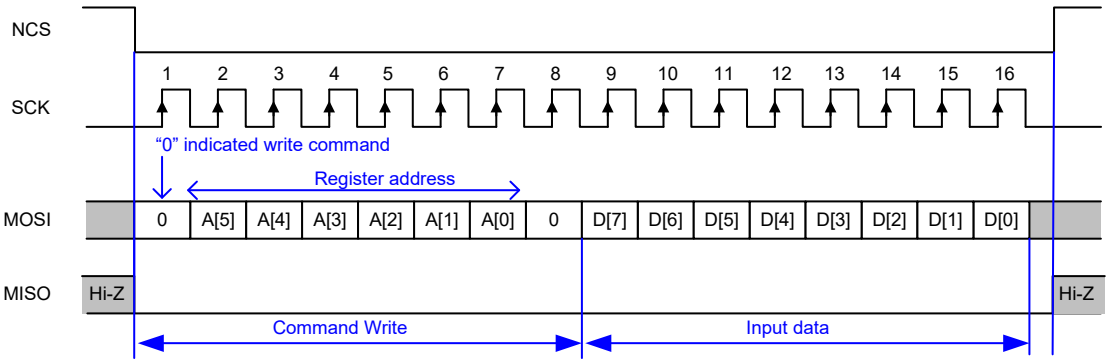
Typical Configuration Employing On-Chip Regulator for MCU with 5.0V I/O

SPI Interface

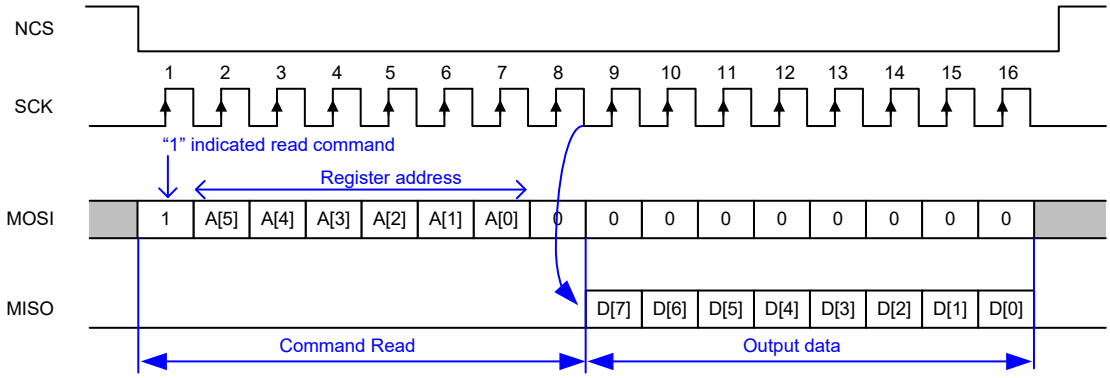
The BC45B4523 can be interfaced through a standard 4-wire SPI interface in order to access to internal registers. The SPI interface is capable of handling input stream with a speed of up to 10Mbps. There are 4 modes available where their timing diagrams are depicted in the following figures. Depending on activities of the interfacing controller, the purpose and usage of each SPI mode are shown in the table below. The timing constrain is shown in "SPI Interface Timing" diagram presented in the "SPI Characteristics" section. Note that if NCS is set to high, MISO will become high-impedance. This allows multiple SPI devices, in which Hi-Z feature in MISO is available, controlled from the same MCU shown as the last figure in this section.

Mode	Purpose and Usage
Single register/single byte write	Setting value from a single setting register
Single register/single byte read	Reading value from a single setting register
Single register/multiple-byte write	Writing consecutive data to FIFO
Multiple register/multiple-byte read	Reading consecutive data from FIFO. Monitoring status of the device

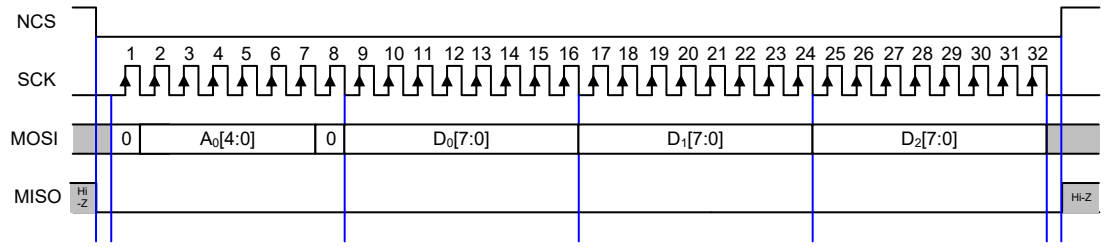
SPI Mode



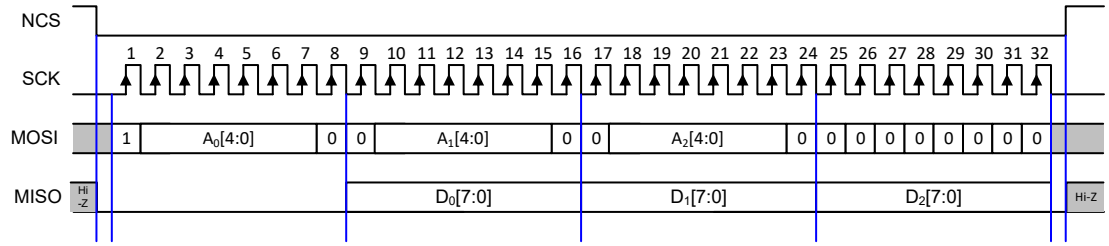
SPI Interface for Single Register/Single Byte Write



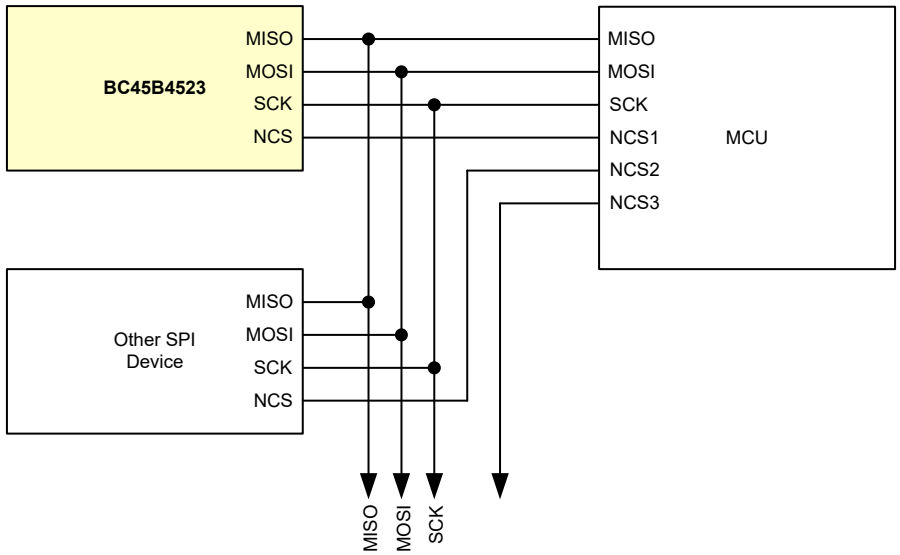
SPI Interface for Single Register/Single Byte Read



SPI Interface for Single Register/Multiple-Byte Write



SPI Interface for Multiple Register/Multiple-Byte Read



SPI Interface to Multiple SPI Devices Having hi-Z Feature in MISO Output

Registers

Register Overview

The device consists of 6-bit addressable registers which is grouped into 2 sectors. Each sector separated into multiple pages by their functions. There are 4 types of registers, namely Dynamic, Write Only, Read/Write and Read Only, in which their behaviours are described in the following table. The overview of the registers is shown in the "Register List" tables.

Type	Description
Dynamic (DY)	The Dynamic register is used to control behaviours of the reader IC as wells as display the status. The Dynamic register can be either set by the external controller or automatically updated by the internal state machine.
Write Only (W)	The write-only register is used for control behaviours of the reader IC, especially timers and FIFO. These registers can only be written by the external controller. Reading from these registers returns zero.
Read/Write (R/W)	The read-write register is used to configure and control behaviours of the reader IC. These registers can be written and read by the external controller.
Read Only (R)	The read only register is used to display the status of the internal state machine. Writing these registers will not affect their values.
—	These registers are intentionally left blank or reserved for future use, reading from these registers returns zero.

Register Types

Register List

Sector 0

Page		Addr.		Register Name	Bit							
					7	6	5	4	3	2	1	0
Command and Status	0	0	0	Sector Select	—	—	—	—	—	—	—	Sector
		0	1	Command	Command[7:0]							
		0	2	FIFOData	FIFOData[7:0]							
		0	3	PrimaryStatus	—	ModemState[2:0]			IRQ	ERR	HiAlert	LoAlert
		0	4	FIFOLength	—	FIFOLength[6:0]						
		0	5	SecondaryStatus	Trunning	RF_Det	CRCReady	EMD_Det	SubC_Det	RxLastBit[2:0]		
		0	6	InterruptEnable	SetIEn	CDIEn	TimerIEn	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn
		0	7	InterruptFlag	SetIRq	CDIRq	TimerIRq	TxIRq	RxIRq	IdleIRq	HiAlertIRq	LoAlertIRq
Control and Status	1	0	8	—	—	—	—	—	—	—	—	—
		0	9	Control	—	WkUpCD	StandBy	PowerDown	Crypto_MOn	TStopNow	TStartNow	FlushFIFO
		0	A	Error	—	KeyErr	—	FIFOOvf	CRCErr	FramingErr	ParityErr	CollErr
		0	B	CollPos	CollPos[7:0]							
		0	C	TimerValue	TimerValue[7:0]							
		0	D	CRCResultLSB	CRCResultLSB[7:0]							
		0	E	CRCResultMSB	CRCResultMSB[7:0]							
		0	F	BitFraming	—	RxAlign[2:0]			—	TxLastBits[2:0]		
TX and Coder	2	1	0	—	—	—	—	—	—	—	—	—
		1	1	TxControl	Tx1Inv	ModulatorSource		100ASK	Tx2Inv	Tx2Cw	Tx2RFEn	Tx1RFEn
		1	2	TxCfgCW	—	—	TxCfgCW[5:0]					
		1	3	TxCfgMod	—	—	TxCfgMod[5:0]					
		1	4	CoderControl	Send1Pulse	—	CoderRate[2:0]		TxCoding[2:0]			
		1	5	ModWidth	ModWidth[7:0]							
		1	6	ModWidthSOF	ModWidthSOF[7:0]							
		1	7	TypeBTxFraming	NoTxSOF	NoTxEOF	EOFWidth	CharSpacing[2:0]			SOFWidth[1:0]	
RX and Decoder	3	1	8	—	—	—	—	—	—	—	—	—
		1	9	RxControl1	SubCPulses[2:0]			SubCCarrier[1:0]		LP_Off	Gain[1:0]	
		1	A	DecoderControl	RxMultiple	CollMarkVal	ZeroAfterColl	RxFraming[1:0]		—	RxCoding[1:0]	
		1	B	BitPhase	BitPhase[7:0]							
		1	C	RxThreshold	MinLevel[2:0]			—	CollLevel[2:0]			—
		1	D	BPSKDemControl	NoRxSOF	NoRxEGT	NoRxEOF	HP2Off	TauD[1:0]		AGCEn	TauAGC
		1	E	RxControl2	Cont_Int	RxAutoPD	—	—	Reserved	ByPassEnv	Reserved	DecoderSrc
		1	F	RxControl3	BPSKDecMeth	BPSKDataRec	SOFSel15693	—	—	—	EMD_ Suppress	SOF43A_5Bits

Page		Addr.		Register Name	Bit							
					7	6	5	4	3	2	1	0
RF-Timming, Channel Redundancy and ADC	4	2	0	Reserved	Reserved							
		2	1	RxWait	RxWait[7:0]							
		2	2	ChannelRedundancy	—	MSBFirst	CRC3309	CRC8	RxCRCEn	TxCRCEn	ParityOdd	ParityEn
		2	3	CRCPresetMSB	CRCPresetMSB[7:0]							
		2	4	CRCPresetLSB	CRCPresetLSB[7:0]							
		2	5	ADCCtrl	—	—	ADC_Delay[1:0]		FD_MinLvl	ADC_FastMode	ADC_Rsln	Reserved
		2	6	ADC_Result_I	ADC_Result_I[7:0]							
		2	7	ADC_Result_Q	ADC_Result_Q[7:0]							
FIFOLevel, Prog. Timer and Wake Up Timer	5	2	8	—	—	—	—	—	—	—	—	—
		2	9	FIFOLevel	—	—	WaterLevel[5:0]					
		2	A	TimerClock	—	—	TAutoRestart	TPreScaler[4:0]				
		2	B	TimerControl	—	—	—	—	TStopRxEnd	TStopRxBegin	TStartTxEnd	TStartTxBegin
		2	C	TimerReloadValue	TReloadValue[7:0]							
		2	D	WkTimerControl	WkTStartNow	WkTStopNow	WkTRunning	WkTAutoRestart	WkTPreScaler[3:0]			
		2	E	WkTimerReloadValue	WkTReloadValue[7:0]							
		2	F	WkTtrigTime	—	—	—	—	WkTtrigTime[3:0]			
Field Detection and Card Detection	6	3	0	FDControl	Reserved	FDDetectTime[2:0]			—	—	FDAverage[1:0]	
		3	1	WkCDControl	Reserved	WkCDGoActive	WkIgnoreFD	WkFDEn	Reserved	CDTxDelay	CDAverage[1:0]	
		3	2	FDThreshold_I_H	FDThreshold_I_H[7:0]							
		3	3	FDThreshold_Q_H	FDThreshold_Q_H[7:0]							
		3	4	CDThreshold_I_L	CDThreshold_I_L[7:0]							
		3	5	CDThreshold_I_H	CDThreshold_I_H[7:0]							
		3	6	CDThreshold_Q_L	CDThreshold_Q_L[7:0]							
		3	7	CDThreshold_Q_H	CDThreshold_Q_H[7:0]							
Test, IO Control and RX Adjustment	7	3	8	—	—	—	—	—	—	—	—	—
		3	9	TDIRqCtrl	—	—	IO1_InValue	IO0_InValue	TDSelect	IO1_Mode	IO0_Mode	IRqInv
		3	A	Test	Reserved	Test[6:0]						
		3	B	Reserved	Reserved							
		3	C	Rx43A_Option	Reserved	RxCorrIntTime[1:0]		Reserved	SOFSel43A	Reserved		
		3	D	Reserved	Reserved							
		3	E	Reserved	Reserved							
		3	F	Gain_ST3	Reserved		Gain_ST3[2:0]			Reserved		

Sector 1

Page		Addr.		Register Name	Bit							
					7	6	5	4	3	2	1	0
LFO and ADC Adjustment	0	0	0	Sector Select	—	—	—	—	—	—	—	Sector
		0	1	LFOTrimResult	LFOTrimResult[7:0]							
		0	2	ManLFOTrimValue	ManLFOTrimValue[7:0]							
		0	3	LFOTrimSel	Reserved				—	—	—	ManLFOTrim
		0	4	FDCDIRqConfig	—	—	—	—	FDIRqCfg[1:0]		CDIRqCfg[1:0]	
		0	5	ADC_Adjust	—	—	—	—	Reserved		ADC_FullScaleAdj[1:0]	
		0	6	—	—	—	—	—	—	—	—	—
		0	7	—	—	—	—	—	—	—	—	—
Production Parameter	1	0	8	Reserved	Reserved							
		0	9	Reserved	Reserved							
		0	A	—	—	—	—	—	—	—	—	—
		0	B	Reserved	Reserved							
		0	C	—	—	—	—	—	—	—	—	—
		0	D	MaskSet	MaskSet[7:0]							
		0	E	ProductionParam	ProductionParam[7:0]							
		0	F	Revision	Revision[7:0]							

Page		Addr.		Register Name	Bit							
					7	6	5	4	3	2	1	0
TX Overshoot Control	2	1	0	TxFallingCtrl	TxOvsT1Fall[3:0]				TxOvsT2Fall[3:0]			
		1	1	TxRisingCtrl	TxOvsT1Rise[3:0]				TxOvsT2Rise[3:0]			
		1	2	TxCfgFall	—	—	TxCfgFall[5:0]					
		1	3	TxCfgRise	—	—	TxCfgRise[5:0]					
		1	4	—	—	—	—	—	—	—	—	—
		1	5	—	—	—	—	—	—	—	—	—
		1	6	—	—	—	—	—	—	—	—	—
		1	7	—	—	—	—	—	—	—	—	—
	3	1	8	—	—	—	—	—	—	—	—	—
		1	9	—	—	—	—	—	—	—	—	—
		1	A	—	—	—	—	—	—	—	—	—
		1	B	—	—	—	—	—	—	—	—	—
		1	C	—	—	—	—	—	—	—	—	—
		1	D	—	—	—	—	—	—	—	—	—
		1	E	—	—	—	—	—	—	—	—	—
		1	F	—	—	—	—	—	—	—	—	—
	4	2	0	—	—	—	—	—	—	—	—	—
		2	1	—	—	—	—	—	—	—	—	—
		2	2	—	—	—	—	—	—	—	—	—
		2	3	—	—	—	—	—	—	—	—	—
		2	4	—	—	—	—	—	—	—	—	—
		2	5	—	—	—	—	—	—	—	—	—
		2	6	—	—	—	—	—	—	—	—	—
		2	7	—	—	—	—	—	—	—	—	—
RX Amplifier Corner	5	2	8	—	—	—	—	—	—	—	—	—
		2	9	—	—	—	—	—	—	—	—	—
		2	A	—	—	—	—	—	—	—	—	—
		2	B	—	—	—	—	—	—	—	—	—
		2	C	—	—	—	—	—	—	—	—	—
		2	D	—	—	—	—	—	—	—	—	—
		2	E	ManualFilter	M_HP1[1:0]		M_LP1[1:0]		M_HP2[1:0]		M_LP2[1:0]	
		2	F	FilterAdjust	ManFilterSel	EnAutoTune	—	—	Filter_Corner_Coef[3:0]			
AGC_SSI and RX Freq. Tuning	6	3	0	—	—	—	—	—	—	—	—	—
		3	1	—	—	—	—	—	—	—	—	—
		3	2	—	—	—	—	—	—	—	—	—
		3	3	—	—	—	—	—	—	—	—	—
		3	4	—	—	—	—	—	—	—	—	—
		3	5	—	—	—	—	—	—	—	—	—
		3	6	—	—	—	—	—	—	—	—	—
		3	7	Signal indicator	SSI[3:0]				CFTV[3:0]			
	7	3	8	—	—	—	—	—	—	—	—	—
		3	9	—	—	—	—	—	—	—	—	—
		3	A	—	—	—	—	—	—	—	—	—
		3	B	—	—	—	—	—	—	—	—	—
		3	C	—	—	—	—	—	—	—	—	—
		3	D	—	—	—	—	—	—	—	—	—
		3	E	—	—	—	—	—	—	—	—	—
		3	F	—	—	—	—	—	—	—	—	—

Register Details

Sector 0 – Page 0: Command and Status

- **Sector Select Register**

This register is used for sector selection.

Address	Bit	7	6	5	4	3	2	1	0
0x00	Name	—	—	—	—	—	—	—	Sector
	Type	—	—	—	—	—	—	—	R/W
	Reset Value	—	—	—	—	—	—	—	0

Bit 7~1 Unimplemented, read as "0"

Bit 0 **Sector**: Define sector for register page control

- **Command Register**

This register is used for command execution.

Address	Bit	7	6	5	4	3	2	1	0
0x01	Name	Command[7:0]							
	Type	DY							
	Reset Value	0	0	0	0	0	0	0	0

Bit 7~0 **Command[7**:0]: Commands for the device execution

Code	Command
0x00	Idle
0x1A	Transmit
0x16	Receive
0x1E	Transceive
0x12	CalCRC
0x19	LoadKeyFIFO
0x1C	Authent
0x10	RxFilterTune
0x20	LFOTune
0x21	ADCCalibrate
0x22	CardDetect
0x23	FieldDetect
0x31	ReadSignature

- **FIFOData Register**

This register is the input and output channel for the 64-byte FIFO.

Address	Bit	7	6	5	4	3	2	1	0
0x02	Name	FIFOData[7:0]							
	Type	DY							
	Reset Value	x	x	x	x	x	x	x	x

"x": Unknown

Bit 7~0 **FIFOData[7:0]**: Input and output channel for transmission, reception and key initialization.

• PrimaryStatus Register

This register contains flags for indicating the status of modem, interrupt and FIFO.

Address	Bit	7	6	5	4	3	2	1	0
0x03	Name	—	ModemState[2:0]			IRQ	ERR	HiAlert	LoAlert
	Type	—	R			R	R	R	R
	Reset Value	—	0	0	0	0	1	0	1

Bit 7 Unimplemented, read as "0"

Bit 6~4 **ModemState[2:0]**: Indicate the state of RX, TX and FIFO

000: Idle – No operation, neither the transmitter nor the receiver is in operation

001: TxSOF – The transmitter is transmitting "Start of Frame" pattern

010: TxData – The transmitter is transmitting data from FIFO or CRC

011: TxEOF – The transmitter is transmitting "End of Frame" pattern

100: RxPrepare – Receiver circuitry is initialized at this state and wait for time period defined by the RxWait and BitPhase bits before starting to receive data

101: RxAwaiting – The receiver starts and is waiting for RX Start of Frame from tag

110: Receiving – The receiver is receiving data

Bit 3 **IRQ**: Interrupt request indication

If there are one or more interrupt requests in InterruptFlag register, the IRQ flag will be set to 1.

Bit 2 **ERR**: Error indication

If one or more errors occur in the Error register (Sector0-0x0A), the ERR flag will be set to 1.

Bit 1 **HiAlert**: FIFO HiAlert warning flag

If FIFOLength ≥ 64-Waterlevel, the HiAlert flag will be set to 1.

Bit 0 **LoAlert**: FIFO LoAlert warning flag

If FIFOLength ≤ Waterlevel, the LoAlert flag will be set to 1.

• FIFOLength Register

This register indicates the number of data remaining in the FIFO buffer.

Address	Bit	7	6	5	4	3	2	1	0
0x04	Name	—	FIFOLength[6:0]						
	Type	—	R						
	Reset Value	—	0	0	0	0	0	0	0

Bit 7 Unimplement, read as "0"

Bit 6~0 **FIFOLength[6:0]**: Indicates the number of data remaining in the FIFO buffer

• SecondaryStatus Register

This register contains the status flags and values related to timers, CRC and receiver status.

Address	Bit	7	6	5	4	3	2	1	0
0x05	Name	Trunning	RF_Det	CRCReady	EMD_Det	SubC_Det	RxLastBit[2:0]		
	Type	R	R	R	R	R	R		
	Reset Value	0	0	1	0	0	0	0	0

Bit 7 **Trunning**: Timer running state indication

If Timer is running, Trunning will be set to 1. The value in TimerValue register decreases at the rate of timer clock, prescaling from 13.56MHz by TPreScaler bit field.

Bit 6 **RF_Det**: RF field detection indication

RF_Det being set to 1 indicates that external RF field level is higher than threshold level after execute FieldDetect command or WkUpCD Power Saving Mode.

Bit 5 **CRCReady**: CRC ready indication

CRCReady being set to 1 indicates that the CRC co-processor is in idle state and ready to operate.

Bit 4 **EMD_Det**: EMD detection indication

The EMD_Det will be set to 1 if the reader system suppresses a frame that falls in EMD criteria. This indicator bit is active when control bit EMD_Suppress (Sector0-0x1F.1) is enabled and is automatically cleared during "RxAwaiting" state.

Bit 3 **SubC_Det**: Subcarrier detection indication

The SubC_Det is set to 1 when preamble or SOF is detected. In case of BPSK coding, SubC_Det asserts when preamble is detected. In case of Manchester and FSK coding, SubC_Det asserts when SOF is detected. This bit is automatically cleared during "RxAwaiting" state.

Bit 2~0 **RxLastBit[2:0]**: Indicates the number of valid bits in the last received byte

RxLastBit displays the number of valid bits in the last received byte in the bit-oriented frame response. If RxLastBit is zero, the last received byte is complete and valid.

- **InterruptEnable Register**

This register is used for interrupt enable control.

Address	Bit	7	6	5	4	3	2	1	0
0x06	Name	SetIEn	CDIEn	TimerIEn	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn
	Type	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset Value	0	0	0	0	0	0	0	0

Bit 7 **SetIEn**: Interrupt enable setup

SetIEn is a mask bit used in setting and resetting interrupt enable bits. Setting this bit to 1 makes the interrupt enable bits, which are written with 1, set. While clearing this bit to 0 makes the interrupt enable bits, which are written with 1, cleared.

E.g. Writing 7F to this interruptEnable register clears all interrupt enable bits.

Writing FF to this interruptEnable register sets all interrupt enable bits.

Bit 6 **CDIEn**: Card detection interrupt enable

If this bit is set to 1, the card detection interrupt request (CDIRq) will be sent to pin IRQ.

Bit 5 **TimerIEn**: Timer interrupt enable

If this bit is set to 1, the timer interrupt request (TimerIRq) will be sent to pin IRQ.

Bit 4 **TxIEn**: Transmitter interrupt enable

If this bit is set to 1, the transmitter interrupt request (TxIRq) will be sent to pin IRQ.

Bit 3 **RxIEn**: Receiver interrupt enable

If this bit is set to 1, the receiver interrupt request (RxIRq) will be sent to pin IRQ.

Bit 2 **IdleIEn**: Idle interrupt enable

If this bit is set to 1, the idle interrupt request (IdleIRq) will be sent to pin IRQ.

Bit 1 **HiAlertIEn**: FIFO HiAlert interrupt enable

If this bit is set to 1, the FIFO HiAlert interrupt request (HiAlertIRq) will be sent to pin IRQ.

Bit 0 **LoAlerIEn**: FIFO LoAlert interrupt enable

If this bit is set to 1, the FIFO LoAlert interrupt request (LoAlertIRq) will be sent to pin IRQ.

- **InterruptRequest Register**

This register contains the interrupt request bits.

Address	Bit	7	6	5	4	3	2	1	0
0x07	Name	SetIRq	CDIRq	TimerIRq	TxIRq	RxIRq	IdleIRq	HiAlertIRq	LoAlertIRq
	Type	W	DY	DY	DY	DY	DY	DY	DY
	Reset Value	0	0	0	0	0	1	0	1

Bit 7 **SetIRq**: Interrupt request setup

SetIRq is a mask bit used in resetting interrupt request bits. Clearing this bit to 0 makes the interrupt request bits, which are written with 1, cleared. Setting this bit to 1 has no effect.

E.g.: Writing 7F to the interruptFlag register clears all interrupt request bits.

Bit 6 **CDIRq**: Card detection interrupt request flag

CDIRq is set to 1 when ADC_Result from Card Detection operation, both direct command or Wake Up Card Detection mode, follows the following conditions

- ADC_Result > CDThreshold_H or
- ADC_Result < CDThreshold_L

Bit 5 **TimerIRq**: Timer interrupt request flag

TimerIRq is set to 1 when the program timer value (13.56MHz) decreases to zero, or counter value of Wake up timer (16.38kHz) decreases to zero, refer to the registers in page 5 of Sector 0 for details.

Bit 4 **TxIRq**: Transmitter interrupt request flag

TxIRq is set to 1 when one of these events occurs:

- Transmit Command: All data have been transmitted
- Transceive Command: All data have been transmitted
- CalCRC Command: All data have been processed
- LoadKeyFIFO Command: Key is already in the buffer

Bit 3 **RxIRq**: Receiver interrupt request flag

RxIRq is set to 1 when the receiver finishes receiving, which can be one of these events:

- Transceive Command: All data have been received
- Receiver Command: All data have been received

Or in Field Detection operation, both direct command or Wake Up Card Detection mode, follows this condition

- ADC_Result > FDThreshold_H, which refers to FDIRq of system.

Bit 2 **IdleIRq**: Idle interrupt request flag

IdleIRq is set to 1 when the operation of command is finished and the state is changed to idle. End of operation of all commands causes the IdleIRq being set to 1. Setting power down, standby or Idle command does not set IdleIRq.

Bit 1 **HiAlertIRq**: FIFO HiAlert interrupt request flag

HiAlertIRq is set to 1 when FIFOLength > 64 - WaterLevel

Bit 0 **LoAlertIRq**: FIFO LoAlert interrupt request flag

LoAlertIRq is set to 1 when FIFOLength < WaterLevel

Sector 0 – Page 1: Control and Status

• Control Register

This register contains the control bits for all operation of reader system.

Address	Bit	7	6	5	4	3	2	1	0
0x09	Name	—	WkUpCD	StandBy	PowerDown	Crypto_MOn	TStopNow	TStartNow	FlushFIFO
	Type	—	DY	DY	DY	DY	W	W	W
	Reset Value	—	0	0	0	0	0	0	0

Bit 7 Unimplemented, read as "0"

Bit 6 **WkUpCD**: Wake Up Card Detection Mode control

Setting this bit to 1 enables Wake Up Card Detection Mode. The device automatically changes mode between Sleep Mode, which is low power mode, and Active Mode that turn on RF field and measure RF amplitude.

Bit 5 **Standby**: Standby Mode control

Setting this bit to 1 enters the Standby mode. In this mode, the oscillator is still running. All current consuming blocks are turned off.

Bit 4 **PowerDown**: Soft Power Down Mode control

Setting this bit to 1 enters the Soft Power Down mode. In this mode, the oscillator is turned off and all current consuming blocks are turned off.

Bit 3 **Crypto_MOn**: Crypto_M engine control

If Crypto_MOn is set to 1, the crypto engine will be switched on and the RF communication will be encrypted. Crypto_MOn is set to 1 only if the authentication process is successful. This bit can be cleared by external control.

Bit 2 **TStopNow**: Timer immediate stop control

Setting this bit to 1 stops the program timer (13.56MHz) immediately. Reading result from this bit is always 0.

Bit 1 **TStartNow**: Timer immediate start control

Setting this bit to 1 starts the program timer (13.56MHz) immediately. Reading result from this bit is always 0.

Bit 0 **FlushFIFO**: Flush FIFO

If this bit is set to 1, the FIFO read/write-pointer and the FIFOOvf flag will be cleared as well as the FIFOLength will become to zero. Reading result from this bit is always 0.

• Error Register

This register contains error flags for the last executed command.

Address	Bit	7	6	5	4	3	2	1	0
0x0A	Name	—	KeyErr	—	FIFOOvf	CRCErr	FramingErr	ParityErr	CollErr
	Type	—	R	—	R	R	R	R	R
	Reset Value	—	1	—	0	0	0	0	0

Bit 7 Unimplemented, read as "0"

Bit 6 **KeyErr**: Key format error

KeyErr will be set to 1 if the key format in the key buffer is incorrect. As the key buffer is not initialized, KeyErr is set after reset.

Bit 5 Unimplemented, read as "0"

Bit 4 **FIFOOvf**: FIFO overflow flag

FIFOOvf will be set to 1 if FIFO is written from the external microprocessor or the state machine while FIFO is full. FIFOOvf is cleared when FIFO is flushed.

Bit 3 **CRCErr**: CRC error

CRCErr will be set to 1 if RxCRCEn is set and the comparison between received CRC and calculated CRC giving a mismatched result. CRCErr is automatically cleared to 0 every time the receiver starts to receive.

Bit 2 **FramingErr**: Framing error

FramingErr will be set to 1 if the received frame format does not conform to the defined protocol. FramingErr is automatically cleared to 0 every time the receiver starts to receive.

Bit 1 **ParityErr**: Parity error

ParityErr will be set to 1 if the parity check has failed. ParityErr is automatically cleared to 0 every time the receiver starts to receive.

Bit 0 **CollErr**: Collision error

CollErr will be set to 1 if the bit-collision in ISO14443A and ISO15693 is detected. CollErr is automatically cleared to 0 every time the receiver starts to receive.

• CollPos Register

This register indicates the bit collision position.

Address	Bit	7	6	5	4	3	2	1	0
0x0B	Name	CollPos[7:0]							
	Type	R							
	Reset Value	0	0	0	0	0	0	0	0

Bit 7~0 **CollPos[7:0]**: Collision position

0x00: the bit collision occurs at the start bit

0x01: the bit collision occurs at the 1st bit

0x0A: the bit collision occurs at the 10th bit

CollPos indicates the bit position of the first detected collision in a received frame. For receving frame with parity, ISO14443A, if the collision occurred at parity position, CollPos value is not increased, it will display the last uncollision bit. Refer to the "Collision Detection" chapter for more details.

• TimerValue Register

This register contains the timer counter value.

Address	Bit	7	6	5	4	3	2	1	0
0x0C	Name	TimerValue[7:0]							
	Type	R							
	Reset Value	1	1	1	1	1	1	1	1

Bit 7~0 **TimerValue[7:0]**: Timer counter value

• CRCResultLSB Register

This register contains the CRC result.

Address	Bit	7	6	5	4	3	2	1	0
0x0D	Name	CRCResultLSB[7:0]							
	Type	R							
	Reset Value	0	1	1	0	0	0	1	1

Bit 7~0 **CRCResultLSB[7:0]**: The least significant byte of the CRC result

The value of this register is valid only if the CRCReady bit is set to 1.

- **CRCResultMSB Register**

This register contains the CRC result.

Address	Bit	7	6	5	4	3	2	1	0
0x0E	Name	CRCResultMSB[7:0]							
	Type	R							
	Reset Value	0	1	1	0	0	0	1	1

Bit 7~0 **CRCResultMSB[7:0]**: The most significant byte of the CRC result

The value of this register is valid only if the CRCReady bit is set to 1.

- **BitFraming Register**

This register is used to control the bit framing input/output for transmission/reception of the bit-oriented frame.

Address	Bit	7	6	5	4	3	2	1	0
0x0F	Name	—	RxAlign[2:0]			—	TxLastBits[2:0]		
	Type	—	DY			—	DY		
	Reset Value	—	0	0	0	—	0	0	0

Bit 7 Unimplemented, read as "0"

Bit 6~4 **RxAlign[2:0]**: Define the first received bit position in the first received byte

RxAlign is used to define the position of the first received data bit to be stored in the first received byte in the bit oriented frame in ISO14443A. RxAlign is automatically cleared after the reception has finished in Transceive and Receive commands.

Bit 3 Unimplemented, read as "0"

Bit 2~0 **TxLastBits[2:0]**: Define the number of bits of the last byte to be transmitted

TxLastBits is used to define the number of bits of the last byte to be transmitted in the bit oriented frame in ISO14443A. The value "000" is used to define the whole last byte that will be transmitted. This bit field is automatically cleared after the transmission has finised in Transceive and Transmit commands.

Sector 0 – Page 2: TX and Coder

- **TxControl Register**

This register is used to control the logical behaviour of the transmitter driver on pin TX1 and TX2.

Address	Bit	7	6	5	4	3	2	1	0
0x11	Name	Tx1Inv	ModulatorSource[1:0]		100ASK	Tx2Inv	Tx2Cw	Tx2RFEn	Tx1RFEn
	Type	R/W	R/W		R/W	R/W	R/W	R/W	R/W
	Reset Value	0	0	0	1	1	0	0	0

Bit 7 **Tx1Inv**:

If this bit is set to 1, TX1 will deliver an inverted 13.56MHz carrier.

Bit 6~5 **ModulatorSource[1:0]**: Select source for Coder input

00: Tri-state

01: High

10: Internal Coder

11: Pin TD

Bit 4 **100ASK**:

Setting this bit to 1 forces a 100% ASK Modulation, independent from the TxCfgMod value in the register 0x13.

For ISO14443A and ISO15693 (100% modulation index), this bit should be set to 1.

Bit 3 **Tx2Inv**:

If this bit is set to 1, TX2 will deliver an inverted 13.56MHz carrier.

Bit 2 **Tx2Cw**:

0: TX2 delivers a modulated 13.56MHz carrier

1: TX2 continuously delivers an un-modulated 13.56MHz carrier

Bit 1 **Tx2RFEn**:

0: TX2 drives a constant following Tx2Inv

1: TX2 delivers a 13.56MHz carrier

Bit 0 **Tx1RFEn**:

0: TX1 drives a constant following Tx1Inv

1: TX1 delivers a 13.56MHz carrier

- **TxCfgCW Register**

This register is used to configure TX1 and TX2 output conductance in the un-modulation state.

Address	Bit	7	6	5	4	3	2	1	0
0x12	Name	—	—	TxCfgCW[5:0]					
	Type	—	—	R/W					
	Reset Value	—	—	1	1	1	1	1	1

Bit 7~6 Unimplemented, read as "0"

Bit 5~0 **TxCfgCW[5:0]**: Define TX1 and TX2 output conductance in the un-modulation state

- **TxCfgMod Register**

This register is used to configure TX1 and TX2 output conductance in the modulation state.

Address	Bit	7	6	5	4	3	2	1	0
0x13	Name	—	—	TxCfgMod					
	Type	—	—	R/W					
	Reset Value	—	—	0	1	0	0	0	0

Bit 7~6 Unimplemented, read as "0"

Bit 5~0 **TxCfgMod[5:0]**: Define TX1 and TX2 output conductance in the modulation state

This bit field is used to regulate the output power during the modulation state (low level field of ENV). If the 100ASK bit is set to 1, the value of TxCfgMod will have no effect.

- **CoderControl Register**

This register is used to set the coder rate and the coding mode.

Address	Bit	7	6	5	4	3	2	1	0
0x14	Name	Send1Pulse	—	CoderRate[2:0]			TxCoding[2:0]		
	Type	R/W	—	R/W			R/W		
	Reset Value	0	—	0	1	1	0	0	1

Bit 7 **Send1Pulse**:

Setting this bit to 1 forces a generation of the only one modulation pulse to switch to the next TimeSlot in conjunction with an Inventory command in ISO15693. As this bit is not cleared automatically, it has to be reset to 0 manualy.

Bit 6 Unimplemented, read as "0"

Bit 5~3 **CoderRate[2:0]**: Configure coder rate

000: 848kbps for ISO14443A

001: 424kbps for ISO14443A; 848kbps for ISO14443B

010: 212kbps for ISO14443A; 424kbps for ISO14443B

011: 106kbps for ISO14443A; 212kbps for ISO14443B

100: 106kbps for ISO14443B

101: ISO15693

11x: Reserved

Bit 2~0 **TxCoding[2:0]**: Define the bit coding and framing during transmission

000: NRZ for ISO14443B

001: Miller Coded for ISO14443A

01x: Reserved

10x: Reserved

110: ISO15693 standard mode (1 of 256 Coding)

111: ISO15693 fast mode (1 of 4 Coding)

- **ModWidth Register**

This register is used to setup the modulation pulse width.

Address	Bit	7	6	5	4	3	2	1	0
0x15	Name	ModWidth[7:0]							
	Type	R/W							
	Reset Value	0	0	0	0	1	1	1	1

Bit 7~0 **ModWidth[7:0]**: Define the pulse width of the modulation pulse in the transmitted bit

Modulation width=2(ModWidth+1)/fc

For example:

ISO14443A@106k: 0x0F (Modulation width=2.36μs);

ISO15693: 0x3F (Modulation width=9.44μs)

This register is not affected if TxCoding is set to NRZ for ISO14443B.

- **ModWidthSOF Register**

This register is used to setup the modulation pulse width in SOF.

Address	Bit	7	6	5	4	3	2	1	0
0x16	Name	ModWidthSOF[7:0]							
	Type	R/W							
	Reset Value	0	0	0	0	1	1	1	1

Bit 7~0 **ModWidthSOF[7:0]**: Define the pulse width in Start of Frame

This bit field is used to define the pulse width of the modulation pulse in Start of Frame in the transmitted telegram.

Modulation width=2(ModWidthSOF+1)/fc

For example,

ISO14443A: 0x0F (Modulation width in SOF=2.36μs)

ISO15693: 0x3F (Modulation width in SOF=9.44μs)

This register is not affected if TxCoding is set to NRZ for ISO14443B.

- **TypeBTxFraming Register**

This register is used to difine framing for ISO14443B transmission.

Address	Bit	7	6	5	4	3	2	1	0
0x17	Name	NoTxSOF	NoTxEOF	EOFWidth	CharSpacing[2:0]			SOFWidth[1:0]	
	Type	R/W	R/W	R/W	R/W			R/W	
	Reset Value	0	0	1	1	1	0	1	1

Bit 7 **NoTxSOF**:
If this bit is set to 1, the SOF will be omitted from the transmitted framing.

Bit 6 **NoTxEOF**:
If this bit is set to 1, the EOF will be omitted from the transmitted framing.

Bit 5 **EOFWidth**: Setup the length of EOF
0: 10 ETU
1: 11 ETU

Bit 4~2 **CharSpacing[2:0]**:
This bit field is used to setup the length of EGT between 0 and 7 ETU when transmitted.

Bit 1~0 **SOFWidth[1:0]**: Define SOF pattern in ISO14443B
00: 10 ETU low and 2 ETU high
01: 10 ETU low and 3 ETU high
10: 11 ETU low and 2 ETU high
11: 11 ETU low and 3 ETU high

Sector 0 – Page 3: RX and Decoder

- **RxControl1 Register**

This register is used to control the receiver behaviours.

Address	Bit	7	6	5	4	3	2	1	0
0x19	Name	SubCPulses[2:0]			SubCCarrier[1:0]		LP_Off	Gain[1:0]	
	Type	R/W			R/W		R/W	R/W	
	Reset Value	0	1	1	0	1	0	1	1

Bit 7~5 **SubCPulses[2:0]**: Define the number of subcarrier pulses per bit
000: 1 Pulse – ISO14443A & 43B @ 848k
001: 2 Pulses – ISO14443A & 43B @ 424k
010: 4 Pulses – SO14443A & 43B @ 242k
011: 8 Pulses – ISO14443A & 43B @ 106k; ISO15693 @ 53k
100: 16 Pulses – ISO15693 @ 26k; ICODE1
101: 32 Pulses – ISO15693 @ 13k
110: 64 Pulses – ISO15693 @ 6.7k
111: Reserved

Bit 4~3 **SubCCarrier[1:0]**: Define the number of carrier clocks used in subcarrier
00: 8 Clks
01: 16 Clks – ISO14443A & ISO14443B
10: 32 Clks – ISO15693
11: 64 Clks

Bit 2 **LP_Off**: Lowpass filters off control
This bit is set to switch off all Lowpass filters to extend the incoming signal bandwidth.

Bit 1~0 **Gain[1:0]**: Define gain of the Amplifier manually when the AGC is turned off (AGCEn=0)

00: 12dB (4x)

01: 24dB (16x)

10: 36dB (64x)

11: 48dB (250x)

• DecoderControl Register

This register is used to control the decoder behaviours.

Address	Bit	7	6	5	4	3	2	1	0
0x1A	Name	RxMultiple	CollMarkVal	ZeroAfterColl	RxFraming[1:0]		—	RxCoding[1:0]	
	Type	R/W	R/W	R/W	R/W		—	R/W	
	Reset Value	0	0	0	0	1	—	0	0

Bit 7 **RxMultiple**:

If this bit is set to 1, system can execute consecutive reception without issuing Receive command. Every received data and its associated error register bit value, even if there is no error, are saved to FIFO. Every end of reception, RX interrupt is asserted. To quit the reception, Idle command must be issued to the Command register. This command is applicable for both Transceive and Receive command.

Bit 6 **CollMarkVal**:

If this bit is set to 1, the collided bit will be set to the value defined by CollMarkVal. This feature helps resolving anti-collision procedure for ISO14443A.

Bit5 **ZeroAfterColl**:

If this bit is set to 1, all received bits after the collided bit will be marked to zero. Otherwise, the data are recorded as decoder received. This feature eases resolving anti-collision procedure for ISO14443A.

Bit 4~3 **RxFraming[1:0]**: Define the Decoder Framing

00: Reserved

01: ISO14443A

10: ISO15693, I-CODE2-SLI

11: ISO14443B

Bit 2 Unimplemented, read as "0"

Bit 1~0 **RxCoding[1:0]**: Define receiving patterns for the decoder

00: Manchester (ISO14443A – 106 kbps; ISO15693 – 1 subcarrier)

01: BPSK (ISO14443A – higher rate: 212, 424, 848kbps; ISO14443B)

10: FSK (ISO15693 – 2 subcarriers)

11: Reserved

• BitPhase Register

This register is used to define the phase relation between TX EOF and RX SOF.

Address	Bit	7	6	5	4	3	2	1	0
0x1B	Name	BitPhase[7:0]							
	Type	R/W							
	Reset Value	0	0	1	1	1	1	0	1

Bit 7 **BitPhase[7:0]**: Define the fractional guard time of the decoder in the unit of clock

This register should be set in addition to RxWait, which is used for starting.

Note: The correct value of this register is essential for proper operation.

- **RxThreshold Register**

This register is used to define a threshold of the bit decoder from the correlator.

Address	Bit	7	6	5	4	3	2	1	0
0x1C	Name	MinLevel[2:0]			—	CollLevel[2:0]			—
	Type	R/W			—	R/W			—
	Reset Value	1	0	1	—	1	0	1	—

Bit 7~5 **MinLevel[2:0]**:

This bit field is used to define the minimum signal strength at the decoder input that shall be accepted. If the signal strength is below this level, it is evaluated as an invalid bit. The signal strength is relatively measured to the following working ranges. (8 steps in the design).

000: 2/72 of V_{DD}

001: 3/72 of V_{DD}

010: 4/72 of V_{DD}

011: 5/72 of V_{DD}

100: 6/72 of V_{DD}

101: 7/72 of V_{DD}

110: 8/72 of V_{DD}

111: 9/72 of V_{DD}

Bit 4 Unimplemented, read as "0"

Bit 3~1 **CollLevel[2:0]**:

This bit field is used to define the minimum signal strength at the decoder input that has to be reached by the weaker half-bit of the Manchester and FSK-coded signal to generate the bit-collision, which is relative to the amplitude of the stronger half-bit. (8 steps in design).

000: 1/9 of stronger half-bit

001: 2/9 of stronger half-bit

010: 3/9 of stronger half-bit

011: 4/9 of stronger half-bit

100: 5/9 of stronger half-bit

101: 6/9 of stronger half-bit

110: 7/9 of stronger half-bit

111: 8/9 of stronger half-bit

Bit 0 Unimplemented, read as "0"

- **BPSKDemControl Register**

This register is used to define the RX framing and decoding control for ISO14443B.

Address	Bit	7	6	5	4	3	2	1	0
0x1D	Name	NoRxSOF	NoRxEGT	NoRxEOF	HP2Off	TauD[1:0]		AGCEn	TauAGC
	Type	R/W	R/W	R/W	R/W	R/W		R/W	R/W
	Reset Value	0	0	0	0	0	1	0	0

Bit 7 **NoRxSOF**:

0: A missing SOF generates a framing error

1: A missing SOF will be ignored and no framing error is reported

Bit 6 **NoRxEGT**:

0: The number of EGT not conforming to the standard generates a framing error

1: The number of EGT not conforming to the standard will be ignored and no framing error is reported

Bit 5 **NoRxEOF**:

0: A missing EOF generates a framing error

1: A missing EOF will be ignored and no framing error is reported

Bit 4 **HP2Off**:

If this bit is set to 1, the 2nd highpass filter will be switched off.

Bit 3~2 **TauD[1:0]**: Define the time constant of the internal PLL during the data receiving phase

00: 4 pulses, lock-in 10 pulses

01: 8 pulses, lock-in 22 pulses

10: 16 pulses, lock-in 44 pulses

11: 32 pulses, lock-in 88 pulses

Bit 1 **AGCEn**: AGC function enable control

0: The amplifier gain is defined by Gain[1:0]

1: The amplifier gain is controlled by the AGC to establish the amplified output signal in a working range

Bit 0 **TauAGC**: Define the time constant of the AGC

0: Hi-Speed (1 subcarrier) (The subcarrier is set by SubCCarrier in the RxControl1)

1: Lo-Speed (2 subcarriers) (The subcarrier is set by SubCCarrier in the RxControl1)

- **RxControl2 Register**

This register is used for decoder source selection and additional control for receiver.

Address	Bit	7	6	5	4	3	2	1	0
0x1E	Name	Cont_Int	RxAutoPD	—	—	Reserved	ByPassEnv	Reserved	DecoderSrc
	Type	R/W	R/W	—	—	R/W	R/W	R/W	R/W
	Reset Value	0	1	—	—	0	0	0	1

Bit 7 **Cont_Int**:

0: The correlator gain equals to 1

1: The correlator gain in the receiver is boosted by 4x for ISO15693 low data rate (6.67kbps)

Bit 6 **RxAutoPD**: Receiver auto power down control

0: The receiver is always activated

1: The receiver circuit is automatically switched on before receiving and switched off after receiving. This option can be used to reduce current consumption.

Bit 5~4 Unimplemented, read as "0"

Bit 3 Reserved bit for internal setting, this bit must be fixed at "0" and can not be modified

Bit 2 **ByPassEnv**: Select types of analog input signals presenting at RX pin for extended range applications

0: Pin RX receives a 13.56MHz carrier-modulated signal (An Internal Envelope detector is employed)

1: Pin RX receives a carrier-demodulated signal (An Internal Envelope detector is bypassed)

Bit 1 Reserved bit for internal setting, this bit this bit must be fixed at "0" and can not be modified

Bit 0 **DecoderSrc**: Select input signals for internal decoders (Only for BPSK pattern)

0: External signal through pin TD

1: Internal Demodulator

- **RxControl3 Register**

This register is used to control the receiver behaviours.

Address	Bit	7	6	5	4	3	2	1	0
0x1F	Name	BPSKDecMeth	BPSKDataRec	SOFSel15693	—	—	—	EMD_Suppress	SOF43A_5Bits
	Type	R/W	R/W	R/W	—	—	—	R/W	R/W
	Reset Value	1	0	1	—	—	—	0	0

Bit 7 **BPSKDecMeth**: Define the BPSK Decoding Method

0: Adaptive Framing

1: Digital Correlator

Refer to the "BPSK Bit Decoder" section for more details.

Bit 6 **BPSKDataRec**: BPSK Data Recognition Function control

0: Disable

1: Enable

If this bit is set to 1, the BPSK Data Recognition block will be enabled. It improves BPSK data reception especially in case of noisy or antenna detuning. This option can be applied in ISO14443A higher rate and ISO14443B.

Bit 5 **SOFSel15693**: Define the method of ISO15693 header recognition

0: Disable

1: Enable running window to search for SOF

If this bit is set to 1, system will use the running window method to search for a matched pattern of 4 valid bits of SOF. If there is a combination pattern like SOF but contain some invalid bits, system will continue to search for next valid SOF and will be still in "Receiving" state. If it is cleared to 0, system will quit the "Receiving" state with error reporting this occurrence. This bit increases noise immunity in most cases. This option is recommended in both normal case and especially receiving write response in which response time is quite long and there is significant probability to find noise pattern similar to the SOF.

Bit 4~2 Unimplemented, read as "0"

Bit 1 **EMD_Suppress**: EMD frame suppression control

0: Disable

1: Enable the EMD frame suppression

Setting this bit to 1 can enable the EMD frame suppression. This option is applicable for ISO14443A and ISO14443B only. The condition for EMD suppression is that the number of data byte < 3 bytes and there is at least an error in reception frame. This frame will be neglected and not send to FIFO. Refer to the "EMD Suppression" section for more details.

Bit 0 **SOF43A_5Bits**: Define the ISO14443A SOF condition

0: Only 1 valid SOF bit will be sufficient condition to treat the incoming frame valid

1: At least consecutive 5 valid bits will be sufficient condition to treat the incoming frame valid. The 5 valid bits are SOF and 4-bits data

Sector 0 – Page 4: RF-Timing, Channel Redundancy and ADC Control

- **Reserved Register**

This register is reserved for internal settings.

Address	Bit	7	6	5	4	3	2	1	0
0x20	Name	Reserved							
	Type	R/W							
	Reset Value	0	0	0	0	1	0	1	0

Bit 7~0 Reserved bits for internal settings. For proper operation, the register content must be fixed at "0000_1010" and can not be modified

- **RxWait Register**

This register is used to define the guard time from TX EOF to the start of receiving the timing for the receiver.

Address	Bit	7	6	5	4	3	2	1	0
0x21	Name	RxWait[7:0]							
	Type	R/W							
	Reset Value	0	0	0	0	0	1	1	0

Bit 7~0 **RxWait[7:0]**:

The RxWait defines the guard time between the TX EOF and the start of receiving of the decoder in the unit of one-bit duration. This will increase receiving capability especially in noisy environment. The one-bit duration unit is defined from SubCPulses and SubCCarrier in the RxControl1 register. For example, in ISO14443A @ 106kbps, the RxWait should be set to 0x06.

- **ChannelRedundancy Register**

This register is used to setup the CRC and Parity check for receiving data.

Address	Bit	7	6	5	4	3	2	1	0
0x22	Name	—	MSBFirst	CRC3309	CRC8	RxCRCEn	TxCRCEn	ParityOdd	ParityEn
	Type	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset Value	—	0	0	0	0	0	1	1

Bit 7 Unimplemented, read as "0"

Bit 6 **MSBFirst**:

If this bit is set to 1, the MSB bit in data frame will be the first bit used for CRC calculation.

Bit 5 **CRC3309**:

If this bit is set to 1, the CRC-calculation will be executed according to ISO/IEC3309 for ISO14443B and ISO15693.

Bit 4 **CRC8**:

0: 16-bit CRC is calculated

1: 8-bit CRC is calculated

Bit 3 **RxCRCEn**:

0: No CRC is expected at the end of the received frame

1: The last byte of the received frame is interpreted as the CRC byte

Bit 2 **TxCRCEn**:

0: No CRC is appended and transmitted

1: The CRC is calculated for the transmitted frame and appended to the end of the transmitted data

Bit 1 **ParityOdd**:

0: Even parity is calculated and compared with the received frame

1: Odd parity is calculated and compared with the received frame

Bit 0 **ParityEn**:

0: No parity bit is inserted or expected (ISO14443B and ISO15693)

1: The parity is inserted in the transmitted data stream at the end of each byte and expected in the received data stream (ISO14443A)

• CRCPresetMSB Register

This register contains the most significant byte of the 16-bit preset value of the CRC Register.

Address	Bit	7	6	5	4	3	2	1	0
0x23	Name	CRCPresetMSB[7:0]							
	Type	R/W							
	Reset Value	0	1	1	0	0	0	1	1

Bit 7~0 **CRCPresetMSB[7:0]**: The most significant byte of the CRC preset value

• CRCPresetLSB Register

This register contains the least significant byte of the 16-bit preset value of the CRC Register.

Address	Bit	7	6	5	4	3	2	1	0
0x24	Name	CRCPresetLSB[7:0]							
	Type	R/W							
	Reset Value	0	1	1	0	0	0	1	1

Bit 7~0 **CRCPresetLSB[7:0]**: The least significant byte of the CRC preset value

• ADCCtrl Register

This register is used to setup the ADC control for field detection and card detection operation.

Address	Bit	7	6	5	4	3	2	1	0
0x25	Name	—	—	ADC_Delay[1:0]		FD_MinLvl	ADC_FastMode	ADC_Rsln	Reserved
	Type	—	—	R/W		R/W	R/W	R/W	R/W
	Reset Value	—	—	1	0	0	0	1	1

Bit 7~6 Unimplemented, read as "0"

Bit 5~4 **ADC_Delay[1:0]**: Define ADC delay time

00: 76μs

01: 151μs

10: 227μs

11: 302μs

This bit field is used to define delay time for starting ADC conversion after all related analog circuits are enabled. Refer to the "RF Amplitude Detector System" section for details.

Bit 3 **FD_MinLvl**: Define step size of ADC in Field Detection operation

0: 7 bits – 10.6mV when ADC_Rsln="0"; 8 bits – 5.3mV when ADC_Rsln="1"

1: ADC is internally configured to 8 bits with 2.7mV resolution

This bit is used for additional configure of ADC resolution in Field Detection operation. Refer to the "RF Amplitude Detector System" section for details.

Bit 2 **ADC_FastMode**: Define the ADC mechanism and timing for conversion

0: Normal operation

1: Fast operation

If this bit is set to 1, the fast mode will be enabled, in which the conversion time can be reduced, however the resolution is maintained. The ADC circuit is internally configured to 8-bit resolution when this bit is set. Refer to the "RF Amplitude Detector System" section for more details.

Bit 1 **ADC_Rsln**: ADC resolution setup

0: 7 bits – 10.6mV

1: 8 bits – 5.3mV

This bit is used to configure the ADC resolution which defines RF amplitude input at RX pin, Refer to the "RF Amplitude Detector System" section for more details. The defined resolution is based on RF input signal which is in phase with internal clock and ADC_FullscaleAdj (Sector1-0x05.[1:0])="00".

Bit 0 Reserved bit for internal setting, this bit must be fixed at "1" and can not be modified

- **ADC_Result_I Register**

This register contains the ADC conversion output, I-phase, in phase with reference clock.

Address	Bit	7	6	5	4	3	2	1	0
0x26	Name	ADC_Result_I[7:0]							
	Type	R							
	Reset Value	0	0	0	0	0	0	0	0

Bit 7~0 **ADC_Result_I[7:0]**: ADC Conversion output, I – phase, which defines RF amplitude at pin RX from FieldDetect and CardDetect

- **ADC_Result_Q Register**

This register contains the ADC conversion output, Q-phase, quadrature phase of reference clock.

Address	Bit	7	6	5	4	3	2	1	0
0x27	Name	ADC_Result_Q[7:0]							
	Type	R							
	Reset Value	0	0	0	0	0	0	0	0

Bit 7~0 **ADC_Result_Q[7:0]**: ADC Conversion output, Q – phase, which defines RF amplitude at pin RX from FieldDetect and CardDetect

Sector 0 – Page 5: FIFOLevel, Program Timer and Wake Up Timer

- **FIFOLevel Register**

This register is used to define the level of FIFO for overflow and underflow warning.

Address	Bit	7	6	5	4	3	2	1	0
0x29	Name	—	—	WaterLevel[5:0]					
	Type	—	—	R/W					
	Reset Value	—	—	0	0	1	0	0	0

Bit 7~6 Unimplemented, read as "0"

Bit 5~0 **WaterLevel[5:0]**: Define the level of FIFO for overflow and underflow warnings

- **TimerClock Register**

This register is used to define the input clock to the timer and control the timer reloading.

Address	Bit	7	6	5	4	3	2	1	0
0x2A	Name	—	—	TAutoRestart	TPreScaler[4:0]				
	Type	—	—	R/W	R/W				
	Reset Value	—	—	0	0	0	1	1	1

Bit 7~6 Unimplemented, read as "0"

Bit 5 **TAutoRestart**: Timer auto restart control

0: The timer decreases to zero and the bit TimerIRq is set to 1

1: The program timer automatically restarts and counts down from TReloadValue, instead of counting down to zero

Bit 4~0 **TPreScaler[4:0]**: Define the timer clock (Ftimer)

Ftimer=13.56MHz / ($2^{TPreScaler}$), the value of TPreScaler bit field can be adjusted from 0 to 21.

• TimerControl Register

This register is used to setup the automatic start and stop of timer, which is triggered by events from RF.

Address	Bit	7	6	5	4	3	2	1	0
0x2B	Name	—	—	—	—	TStopRxEnd	TStopRxBegin	TStartTxEnd	TStartTxBegin
	Type	—	—	—	—	R/W	R/W	R/W	R/W
	Reset Value	—	—	—	—	0	1	1	0

Bit 7~4 Unimplemented, read as "0"

Bit 3 **TStopRxEnd**:

0: The end of reception event does not affect the timer

1: The program timer stops automatically after the end of data reception

Bit 2 **TStopRxBegin**:

0: The reception of the 1st valid bit does not affect the timer

1: The program timer stops automatically after the 1st valid bit is received

Bit 1 **TStartTxEnd**:

0: The end of transmission event does not affect the timer

1: The program timer starts automatically after the end of transmission. If the program timer is running, the timer restarts from TReloadValue

Bit 0 **TStartTxBegin**:

0: The transmission of the 1st valid bit does not affect the timer

1: The program timer starts automatically after the 1st valid bit is transmitted. If the program timer is running, the timer restarts from TReloadValue

• TimerReloadValue Register

This register is used to define the timer start value.

Address	Bit	7	6	5	4	3	2	1	0
0x2C	Name	TReloadValue[7:0]							
	Type	R/W							
	Reset Value	0	0	0	0	1	0	1	0

Bit 7~0 **TReloadValue[7:0]**: Define the program timer start value

Note that the value modification will affect the timer in the next round.

• WkTimerControl Register

This register is used to control wake up timer operation and prescaler that used in the WkUpCD mode. It should be noted that SPI writing the WkTStart & WkTStop does not take effect immediately, it will delay for an internal clock of 16.38kHz to start running.

Address	Bit	7	6	5	4	3	2	1	0
0x2D	Name	WkTStartNow	WkTStopNow	WkTRunning	WkTAutoRestart	WkTPreScaler[3:0]			
	Type	W	W	R	R/W	R/W			
	Reset Value	0	0	0	1	1	0	0	1

Bit 7 **WkTStartNow**: Wake up timer immediate start control

Setting this bit to 1 starts the wake up timer (16.38kHz) immediately. Reading result from this bit is always "0".

Bit 6 **WkTStopNow**: Wake up timer immediate stop control

Setting this bit to 1 stops the wake up timer (16.38kHz) immediately. Reading result from this bit is always "0". This bit will be activated when the wake up timer is running.

Bit 5 **WkTRunning**: Wake up timer running state indication

If wake up timer is running, WkTRunning will be set to 1. The Wake Up timer value decreases at the rate of wake up timer clock, prescaling from 16.38kHz by WkTPreScaler.

Bit 4 **WkTAutoRestart**: Wake up timer auto restart control

0: The timer will decrease to zero and the bit TimerIRq is set to 1

1: The wake up timer will automatically restart and count down from WkTReloadValue, instead of counting down to zero

Bit 3~0 **WkTPresScaler[3:0]**: Define the wake up timer clock (Fwk)

Fwk=16.38kHz / ($2^{WkTPreScaler}$), the value of WkTPreScaler can be asjusted from 0 to 12.

- **WkTimerReloadValue Register**

This register is used to define the wake up timer start value.

Address	Bit	7	6	5	4	3	2	1	0
0x2E	Name	WkTReloadValue[7:0]							
	Type	R/W							
	Reset Value	0	0	1	0	0	0	0	0

Bit 7~0 **WkTReloadValue[7:0]**: Define the wake up timer start value

Note that the value modification will affect the timer in the next round. The wake up period in card detection mode, TwkUp, can be defined by the following equation:

TwkUp=WkTReloadValue × ($2^{WkTPreScaler}$) / (16.38kHz).

- **WkTtrigTime Register**

This register is used to define the number of wake up timer underflow counter to generate Timer Interrupt flag.

Address	Bit	7	6	5	4	3	2	1	0
0x2F	Name	—	—	—	—	WkTtrigTime[3:0]			
	Type	—	—	—	—	R/W			
	Reset Value	—	—	—	—	0	1	1	0

Bit 7~4 Unimplemented, read as "0"

Bit 3~0 **WkTtrigTime[3:0]**: Define the number of wake up timer underflow

Equation: TwkIrq=$2^{WkTtrigTime}$ × TwkUp

For Example, if wake up period, TwkUp, is set to 1 second by WkTReloadValue & WkTPreScaler, when WkTtrigTime=3, TimerIRq will be set every 8 seconds.

Sector 0 – Page 6: Field Detection and Card Detection

- **FDControl Register**

This register is used for external RF Field Detection control.

Address	Bit	7	6	5	4	3	2	1	0
0x30	Name	Reserved	FDDetectTime[2:0]			—	—	FDAverage[1:0]	
	Type	R/W	R/W			—	—	R/W	
	Reset Value	0	1	0	0	—	—	0	0

Bit 7 Rserved bit for internal setting, this bit must be fixed at "0" and can not be modified

Bit 6~4 **FDDetectTime[2:0]**: Define the number of detection time, FD_Times, in the Field Detection operation

The equation of the FD_Times is: FD_Times=$2^{FDDetectTime}$, refer to the "RF Amplitude Detector System" section for more details.

Bit 3~2 Unimplemented, read as "0"

Bit 1~0 **FDAverage[1:0]**: Define the average times in each conversion, FD_Ave, in the Field Detection operation

The equation of the FD_Ave is: FD_Times=$2^{FDAverage}$, refer to the "RF Amplitude Detector System" section for more details.

• WkCDControl Register

This register is used for Wake Up Card Detection control.

Address	Bit	7	6	5	4	3	2	1	0
0x31	Name	Reserved	WkCDGoActive	WkIgnoreFD	WkFDEn	Reserved	CDTxDelay	CDAverage[1:0]	
	Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	Reset Value	0	0	0	1	0	1	0	0

Bit 7 Reserved bit for internal setting, this bit must be fixed at "0" and can not be modified

Bit 6 **WkCDGoActive**: Define operation in WkUpCD mode when CDIRq is set

0: The device is still in WkUpCD mode

1: The device is automatically go to active state that ready to execute further operation

Bit 5 **WkIgnoreFD**: Define operation in WkUpCD mode when WkFDEn="1" and RxIRq="1"

0: If external RF field is detected, RxIRq will be set. The device will skip Card Detection operation to prevent RF field collision

1: Card Detection operation still execute even if external RF field is detected

Bit 4 **WkFDEn**: Define operation in WkUpCD mode for Field Detection operation

0: Field Detection operation is disabled

1: Field Detection operation is enabled before Card Detection for preventing RF field collision

Bit 3 Reserved bit for internal setting, this bit must be fixed at "0" and can not be modified

Bit 2 **CDTxDelay**: Define wait time for RF amplitude settle after transmitter is enabled in Card Detection Mode

0: 2.36μs (32/fc)

1: 4.72μs (64/fc)

Bit 1~0 **CDAverage[1:0]**: Define the average times in each coversion, CD_Ave, in the Card Detection operation

CD_Ave=$2^{CDAverage}$, refer to the "RF Amplitude Detector System" section for more details

• FDThreshold_I_H Register

This register is used to setup the threshold level phase I for field detection operation.

Address	Bit	7	6	5	4	3	2	1	0
0x32	Name	FDThreshold_I_H[7:0]							
	Type	R/W							
	Reset Value	0	0	1	0	0	0	0	0

Bit 7~0 **FDThreshold_I_H[7:0]**:

This bit field is used to define threshold level phase I for external RF field, if ADC_Result_I > FDThreshold_I_H, RxIRq will be set when condition is matched following FDIRqCfg.

• FDThreshold_Q_H Register

This register is used to setup the threshold level phase Q for field detection operation.

Address	Bit	7	6	5	4	3	2	1	0
0x33	Name	FDThreshold_Q_H[7:0]							
	Type	R/W							
	Reset Value	0	0	1	0	0	0	0	0

Bit 7~0 **FDThreshold_Q_H[7:0]**:

This bit field is used to define threshold level phase Q for external RF field, if ADC_Result_Q > FDThreshold_Q_H, RxIRq will be set when condition is matched following FDIRqCfg.

• CDThreshold_I_L Register

This register is used to setup the low threshold level phase I for card detection operation.

Address	Bit	7	6	5	4	3	2	1	0
0x34	Name	CDThreshold_I_L[7:0]							
	Type	R/W							
	Reset Value	0	1	0	0	0	0	0	0

Bit 7~0 **CDThreshold_I_L[7:0]**:

This bit field is used to define threshold level phase I for card detection operation, when card is loaded to RF field driven by the device itself. If ADC_Result_I < CDThreshold_I_L or ADC_Result_I > CDThreshold_I_H, CDIRq will be set when condition is matched following CDIRqCfg.

• CDThreshold_I_H Register

This register is used to setup the high threshold level phase I for card detection operation.

Address	Bit	7	6	5	4	3	2	1	0
0x35	Name	CDThreshold_I_H[7:0]							
	Type	R/W							
	Reset Value	1	0	0	0	0	0	0	0

Bit 7~0 **CDThreshold_I_H[7:0]**:

This bit field is used to define threshold level phase I for card detection operation, when card is loaded to RF field driven by the device itself. If ADC_Result_I < CDThreshold_I_L or ADC_Result_I > CDThreshold_I_H, CDIRq will be set when condition is matched following CDIRqCfg.

• CDThreshold_Q_L Register

This register is used to setup the low threshold level phase Q for card detection operation.

Address	Bit	7	6	5	4	3	2	1	0
0x36	Name	CDThreshold_Q_L[7:0]							
	Type	R/W							
	Reset Value	0	1	0	0	0	0	0	0

Bit 7~0 **CDThreshold_Q_L[7:0]**:

This bit field is used to define threshold level phase Q for card detection operation, when card is loaded to RF field driven by the device itself. If ADC_Result_Q < CDThreshold_Q_L, ADC_Result_Q > CDThreshold_Q_H, CDIRq will be set when condition is matched following CDIRqCfg.

- **CDThreshold_Q_H Register**

This register is used to setup the high threshold level phase Q for card detect operation.

Address	Bit	7	6	5	4	3	2	1	0
0x37	Name	CDThreshold_Q_H[7:0]							
	Type	R/W							
	Reset Value	1	0	0	0	0	0	0	0

Bit 7~0 **CDThreshold_Q_H[7:0]**:

This bit field is used to define threshold level phase Q for card detect operation, when card is loaded to RF field driven by the device itself. If ADC_Result_Q < CDThreshold_Q_L, ADC_Result_Q > CDThreshold_Q_H, CDIRq will be set when condition is match following CDIRqCfg.

Sector 0 – Page 7: Test, IO Control and RX Adjustment

- **TDIRqCtrl Register**

This register is used for TD and IRQ pin control.

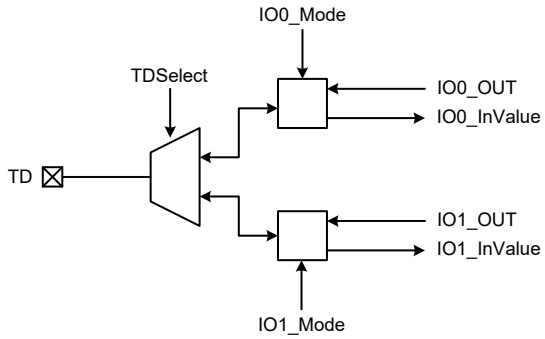
Address	Bit	7	6	5	4	3	2	1	0
0x39	Name	—	—	IO1_InValue	IO0_InValue	TDSelect	IO1_Mode	IO0_Mode	IRqInv
	Type	—	—	R	R	R/W	R/W	R/W	R/W
	Reset Value	—	—	0	0	0	1	1	0

Bit 7~6 Unimplemented, read as "0"

Bit 5 **IO1_InValue**: Return TD pin input value when TDSelect="1" and IO1_Mode="0"

Bit 4 **IO0_InValue**: Return TD pin input value when TDSelect="0" and IO0_Mode="0"

Bit 3 **TDSelect**: Select TD pin function between IO1 and IO0 as shown in following figure "TD pin basic structure"



Bit 2 **IO1_Mode**: Select IO1 signal function

0: Input

1: Output

Bit 1 **IO0_Mode**: Select IO0 signal function

0: Input

1: Output

Bit 0 **IRqInv**:

0: IRQ pin is active high

1: IRQ pin is active low

• Test Register

This register is used for TD and TA pin configuration.

Address	Bit	7	6	5	4	3	2	1	0
0x3A	Name	Reserved	Test[6:0]						
	Type	R/W	R/W						
	Reset Value	0	0	0	0	0	0	0	0

Bit 7 Reserved bit for internal setting, this bit must be fixed at "0" and can not be modified

Bit 6~0 **Test[6:0]**: Test code to bring internal signals to test pin TD and TA

• Reserved Register

This register is reserved for internal settings.

Address	Bit	7	6	5	4	3	2	1	0
0x3B	Name	Reserved							
	Type	R/W							
	Reset Value	1	1	1	1	0	0	0	0

Bit 7~0 Reserved bits for internal settings. For proper operation, the register content must be fixed at "1111_0000" and can not be modified

• Rx43A_Option Register

This register is used to adjust receiving concept for ISO14443A at a rate of 106kbps.

Address	Bit	7	6	5	4	3	2	1	0
0x3C	Name	Reserved	RxCorrIntTime[1:0]		Reserved	SOFSel43A	Reserved		
	Type	R/W	R/W		R/W	R/W	R/W		
	Reset Value	1	0	0	0	1	0	0	0

Bit 7 Reserved bit for internal setting, this bit must be fixed at "1" and can not be modified

Bit 6~5 **RxCorrIntTime[1:0]**:

00: 60fc

01: 56fc

1x: 52fc

This bit field is used to adjust integration time of half bit evaluation in correlator for ISO14443A – Manchester receiving, which is applied for reducing the effect of RX channel distortion. Reducing integration time also decreases sensitivity.

Bit 4 Reserved bit for internal setting, this bit must be fixed at "0" and can not be modified

Bit 3 **SOFSel43A**: Define the method of ISO14443A – Manchester pattern header recognition

0: Disable

1: Enable

This bit is used to define the method of ISO14443A – Manchester pattern header recoginition. If this bit is set to "1", the system will use running window method to search for a matched pattern of valid logic "1". If there is a pattern like logic "0" or collision, system continues to search for next valid SOF and is still in "Receiving" state. If it is cleared to 0, system will quit the "Receiving" state with FramingErr reporting this occurrence. This bit increases noise immunity in most cases.

Bit 2~0 Reserved bits for internal setting, these bits must be fixed at "000" and can not be modified

- **Reserved Register**

This register is reserved for internal settings.

Address	Bit	7	6	5	4	3	2	1	0
0x3D	Name	Reserved							
	Type	R/W							
	Reset Value	1	1	1	1	0	0	0	0

Bit 7~0 Reserved bits for internal settings. For proper operation, the register content must be fixed at "1111_0000" and can not be modified

- **Reserved Register**

This register is reserved for internal settings.

Address	Bit	7	6	5	4	3	2	1	0
0x3E	Name	Reserved							
	Type	R/W							
	Reset Value	1	0	1	1	1	0	0	0

Bit 7~0 Reserved bits for internal setting. For proper operation, the register content must be fixed at "1011_1000" and can not be modified

- **Gain_ST3 Register**

This register is used to setup the gain of the last state amplifier.

Address	Bit	7	6	5	4	3	2	1	0
0x3F	Name	Reserved		Gain_ST3[2:0]			Reserved		
	Type	R/W		R/W			R/W		
	Reset Value	0	0	0	0	0	0	0	0

Bit 7~6 Reserved bits for internal setting, these bits must be fixed at "00" and can not be modified

Bit 5~3 **Gain_ST3[2:0]**: Define the gain of the last state amplifier for systems requiring extensive gain

000: 1x (+0dB)
001: 1.4x (+3dB)
010: 2x (+6dB)
011: 2.8x (+9dB)
100: 4x (+12dB)
101: 5.6x (+15dB)
110: 8x (+18dB)
111: 11x (+21dB)

Bit 2~0 Reserved bits for internal setting. For proper operation, this value should be reconfigured to "010" after system power up

Sector 1 – Page 0: LFO and ADC Adjustment

- **Sector Select Register**

This register is used for sector selection.

Address	Bit	7	6	5	4	3	2	1	0
0x00	Name	—	—	—	—	—	—	—	Sector
	Type	—	—	—	—	—	—	—	R/W
	Reset Value	—	—	—	—	—	—	—	0

Bit 7~1 Unimplemented, read as "0"

Bit 0 **Sector**: Define sector for register page control

• LFOTrimResult Register

This register indicates the low frequency oscillator trimming result.

Address	Bit	7	6	5	4	3	2	1	0
0x01	Name	LFOTrimResult[7:0]							
	Type	R							
	Reset Value	x	x	x	x	x	x	x	x

"x": Unknown

Bit 7~0 **LFOTrimResult[7:0]**: Display the low frequency oscillator trimming result, which is trimmed after system start up or execute "LFOTune" command

• ManLFOTrimValue Register

This register is used to define the LFO trimmed code when automatic trim is disabled.

Address	Bit	7	6	5	4	3	2	1	0
0x02	Name	ManLFOTrimValue[7:0]							
	Type	R/W							
	Reset Value	0	0	0	0	0	0	0	0

Bit 7~0 **ManLFOTrimValue[7:0]**: Define the LFO trimmed code when automatic trim is disabled. The trimmed code can be selected by ManLFOTrim

• LFOTrimSel Register

This register is used to define LFO trimming methodology.

Address	Bit	7	6	5	4	3	2	1	0
0x03	Name	Reserved				—	—	—	ManLFOTrim
	Type	R/W				—	—	—	R/W
	Reset Value	0	0	0	0	—	—	—	0

Bit 7~4 Reserved bits for internal setting, these bits must be fixed at "0000" and can not be modified

Bit 3~1 Unimplemented, read as "0"

Bit 0 **ManLFOTrim**: Define LFO trimming methodology

0: Automatic trimming, LFO trimmed code is defined by LFOTrimResult

1: Manual trimming, LFO trimmed code is defined by ManLFOTrimValue

• FDCDIRqConfig Register

This register is used to define the FDIRq and CDIRq occurrence events.

Address	Bit	7	6	5	4	3	2	1	0
0x04	Name	—	—	—	—	FDIRqCfg[1:0]		CDIRqCfg[1:0]	
	Type	—	—	—	—	R/W		R/W	
	Reset Value	—	—	—	—	0	0	0	0

Bit 7~4 Unimplemented, read as "0"

Bit 3~2 **FDIRqCfg[1:0]**: Define the condition that IRq is set in FieldDetect mode

00: ADC_Result_I or ADC_Result_Q is beyond the threshold level

01: ADC_Result_I is beyond the threshold level

10: ADC_Result_Q is beyond the threshold level

11: ADC_Result_I and ADC_Result_Q is beyond the threshold level

Bit 1~0 **CDIRqCfg[1:0]**: Define the condition that IRq is set in CardDetect mode

00: ADC_Result_I or ADC_Result_Q is beyond the threshold level

01: ADC_Result_I is beyond the threshold level

10: ADC_Result_Q is beyond the threshold level

11: ADC_Result_I and ADC_Result_Q is beyond the threshold level

- **ADC_Adjust Register**

This register defines the maximum input RF amplitude at pin RX for ADC by tuning ADC internal voltage.

Address	Bit	7	6	5	4	3	2	1	0
0x05	Name	—	—	—	—	Reserved		ADC_FullScaleAdj[1:0]	
	Type	—	—	—	—	R/W		R/W	
	Reset Value	—	—	—	—	0	0	0	0

Bit 7~4 Unimplemented, read as "0"

Bit 3~2 Reserved bits for internal setting. For proper operation, these value should be reconfigured to "01" after system power up for best performance

Bit 1~0 **ADC_FullScaleAdj[1:0]**: Define the maximum input RF amplitude at pin RX

00 : ~ 1.35 Vp (5.3mV per step at 8 bits resolution)

01 : ~ 1.02 Vp (4.0mV per step at 8 bits resolution)

10 : ~ 1.64 Vp (6.6mV per step at 8 bits resolution)

11 : ~ 2.01 Vp (7.9mV per step at 8 bits resolution)

This bit field defines the maximum input RF amplitude at pin RX for ADC by adjusting internal ADC voltage reference. The defined amplitude is based on in phase clock projection. If RF signal at RX has phase shift, the amplitude will be higher at the factor of cosine function. Refer to the "RF Amplitude Detector System" section for more details.

Sector 1 – Page 1: Production Parameter

- **Reserved Registers**

These register are reserved for internal settings.

Address	Bit	7	6	5	4	3	2	1	0
0x08~0x09, 0x0B	Name	Reserved							
	Type	R/W							
	Reset Value	0	0	0	0	0	0	0	0

Bit 7~0 Reserved bits for internal settings. For proper operation, the register contents can not be modified.

- **MaskSet Register**

This register shows the device mask set.

Address	Bit	7	6	5	4	3	2	1	0
0x0D	Name	MaskSet[7:0]							
	Type	R							
	Reset Value	x	x	x	x	x	x	x	x

"x": Unknown

Bit 7~0 **MaskSet[7:0]**: Display the device Mask Set for fabrication and production, for current version the value is 0xA8

- **ProductionParam Register**

This register shows the device production parameter.

Address	Bit	7	6	5	4	3	2	1	0
0x0E	Name	ProductionParam[7:0]							
	Type	R							
	Reset Value	x	x	x	x	x	x	x	x

"x": Unknown

Bit 7~0 **ProductionParam[7:0]**: Display the device production parameter, which is changed following production lot

- **Revision Register**

This register shows the device revision.

Address	Bit	7	6	5	4	3	2	1	0
0x0F	Name	Revision[7:0]							
	Type	R							
	Reset Value	x	x	x	x	x	x	x	x

"x": Unknown

Bit 7~0 **Revision[7:0]**: Display the device revision, the current revision is 0x20.

Sector 1 – Page 2: TX Overshoot Control

- **TxFallingCtrl Register**

This register is used to control the TX waveform for falling edge. Refer to the "TX Overshoot Control" section for more details.

Address	Bit	7	6	5	4	3	2	1	0
0x10	Name	TxOvsT1Fall[3:0]				TxOvsT2Fall[3:0]			
	Type	R/W				R/W			
	Reset Value	0	0	0	0	0	0	0	0

Bit 7~4 **TxOvsT1Fall[3:0]**: Define T1 time to control RF waveform overshoot for falling edge

Bit 3~0 **TxOvsT2Fall[3:0]**: Define T2 time to control RF waveform overshoot for falling edge

- **TxRisingCtrl Register**

This register is used to control the TX waveform for rising edge. Refer to the "TX Overshoot Control" section for more details.

Address	Bit	7	6	5	4	3	2	1	0
0x11	Name	TxOvsT1Rise[3:0]				TxOvsT2Rise[3:0]			
	Type	R/W				R/W			
	Reset Value	0	0	0	0	0	0	0	0

Bit 7~4 **TxOvsT1Rise[3:0]**: Define T1 time to control RF waveform overshoot for rising edge

Bit 3~0 **TxOvsT2Rise[3:0]**: Define T2 time to control RF waveform overshoot for rising edge

- **TxCfgFall Register**

This register is used to configure TX1 and TX2 output conductance at falling edge of TX envelope. Refer to the "TX Overshoot Control" section for more details.

Address	Bit	7	6	5	4	3	2	1	0
0x12	Name	—	—	TxCfgFall[5:0]					
	Type	—	—	R/W					
	Reset Value	—	—	0	1	0	0	0	0

Bit 7~6 Unimplemented, read as "0"

Bit 5~0 **TxCfgFall[5:0]**: Define TX1 and TX2 output conductance at falling edge of TX envelope

- **TxCfgRise Register**

This register is used to configure TX1 and TX2 output conductance at rising edge of TX envelope. Refer to the "TX Overshoot Control" section for more details.

Address	Bit	7	6	5	4	3	2	1	0
0x13	Name	—	—	TxCfgRise[5:0]					
	Type	—	—	R/W					
	Reset Value	—	—	0	1	0	0	0	0

Bit 7~6 Unimplemented, read as "0"

Bit 5~0 **TxCfgRise[5:0]**: Define TX1 and TX2 output conductance at rising edge of TX envelope.

Sector 1 – Page 5: RX Amplifier Corner

- **ManualFilter Register**

This register is used for manual adjustment of the filter cut-off frequency if the bit ManFilterSel in the register FilterAdjust is set to "1".

Address	Bit	7	6	5	4	3	2	1	0
0x2E	Name	M_HP1[1:0]		M_LP1[1:0]		M_HP2[1:0]		M_LP2[1:0]	
	Type	R/W		R/W		R/W		R/W	
	Reset Value	0	0	0	1	1	0	0	1

Bit 7~6 **M_HP1[1:0]**: Define high-pass cut-off frequency for the 1st stage high pass filter
00: 636kHz
01: 318kHz
10: 151kHz
11: 75kHz

Bit 5~4 **M_LP1[1:0]**: Define low-pass cut-off frequency for the 1st stage low pass filter
00: 2400kHz
01: 1200kHz
10: 683kHz
11: 363kHz

Bit 3~2 **M_HP2[1:0]**: Define high-pass cut-off frequency for the 2nd stage high pass filter
00: 381kHz
01: 151kHz
10: 75kHz
11: 37kHz

Bit 1~0 **M_LP2[1:0]**: Define low-pass cut-off frequency for the 2nd stage low pass filter
00: 2400kHz
01: 1200kHz
10: 683kHz
11: 363kHz

• FilterAdjust Register

This register is used for filter corner adjustment.

Address	Bit	7	6	5	4	3	2	1	0
0x2F	Name	ManFilterSel	EnAutoTune	—	—	Filter_Corner_Coef[3:0]			
	Type	R/W	R/W	—	—	R/W			
	Reset Value	0	1	—	—	0	1	0	1

Bit 7 **ManFilterSel**
0: Filter corner is defined by the RX mode
1: Filter corner is defined following the ManualFilter register

Bit 6 **EnAutoTune: Select mechanism in tuning filter corner**
0: Filter tuning coefficient is configured through Filter_Corner_Coef
1: Filter tuning coefficient is configured by the tuning result, CFTV, from the RxFilterTune command

Bit 5~4 Unimplemented, read as "0"

Bit 3~0 **Filter_Corner_Coef[3:0]**: Define the filter corner frequency
0000: The corner frequency is set to the highest adjustable value
1111: The corner frequency is set to the lowest adjustable value
0101: Default value

Sector 1 – Page 6: AGC_SSI and RX Freqency Tuning

• Signal Indicator Register

This register is used to indicate signal strength and display corner frequency tuning result.

Address	Bit	7	6	5	4	3	2	1	0
0x37	Name	SSI[3:0]				CFTV[3:0]			
	Type	R				R			
	Reset Value	0	0	0	0	x	x	x	x

"x": Unknown

Bit 7~4 **SSI[3:0]**: Display subcarrier signal strength

SSI[3:0]	Signal Strength	SSI[3:0]	Signal Strength
0000	2 ~ 2.7mV	1000	31 ~ 44mV
0001	2.7 ~ 3.9mV	1001	44 ~ 62mV
0010	3.9 ~ 5.5mV	1010	62 ~ 88mV
0011	5.5 ~ 7.7mV	1011	88 ~ 125mV
0100	7.8 ~ 11mV	1100	125 ~ 175mV
0101	11 ~ 16mV	1101	175 ~ 250mV
0110	16 ~ 22mV	1110	250 ~ 350mV
0111	22~ 31mV	1111	350 ~ 500mV

Bit 3~0 **CFTV[3:0]**: Corner frequency tuning value
This bit field shows the result of tuning value after using command "RxFilterTune". The tuning value affects all filters in receiver chain.

Recommended Register Value for Normal Operation

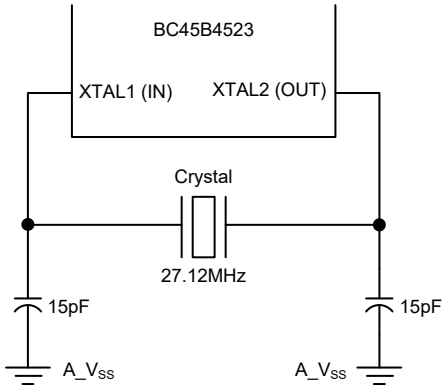
	Addr.		Protocol	Default /Reset	43A				43B				15693 TX		15693 RX Man			15693 RX FSK	
			Data Rate		106	212	424	848	106	212	424	848	1/4	1/256	53k	26k	6.7k	26k	6.7k
Page			Register Name																
Sector0																			
Control and Status	1	0	D	CRCResultLSB	0x63	0x63	0x63	0x63	0x63	0x9C	0x9C	0x9C	0x9C	0x9C	0x9C	0x9C	0x9C	0x9C	0x9C	0x9C
		0	E	CRCResultMSB	0x63	0x63	0x63	0x63	0x63	0x9C	0x9C	0x9C	0x9C	0x9C	0x9C	0x9C	0x9C	0x9C	0x9C	0x9C
TX and Coder	2	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		1	1	TxControl	0x18	0x5B	0x5B	0x5B	0x5B	0x4B	0x4B	0x4B	0x4B	0x5B	0x5B	—	—	—	—	—
		1	2	TxCfgCW	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	0x36	TBD	—	—	—	—	—
		1	3	TxCfgMod	0x10	—	—	—	—	0x10	0x10	0x10	0x10	0x10	0x10	—	—	—	—	—
		1	4	CoderControl	0x19	0x19	0x11	0x09	0x01	0x20	0x18	0x10	0x08	0x2F	0x2E	—	—	—	—	—
		1	5	ModWidth	0x0F	0x0F	0x07	0x02	0x01	0x3F	0x1F	0x11	0x07	0x3F	0x3F	—	—	—	—	—
		1	6	ModWidthSOF	0x0F	0x0F	0x07	0x02	0x01	0x3F	0x1F	0x11	0x07	0x3F	0x3F	—	—	—	—	—
		1	7	TypeBTxFraming	0x3B	—	—	—	—	0x0D	TBD	TBD	TBD	—	—	—	—	—	—	—
RX and Decoder	3																		
		1	8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		1	9	RxControl1	0x6B	0x6B	0x4B	0x2B	0x0B	0x6B	0x4B	0x2B	0x0B	–	–	0x73	0x93	0xD3	0x93	0xD3
		1	A	DecoderControl	0x08	0x28	0x29	0x29	0x29	0x19	0x19	0x19	0x19	–	–	0x30	0x30	0x30	0x32	0x32
		1	B	BitPhase	0x3D	0x3D	TBD	TBD	TBD	0x3D	TBD	TBD	TBD	–	–	TBD	TBD	0x0E	TBD	TBD
		1	C	RxThreshold	0xAA	0x6C	TBD	TBD	TBD	0x6C	TBD	TBD	TBD	–	–	TBD	TBD	0x4C	TBD	TBD
		1	D	BPSKDemControl	0x04	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	–	–	TBD	TBD	0x04	TBD	TBD
		1	E	RxControl2	0x41	0x41	0x41	0x41	0x41	0x41	0x41	0x41	0x41	–	–	0x41	0x41	0x41	0x41	0x41
		1	F	RxControl3	0xA0	0xC3	TBD	TBD	TBD	0XC3	TBD	TBD	TBD	–	–	TBD	TBD	0XE3	TBD	TBD
RF-Timing, Channel Redundancy and ADC	4																		
		2	0	Reserved	0x0A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		2	1	RxWait	0x06	0x04	TBD	TBD	TBD	0x03	TBD	TBD	TBD	—	—	TBD	TBD	0x01	TBD	TBD
		2	2	ChannelRedundancy	0x03	0x03	0x03	0x03	0x03	0x2E	0x2E	0x2E	0x2E	0x2C	0x2C	0x2C	0x2C	0x2C	0x2C	0x2C
		2	3	CRCPresetMSB	0x63	0x63	0x63	0x63	0x63	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
		2	4	CRCPresetLSB	0x63	0x63	0x63	0x63	0x63	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
		2	5	ADCCtrl	0x23	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		2	6	ADC_Result_I	0x00	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		2	7	ADC_Result_Q	0x00	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
FIFO Level, Prog. Timer and Wakeup Timer	5																		
		2	A	TimerClock	0x07	0x0A	0x0A	0x0A	0x0A	0x0A	0x0A	0x0A	0x0A	0x0A	0x0A	0x0A	0x0A	0x0A	0x0A	0x0A
		2	B	TimerControl	0x06	0x06	0x06	0x06	0x06	0x06	0x06	0x06	0x06	0x06	0x06	0x06	0x06	0x06	0x06	0x06
		2	C	TimerReloadValue	0x0A	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
Test, IO Control and RX Adjustment	7	3	8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		3	9	TDIRqCtrl	0x06	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		3	A	Test	0x00	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		3	B	Reserved	0xF0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		3	C	Rx43A_Option	0x88	0x28	TBD	TBD	TBD	—	—	—	—	—	—	—	—	—	—	—
		3	D	Reserved	0xF0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		3	E	Reserved	0xB8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		3	F	Gain_ST3	0x00	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	—	—	TBD	TBD	0x12	TBD	TBD
Sector1																			
LFO and ADC Adjustment	0	0	4	FDCDIRqConfig	0x00	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		0	5	ADC_Adjust	0x00	0x06	0x06	0x06	0x06	0x06	0x06	0x06	0x06	0x06	0x06	0x06	0x06	0x06	0x06	0x06

Recommended Register Value for Each Supported Protocol

Architecture and Peripherals

Crystal Oscillator

The BC45B4523 incorporates a stable low-jitter internal oscillator for generating a master clock for internal and external systems. The device accepts self crystal oscillator and external clock feeding. In certain applications, such as long range readers where noise is a major limiting factor, using an internal oscillator is recommended to obtain minimum jitter.



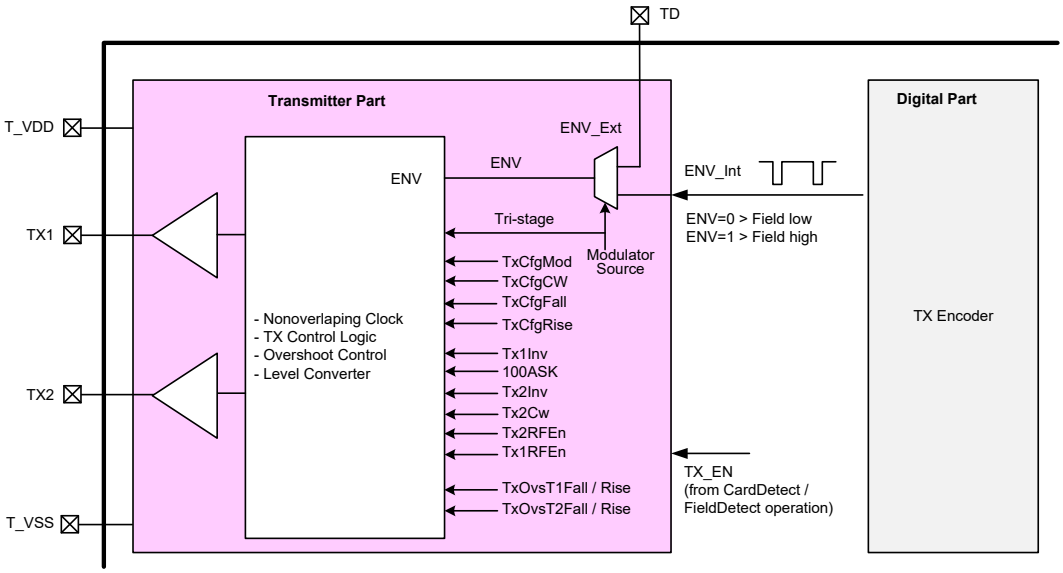
Crystal Oscillator and Clock Divider

In case of external clock sources, the following criteria must be taken into account.

- The duty cycle must be within 40% to 60%.
- The source should be stable and low jitter. The more jitter, the more noise in the RF system.
- The external clock must be fed to the oscillator input, the XTAL1 pin.

Transmitter

A transmitter consists of two drivers and a control logic. The drivers are capable of operating from 2.7V to 5.5V supplied on the T_VDD pin separated from an analog core and a digital core. Wide operating supply voltages enable various applications, from desktop to mid-range panel readers, to be realized by a single NFC reader IC. The drivers are flexibly configured to connect to either closed-coupling matching networks or external drivers, such as Class-E amplifiers in long range applications. The transmitter block diagram is shown as below.



Simplified Transmitter System

The driving behaviour of the transmitter is defined by the register TxControl (Sector0-0x11). By configuring the Tx1Inv, Tx2Inv, Tx2Cw, Tx2RFEn and Tx1RFEn bits, the driver can provide a differential modulated output, a single-ended modulated output or a plain carrier with a baseband signal for driving external circuitry. Setting the 100ASK bit makes the transmitter stops driving carrier during the modulation period. The behaviours of the transmitter in all possible combinations are shown in "TXn Driver Behaviours on TxControl Combinations" table for pin TX1 and pin TX2 respectively.

- **TxControl Register**

This register controls the logical behaviour of the transmitter driver on pin TX1 and TX2.

Address	Bit	7	6	5	4	3	2	1	0
Sector0-0x11	Name	Tx1Inv	ModulatorSource[1:0]		100ASK	Tx2Inv	Tx2Cw	Tx2RFEn	Tx1RFEn
	Type	R/W	R/W		R/W	R/W	R/W	R/W	R/W
	Reset Value	0	0	0	1	1	0	0	0

Configuration			Input (ENV_Int)	Output		Mode
Tx1RFEn	100ASK	Tx1Inv		TX1 Logic	TX1 Conductance	
0	X	0	0	0	Short to T_V_{SS}	Shutdown or Connect to external Circuit
0	X	0	1	1	TxCfgCW	
0	X	1	0	1	TxCfgMOD	Shutdown
0	X	1	1	1	TxCfgCW	
1	0	0	0	RF	TxCfgMOD	Modulation 10-60% ASK
1	0	0	1	RF	TxCfgCW	
1	0	1	0	RF_N	TxCfgMOD	
1	0	1	1	RF_N	TxCfgCW	
1	1	0	0	0	Short to T_V_{SS}	Modulation 100% ASK
1	1	0	1	RF	TxCfgCW	
1	1	1	0	1	TxCfgCW	
1	1	1	1	RF_N	TxCfgCW	

TX1 Driver Behaviours on TxControl Combinations

Configuration				Input (ENV_Int)	Output		Mode
Tx2RFEn	100ASK	TX2Cw	Tx2Inv		TX2 Logic	TX2 Conductance	
0	X	0	0	0	0	Short to T_V_{SS}	Shutdown or Connect to external Circuit
0	X	0	0	1	1	TxCfgCW	
0	X	0	1	0	1	TxCfgMOD	Shutdown
0	X	0	1	1	1	TxCfgCW	
0	X	1	0	0	0	Short to T_V_{SS}	
0	X	1	0	1	0	Short to T_V_{SS}	
0	X	1	1	0	1	TxCfgCW	
0	X	1	1	1	1	TxCfgCW	
1	0	0	0	0	RF	TxCfgMOD	Modulation 10-60% ASK
1	0	0	0	1	RF	TxCfgCW	
1	0	0	1	0	RF_N	TxCfgMOD	
1	0	0	1	1	RF_N	TxCfgCW	

Configuration				Input (ENV_Int)	Output		Mode
Tx2RFEn	100ASK	TX2Cw	Tx2Inv		TX2 Logic	TX2 Conductance	
1	1	0	0	0	0	Short to T_V_{SS}	Modulation 100% ASK
1	1	0	0	1	RF	TxCfgCW	
1	1	0	1	0	1	TxCfgCW	
1	1	0	1	1	RF_N	TxCfgCW	
1	X	1	0	X	RF	TxCfgCW	CW on TX2, carrier derived (connect to external circuit)
1	X	1	1	X	RF_N	TxCfgCW	

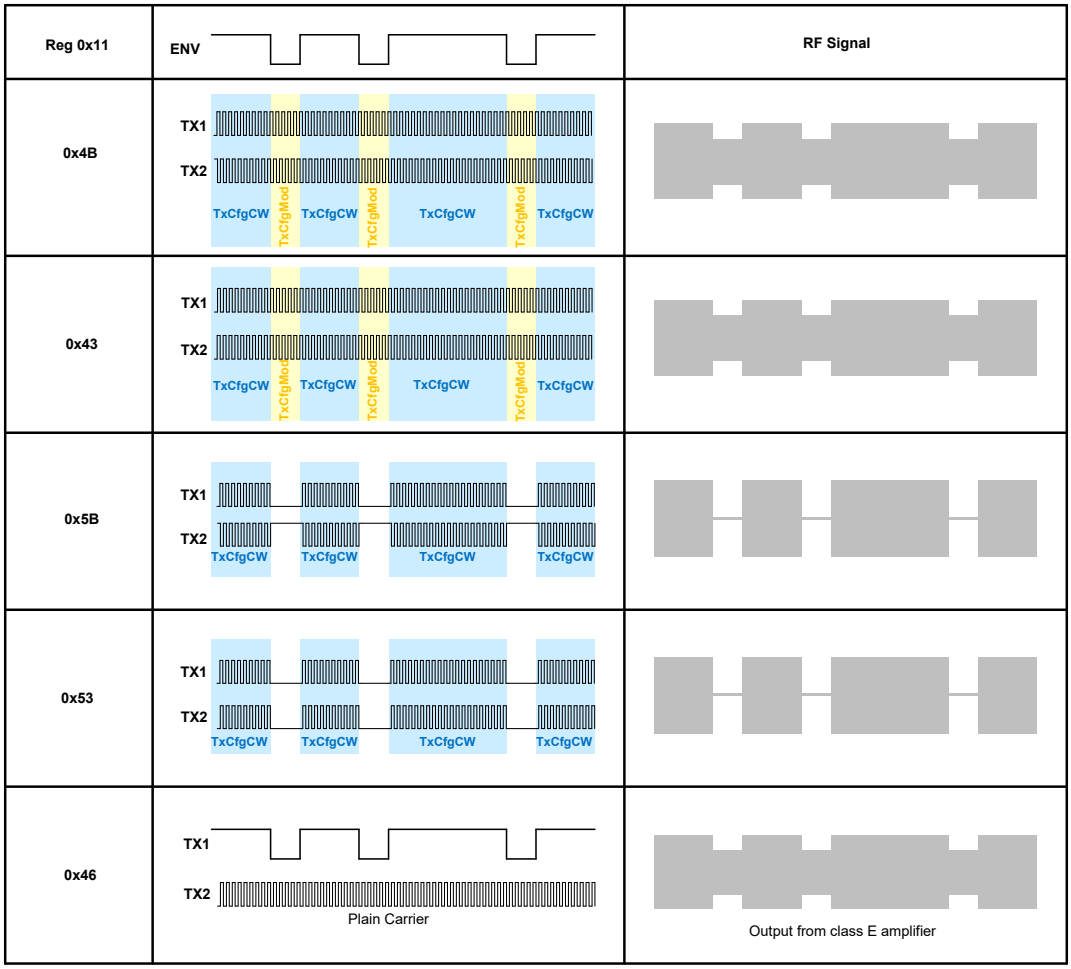
TX2 Driver Behaviours on TxControl Combinations

In case of an ASK modulation where the 100ASK is reset, the conductance of the drivers is controlled by two 6-bit bit fields, namely the TxCfgCW (Sector0-0x12.[5:0]) and TxCfgMod (Sector0-0x13.[5:0]), to create two different RF levels, called un-modulation and modulation respectively. TxCfgCW corresponds to the level high of the baseband signal ENV from the transmitter coder, whereas TxCfgMod corresponds to the level low. Based on the transmitted signal from the coder, value of TxCfgCW must be higher than that of TxCfgMod to make the pattern of the RF-field modulation conforms to the standard. Depending on the antenna characteristic, the modulation index can be adjusted from 0% to 60% with 63 steps resolution if TxCfgCW is set to the maximum value of 0x3F.

The transmitter is allowed to transmit data from an internal coder, an external control signal via pin TD, or a tri-state set through the ModulatorSource bit. The output driver incorporates a non-overlapping clock to reduce the power due to switching leakage current from T_V_{DD} to T_V_{SS}. Note that the logic of the signal ENV_Int from the coder in the rest state is high(1). Examples of TxControl configurations for various working modes are shown in table and figure as follows.

Value	Mode	TX1 Output	TX2 Output	Purpose	Supported Standard
0x00	Shut down TX	Hi-Z	Hi-Z	—	—
0x58	Shut down TX	1	1	Shut down	—
0x4B	Differential Output, ASK	Modulated 13.56MHz carrier	Inverted modulated 13.56MHz carrier	—	ISO14443B, ISO15693
0x43	Double Power, Single ended Output, ASK	Modulated 13.56MHz carrier	Modulated 13.56MHz carrier	TX1 and TX2 can be shorted together for double power	ISO14443B, ISO15693,
0x5B	Differential Output, 100%ASK	Modulated 13.56MHz carrier	Inverted modulated 13.56MHz carrier	—	ISO14443A, ISO15693
0x53	Double Power, Single ended Output, 100%ASK	Modulated 13.56MHz carrier	Modulated 13.56MHz carrier	TX1 and TX2 can be shorted together for double power	ISO14443A, ISO15693
0x46	Driving External circuitry	Internal Baseband sub-carrier signal	13.56 MHz carrier	Connect to the external driver, e.g., Class-E Amplifier	ISO14443B, ISO15693,

Suggested Values and Applications for Transmitter Configuration Control



RF Signal Pattern and Output Logic Level during Modulation

The bit modulation pattern and the frame format for the operating standards can be configured using the register CoderControl (Sector0-0x14). The following table shows CoderControl settings for ISO14443A, ISO14443B and ISO15693. In addition, the RF modulation width in both transmitted bits and the SOF in ISO14443A and ISO15693 can be adjusted by the ModWidth(Sector0-0x15) and ModWidthSOF (Sector0-0x16) registers respectively at the resolution of 2 clocks. For ISO14443B, the transmitted frame format, related to SOF, EOF and EGT, can be configured via the register TypeBTxFraming (Sector0-0x17).

Standard	TX Rate	CoderRate[2:0]	TxCoding[2:0]
ISO14443A	106kbps	011	001
	212kbps	010	001
	424kbps	001	001
	848kbps	000	001
ISO14443B	106kbps	100	000
	212kbps	011	000
	424kbps	010	000
	848kbps	001	000
ISO15693	1 of 4	101	110
	1 of 256	101	111

CoderRate and TxCoding Settings for Supported Standards

Besides, the output driver includes the non-overlapping clock to reduce the power due to leakage current from T_V_{DD} to ground during switching. TX_EN is an internal global control signal sent from the main control block operated in CardDetect and FieldDetect mode. When TX_EN is cleared, in FieldDetect operation, both the driver pins, the TX1 and TX2, are configured to Hi-Z state.

TX Overshoot Control

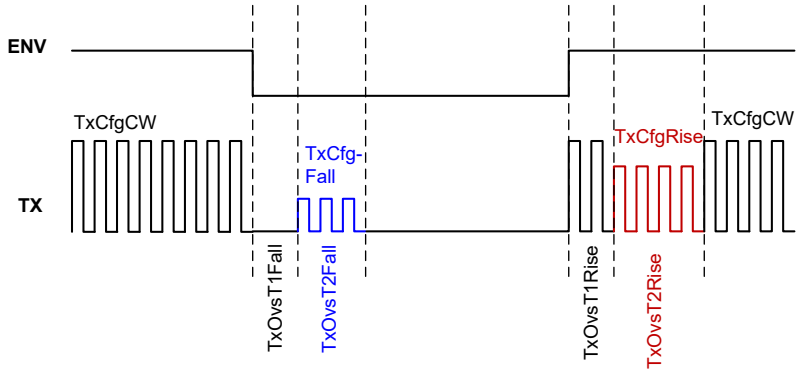
The device provides RF overshoot protection control to avoid both overshoot and undershoot during communication. When the TX Envelope, ENV, is toggled low, internal overshoot timer starts operation. The timing control can be separated into several phases.

In the first phase, controlled by the TxOvsT1Fall bit field, TX output conductance is cleared when 100ASK="1", or set to the value of the TxCfgMod bit field when 100ASK="0". Secondly, TX output conductance is defined by the TxCfgFall bit field for a time configured by the TxOvsT2Fall bit field. Then conductance is cleared or set to the same value of the first phase and wait until ENV is toggled high. When ENV is set high, TX conductance is set to the value of the TxCfgCW bit field for a time configured by the TxOvsT1Rise bit field and then changed to TxCfgRise for a time configured by the TxOvsT2Rise bit field. Finally, TX conductance will return to un-modulation level, TxCfgCW. The TX conductance and timing of each phase is defined as listed in the following table.

Phase	Timing Control	Address.Bit	TX Conductance	Address.Bit	Note
1	TxOvsT1Fall	Sector1-0x10.[7:4]	0	—	100ASK="1"
			TxCfgMod	Sector0-0x13.[5:0]	100ASK="0"
2	TxOvsT2Fall	Sector1-0x10.[3:0]	TxCfgFall	Sector1-0x12.[5:0]	—
3	Depend on ENV width	—	0	—	100ASK="1"
		—	TxCfgMod	Sector0-0x13.[5:0]	100ASK="0"
4	TxOvsT1Rise	Sector1-0x11.[7:4]	TxCfgCW	Sector0-0x12.[5:0]	—
5	TxOvsT2Rise	Sector1-0x11.[3:0]	0	—	100ASK="1"
			TxCfgRise	Sector0-0x13.[5:0]	100ASK="0"

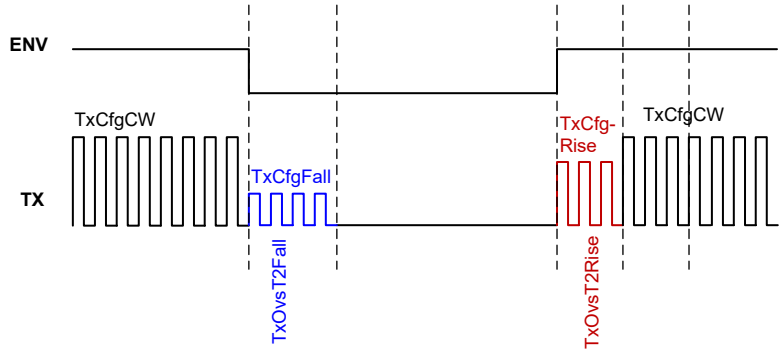
TX Overshoot Control Settings

The TX overshoot control examples are shown in the fol lowing figures.



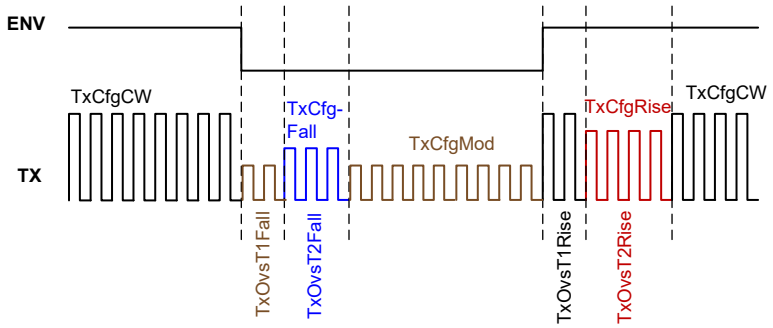
TX Example Waveform for Overshoot Control

(100ASK=1, TxOvsT1Fall=2, TxOvsT2Fall=3, TxOvsT1Rise=2, TxOvsT2Rise=4)



TX Example Waveform for Overshoot Control

(100ASK=1, TxOvsT1Fall=0, TxOvsT2Fall=4, TxOvsT1Rise=0, TxOvsT2Rise=3)

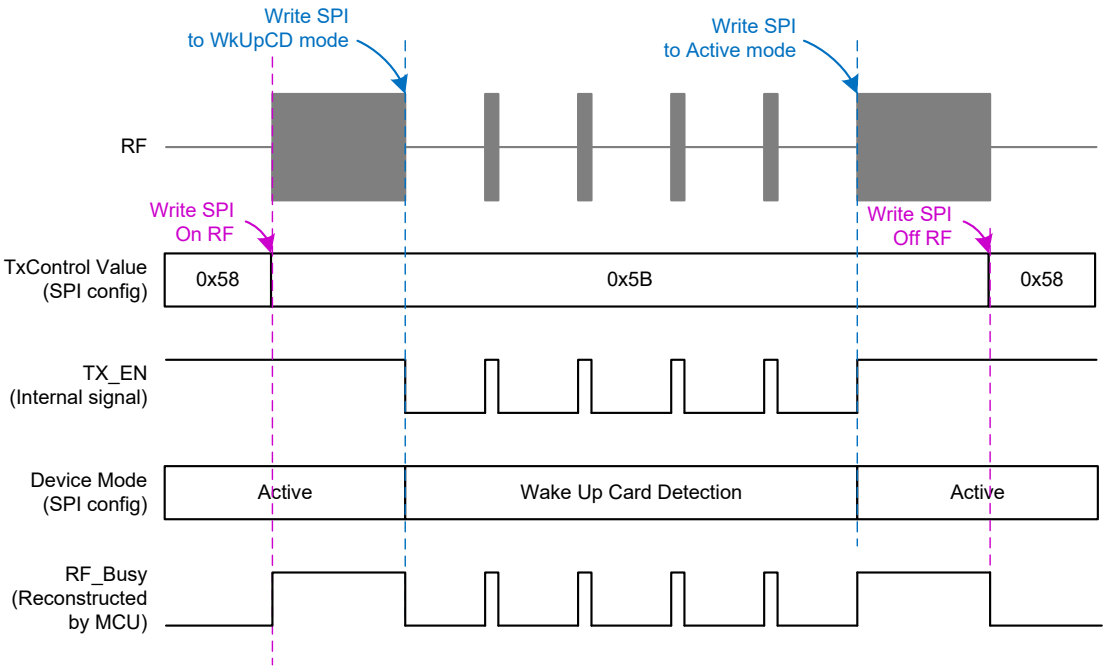


TX Example Waveform for Overshoot Control

(100ASK=0, TxOvsT1Fall=2, TxOvsT2Fall=3, TxOvsT1Rise=2, TxOvsT2Rise=4)

RF Busy Indicator

To monitor RF field transmission phase of the device, RF_Busy, the external control device or microcontroller need to reconstruct the device registers and signal behaviours as shown in the figure below.



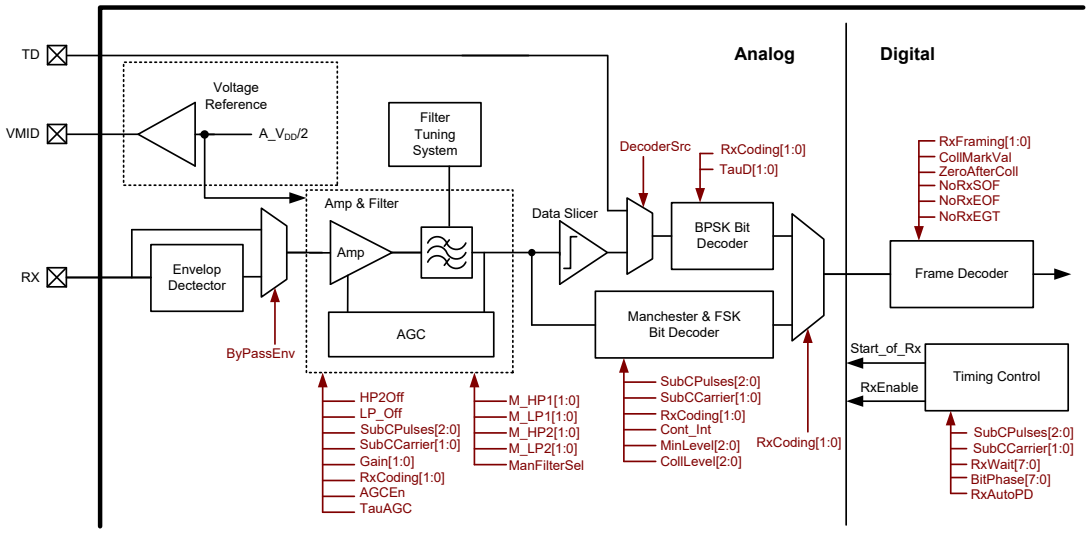
RF_Busy Signal MCU's Recognization

In active mode (idle, transmit or receive), TxControl value (Sector0-0x11) directly controls transmitter. RF is turned on when register is configured to a proper value as shown in the above "Suggested Values and Applications for Transmitter Configuration Control" table, such as 0x5B or 0x4B. While in WkUpCD mode, the RF is turned on and off automatically following the TX_EN internal signal which periodically toggle, refer to the "Wake Up Card Detection Mode" for more details. When the TX_EN is "1", transmistter is performed by the TxControl register. When the TX_EN cleared to "0", transmitter is forced to turned off. The TX_EN can be monitored by probing out via TD pin as described in the "Test Signal" section.

Therefore, the RF_Busy should be reconstructed by MCU with a combination of TxControl value in Active mode and the TX_EN in WkUpCD mode.

Receiver

The receiver part consists of an envelope detector, a voltage reference generator, an amplifier & filter system, a filter tuning system, a BPSK bit decoder, a Manchester-and-FSK bit decoder, a frame decoder and a timing control generator. The conceptual block diagram is shown as below.

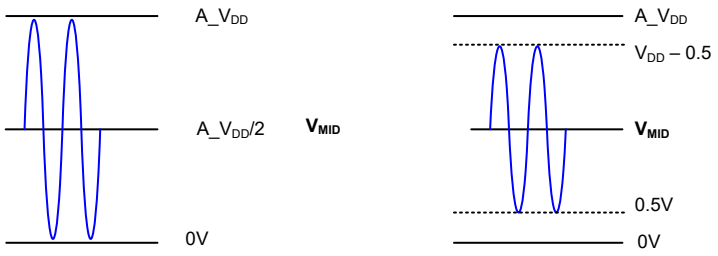


Simplified Receiver System

Envelope Detector and Voltage Reference

The device has integrated an internal envelope detector to extract the card-modulation signal from the RF carrier presented at RX pin. The internal envelope detector is suitable for proximity readers. In addition, the architecture allows the device to use an external envelope detector to boost read range. In this case, the ByPassEnv bit (Sector0-0x1E.2) must be set to route the input signal directly to the amplifier & filter section.

The following figure displays the input signal swing on the RX pin. If external envelope detector is selected, the input signal to the RX pin must be kept within 0.5V and V_{DD} - 0.5V to prevent distortion. In case of the internal envelope detector, the amplitude of the signal carrier on the pin RX must be kept in rail-to-rail.

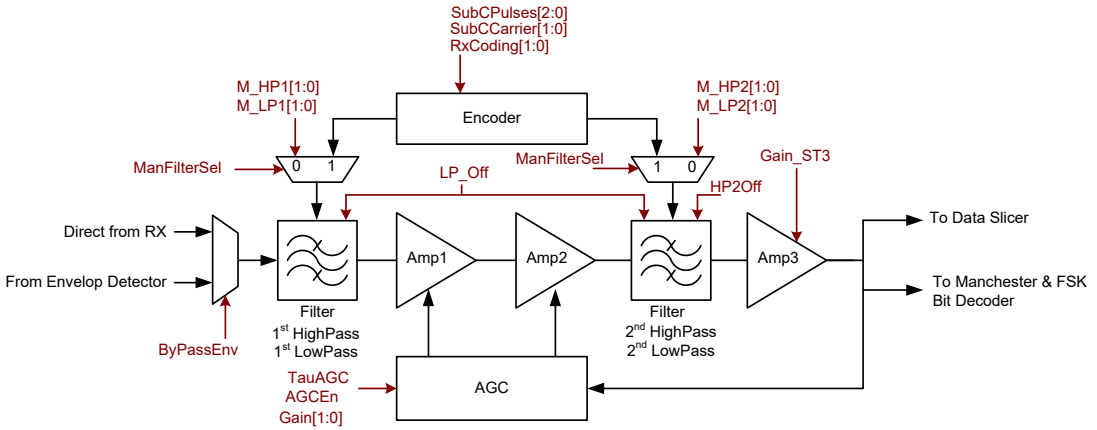


Signal swing on the RX pin

The voltage reference generator provides a reference voltage, about $A\_V_{DD}/2$, for a receiver divider path through the VMID pin and an internal voltage reference. For system stability, an external 100nF capacitor must be connected on the VMID pin.

Amplifier & Filter System

The filter and the amplifier can remove unwanted RF carriers, enlarge the received signal from the envelope detector and reconstruct the baseband signal. The amplifier incorporates automatic gain control (AGC) to adjust the amplitude of the amplified baseband signal to a proper working range. The figure below shows detailed structure of the amplifier & filter system.



Amplifier & Filter System Detailed Structure

Using the AGC can discriminate the larger signal from the smaller signal in case of anti-collision for Manchester coding. As a result, the cards nearer to the reader will be seen first. Also, the AGC prevents the pulse shape from distortion. In addition, in noisy environment, the AGC adjusts the gain to the maximum operable value that the noise does not overwhelm the internal working range. Although the operable read range is confined, the readable range still exists if the AGC is used. For fixed gain selection, if the gain is set too high, the signal and noise may be amplified to the extent that the following state is unable to discriminate. Using the AGC is optional for users by setting the AGCEn register bit (Sector0-0x1D.1). If the AGCEn is not set, the user can fix the gain of the first two stage amplifier by setting the Gain[1:0] (Sector0-0x19.[1:0]). The gain of last amplifier, which is not in the AGC loop, can be arbitrarily set to increase total gain from 0dB to 21dB by configuring the Gain_ST3[2:0] bits (Sector0-0x3F.[5:3]). Using this additional gain is recommended for ISO15693 where extended read range is required. In other standards, the suggested value of Gain_ST3[2:0] is "000". When using this gain state, users should check that noise from the designed system is not large and does not overwhelm the latter decoder until it is unable to interpret data. The TauAGC bit (Sector0-0x1D.0) is optional for setting the speed of the AGC. If TauAGC is cleared to 0, the time constant of the loop bandwidth equals one period of the operating subcarrier. If TauAGC is 1, the time constant equals two periods. In normal condition, clearing the TauAGC to 0 is recommended. If the AGC is not used, the amplifier gain is defined as the following table shows.

Gain[1:0]	Gain
00	12dB (4x)
01	24dB (16x)
10	36dB (64x)
11	48dB (250x)

Amplifier Gain of the First Two Stage in the Receiver

In normal operation where the manual-filter-adjustment register bit ManFilterSel (Sector1-0x2F.7) is not set, the filter's frequency corner is automatically defined by the SubCCarrier[1:0] bits (Sector0-0x19.[4:3]) and RxCoding[1:0] bits (Sector0-0x1A.[1:0]). The frequency corner is designed by following requirements of the operating standard to cover the power spectrum of the incoming line coding in most situations. Besides, the frequency corner can be arbitrarily adjusted by setting the ManFilterSel bit and specifying the desired frequency corner values in the ManualFilter register (Sector1-0x2E). This can be used to cope with distorted bandwidth of the antenna in some circumstances, for example, detuning of the reader antenna by placing the card very close. In addition, the HP2Off bit (Sector0-0x1D.4) and LP_Off bit (Sector0-0x19.2) are optionally used to deal with the channel bandwidth distortion. Setting the HP2Off bit turns off the 2nd stage high-pass filter in the amplifier chain, resulting in a reduction of spurious collision due to the residue pulse effect after a large burst of Manchester coding, especially in ISO14443A. Setting the LP_Off bit extends the channel bandwidth by trading of increasing of input noise. However, in normal situations, it's recommended to reset both HP2Off and LP_Off bits.

Filter Tuning System

If the automatic tuning enable bit EnAutoTune (Sector1-0x2F.6) is set to 1, the RxFilterTune command will be activated and the filter tuning system will restore the corner frequencies of the filter to the proper values in order to eliminate results from temperature and process variations due to IC manufacturing. Tuning time after activating the

command is 302μs. However, the effect from temperature variation is not significant even if the whole IC is heated up by the driver. This process is performed every time the system is powered up. Therefore, it is not required to tune the filter frequently by users.

If the EnAutoTune is cleared to 0, the corner frequencies of each filter shown in the "Amplifier & Filter System Detailed Structure" figure can be manually set by the filter-corner coefficient bit filed Filter_Corner_Coef (Sector1-0x2F.[3:0]). If the Filter_Corner_Coef bit field is set to "0000", the corner frequency will be set to the highest adjustable value. In contrast, the lowest adjustable corner frequency is obtained when the Filter_Corner_Coef bit field is set to "1111".

BPSK Bit Decoder

The BPSK decoder converts the incoming BPSK streams into digital data bits which are able to be processed by the frame decoder. The TauD[1:0] (Sector0-0x1D.[3:2]) defines a time constant of the digital phase lock loop (DPLL) used to recover the subcarrier clock from the BPSK line coding. The higher value of TauD[1:0], the longer the locking time but the more stability. However, depending on the preamble length of each standard, users should properly configure the TauD[1:0]. The following table shows the number of pulses that the DPLL can lock in worst case scenarios. The BPSK stream can be either from the internal data slicer or the external digitized BPSK signal via the TD pin by setting the DecoderSrc bit (Sector0-0x1E.0).

TauD[1:0]	The Number of Pulses can Lock
00	10
01	22
10	44
11	88

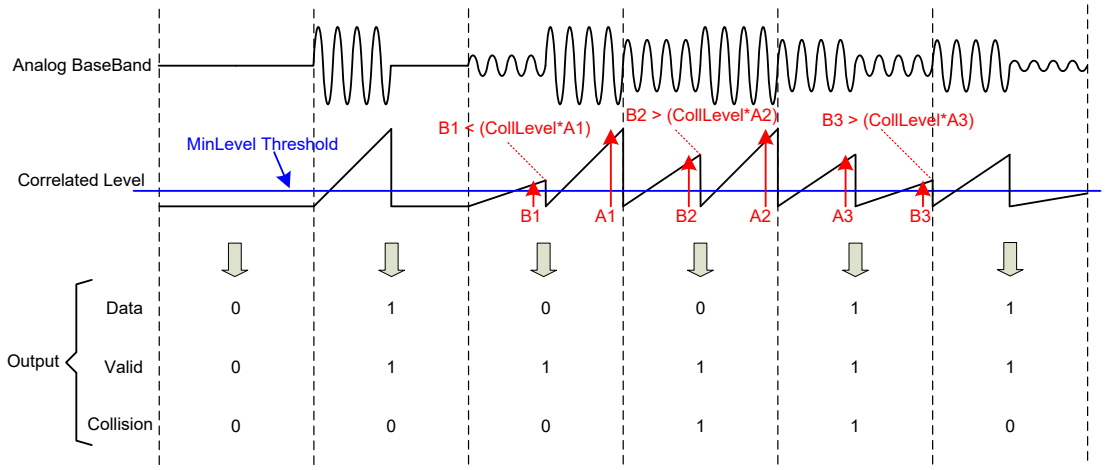
The Number of Pulses that the DPLL can Lock in the Worst Case

To enhance noise tolerance, setting the BPSKDataRec bit (Sector0-0x1F.6) will enable BPSK data recovery scheme that predict data pattern from repetitiveness of BPSK data stream pattern for ISO14443A/B. The decoding method, controlled by BPSKDecMeth bit (Sector0-0x1F.7), can be selected to be either adaptive framing or digital correlator. Both methods can handle BPSK in noisy situation. The adaptive framing is suitable for distorted bit length (ETU) or high jitter baseband swinging around normal bit grid. This method can handle consecutive shrunk or extended bit length. The maximum boundary of deviation is ±1/8 ETU. The digital correlator is suitable for high jitter baseband signal where bit boundary must swing around normal bit grid. This method monitors repetitiveness of data stream to evaluate the incoming bit whether it is 1 or 0. The MinLevel bit field (Sector0-0x1C.[7:5]) can set threshold defining validity of incoming bit. For general case, digital correlator is recommended.

Manchester-and-FSK Bit Decoder

The Manchester-and-FSK bit decoder is capable of decoding both 1-subcarrier Manchester in ISO14443A and ISO15693, and 2-subcarrier Manchester coding (FSK) in ISO15693. The decoder is an analog circuit based on a correlator to search if any incoming signal matches the predefined pattern. The correlator can increase the signal-to-noise ratio, especially, for low data rate in ISO15693 in which the redundancies from long bit patterns are plentiful. The following figure shows the Manchester-and-FSK bit decoder output from the analog baseband. Each bit interval is divided into half to evaluate output values, collision and validity, and then delivered to the frame decoder. The triangle shape of the signals in the following figure are the integrating results of each half bit for evaluation. Each decoded data bit is proven valid if the signal in each half bit is stronger than the MinLevel threshold, set by the MinLevel[2:0] (Sector0-0x1C.[7:5]), as shown in the following figure. The lower value of the Minlevel results in the higher receiving sensitivity by trading off the receiving errors due to noise. Each decoded data bit is treated to be collided if the signal in the weaker half-bit is relatively larger than the stronger half-bit. The CollLevel[2:0] (Sector-0x1C.[3:1]) defines such relative level from the stronger half bit.

The CollLevel value should be set to a proper level for a specific operating mode. If CollLevel is set too high, the high threshold can cause the codec fail to detect collision due to variations in evaluation resulting from noise or bitphase misaligment. Also, if CollLevel is set too low, the lower threshold can cause false collisions due to noise or bitphase misalignment. In general transactions where anti-collision is not required, the CollLevel value should be set to the highest value to prevent errors from collision report due to noise in the system. Effect from MinLevel and CollLevel setting is also illustrated in the following figure. From experiment, the recommended values of MinLevel and CollLevel setting are shown in the following table.



Manchester-and-FSK Bit Decoder Output (ISO14443A)

Standard / Coding	MinLevel[2:0]	CollLevel[2:0]
ISO14443A / Manchester (No Anti-Collision)	111	111
ISO14443A / Manchester (Anti-Collision)	100	110
ISO15693 / Manchester	101	101
ISO15693 / FSK	101	101

Typical Value for MinLevel and CollLevel

The SubCCarrier[1:0], SubCPulses[2:0] and RxCoding[1:0] bit fields must be predefined to form expected bit patterns and evaluating intervals. As shown in the figure in the "Timing Control Generator" section, the correlator starts operation by relying on the activation of the internal signal Start_of_Rx. Timing of Start_of_Rx can be controlled by the RxWait register (Sector0-0x21) and BitPhase register (Sector0-0x1B) where their details will be described in the "Timing Control Generator" section. For low data rate of 6.67kbps and 13.3kbps in ISO15693, setting the special control bit Cont_Int (Sector0-0x1E.7) can further increase the gain of the correlator by 4 times and 2 times respectively. This also increases the signal-to-noise ratio by 6dB and 3dB accordingly.

Frame Decoder

Depending on operating standards defined by registers RxFraming (Sector0-0x1A.[4:3]) and SubCCarrier, the frame decoder extracts byte data, checks CRC, parity and frame formats. Moreover, it removes headers and trailers. Then, the decoded data is transferred to the FIFO.

For Manchester decoding in ISO14443A and ISO15693, if there is a collision of data, the frame decoder will detect and report the first collision of the bit stream in the register CollPos (Sector0-0x0B). Two optional control register bits are provided, namely CollMarkVal (Sector0-0x1A.6) and ZeroAfterColl (Sector0-0x1A.5), to ease the software in manipulating the collision bit in ISO14443A and ISO15693. The collided bits are set to the value following the CollMarkVal bit. If ZeroAfterColl is set, the receiving bit after collision will be cleared to zero.

For BPSK decoding in the ISO14443A, end frame is defined by even parity. For BPSK decoding applied for ISO14443B, the NoRxSOF, NoRxEOF and NoRxEGT bits(Sector0-0x1D.[7:5]) can be optionally selected to suppress errors due to unusual frame formats that may arise from some cards.

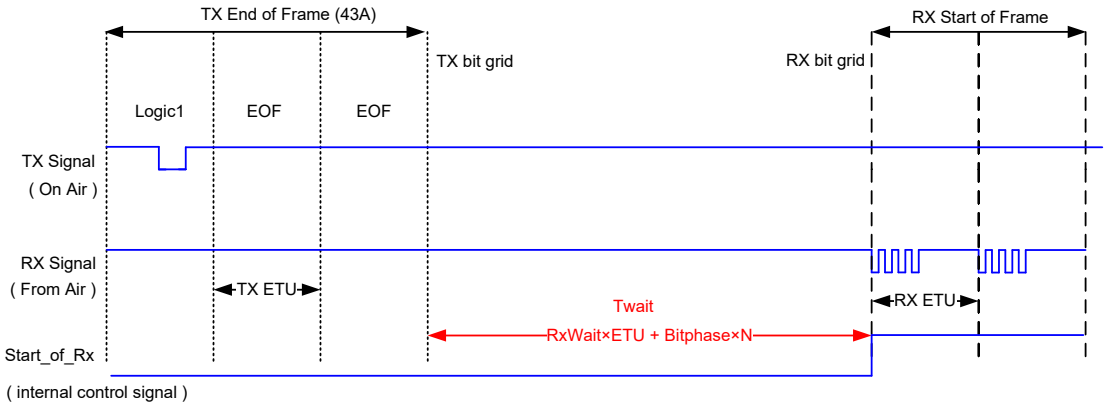
If errors occur during reception, error flags related to decoders, namely CRCErr, FramingErr, ParityErr and CollErr, (Sector0-0x0A.[3:0]) will be reported.

Timing Control Generator

The timing control generator provides control signal Start_of_Rx to start decoding for all types of decoders in the receiver part. Time between the end of the last transmission bit and the Start_of_Rx active, named Twait, is defined by registers RxWait (Sector0-0x21) and BitPhase (Sector0-0x1B) according to the following relation

$$Twait\ (Clk)=RxWait\times ETU + BitPhase\times N$$

ETU is an elementary time unit of the bit defined by t r[1:0] and the number of pulses in SubCpulses[2:0] as shown in the "ETU Interval" table below. The numbers in yellow boxes are practical numbers for existing modes in supported standards. The following table named "Setting of SubCCarrier[1:0] and SubCpulses[2:0] for Supported Standards" shows SubCCarrier[1:0] and SubCpulses[2:0] required for each supported standard. BitPhase defines an additional time delay in a fraction of ETU. N, depending on SubCpulses[2:0], is a scaling factor in multiple of clocks as shown in the "Scaling Factor (N) in Multiple of Clocks" table. The Twait is conceptually illustrated in the following figure. The Twait must be properly set to indicate the Manchester-and-FSK bit decoder to start synchronizing with the beginning point of the uplink signal, especially, in ISO14443A at the rate of 106kbps and ISO15693. In case of BPSK decoding, Start_of_Rx must be set to active prior to the coming of the uplink signal. Proper values for RxWait and BitPhase in each standard are shown in the "Recommended Values for RxWait and BitPhase in Each Standard" table. In addition, if the control signal RxAutoPD (Sector0-0x1E.6) is set, the receiver part is only turned on after the end of the transmission and turned off after the completion of the reception to reduce power consumption of the analog part.



Twait Timing between TxEOF and RxSOF in ISO14443A at 106kbps

SubCCarrier [1:0]	SubCpulses[2:0]						
	000 (1 Pulse)	001 (2 Pulses)	010 (4 Pulses)	011 (8 Pulses)	100 (16 Pulses)	101 (32 Pulses)	110 (64 Pulses)
01 (16 clks)					256	512	1024
10 (32 clks)		64	128				
11 (64 clks)		128	256	512	1024	2048	4096

ETU Interval (in Number of Clocks)

SubCCarrier [1:0]	SubCpulses[2:0]						
	000 (1 Pulse)	001 (2 Pulses)	010 (4 Pulses)	011 (8 Pulses)	100 (16 Pulses)	101 (32 Pulses)	110 (64 Pulses)
01 (16 clks)					—	—	—
10 (32 clks)	—	—	—				
11 (64 clks)	—	—	—	—	—	—	—

Setting of SubCCarrier[1:0] and SubCpulses[2:0] for Supported Standards

SubCpulses[2:0]		N
Code	Number of Pulse	
000	1 Pulse	1
001	2 Pulses	1
010	4 Pulses	1
011	8 Pulses	1
100	16 Pulses	2

SubCpulses[2:0]		N
Code	Number of Pulse	
101	32 Pulses	4
110	64 Pulses	8

Scaling Factor (N) in Multiple of Clocks

Standard	Downlink	Uplink	RxWait	BitPhase
ISO14443A	Miller – 106kbps	Manch – 106kbps	0x07	0x3D
	Miller – 212kbps	Manch – 106kbps	0x03*	0x88*
	Miller – 424kbps	Manch – 106kbps	0x03*	0x32*
	Miller – 848kbps	Manch – 106kbps	0x03*	0x40*
	Miller - 212, 424, 848	BPSK - 212, 424, 848	0x03*	Don't care
ISO14443B	NRZ - 106, 212, 424, 848	BPSK - 106, 212, 424, 848	0x03	Don't care
ISO15693	1 of 4 - 26k, 1 of 256 - 26k	Manch - 26kbps	0x08	0x40
		Manch - 6.67kbps	0x02	0x0E
		FSK - 26kbps	0x08	0x40
		FSK - 6.67kbps	0x02	0x0E

*: The provided values are mean values that can be used for most cards. However, there are difference in response timing among various card manufacturers. To achieve highest performance in a certain system or for a specific card, RxWait and BitPhase shall be tuned to properly align with the card response.

Recommended Values for RxWait and BitPhase in Each Standard

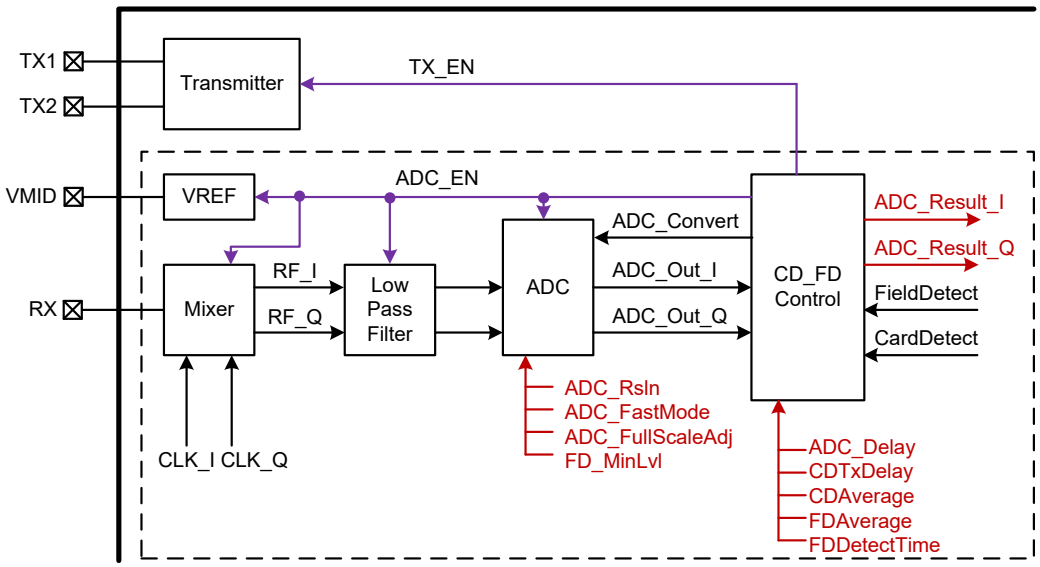
Key Register Settings for Reception

The following table shows the RxFraming[1:0], RxCoding[1:0], SubCCarrier[1:0] and SubCpulses[2:0] settings for ISO14443A, ISO14443B and ISO15693.

Standard	RX Rate	RxFraming[1:0]	RxCoding[1:0]	SubCCarrier[1:0]	SubCpulses[2:0]
ISO14443A	Manch 106kbps	01	00	01	011
	BPSK 212kbps		01		010
	BPSK 424kbps				001
	BPSK 848kbps				000
ISO14443B	BPSK 106kbps	11	01	01	011
	BPSK 212kbps				010
	BPSK 424kbps				001
	BPSK 848kbps				000
ISO15693	Manch 53kbps	10	00	10	011
	Manch 26kbps				100
	Manch 13kbps				101
	Manch 6.7kbps				110
	FSK 26kbps		10		100
	FSK 13kbps				101
	FSK 6.7kbps				110

RxFraming, RxCoding, SubCCarrier and SubCpulses Settings for Supported Standards

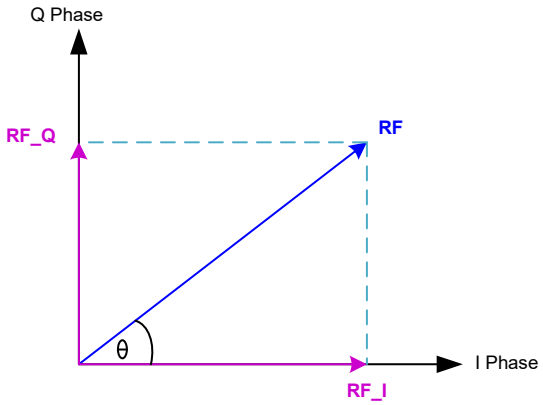
RF Amplitude Detector System



Simplified RF Amplitude Detector System

The device is capable to measure 13.56MHz sinewave amplitude at RX pin with a system shown in the above figure. The system will be applied in CardDetect mode, which measure the changing RF amplitude driving by device itself, and FieldDetect mode, which sense the RF field from external component.

Mixer circuit multiplies external RF at pin RX with internal clock reference in phase and quadrature phase, CLK_I and CLK_Q. Mixer output signals, RF_I and RF_Q, will be projected into each phase following phase difference between RF at input and clock reference as shown in the following figure. Then both signals will be filtered to DC voltage represented RF amplitude before being converted to digital domain by ADC.



Mixer Output Signal Concept

ADC output resolution can be selected by ADC_RsIn bit (Sector0-0x25.1), where "1" for 8 bits and "0" for 7 bits. The higher resolution also increases the ADC conversion time. ADC_FastMode bit (Sector0-0x25.2) defines ADC conversion mechanism. When this bit is set to "1", the conversion time is reduced by maintain its resolution.

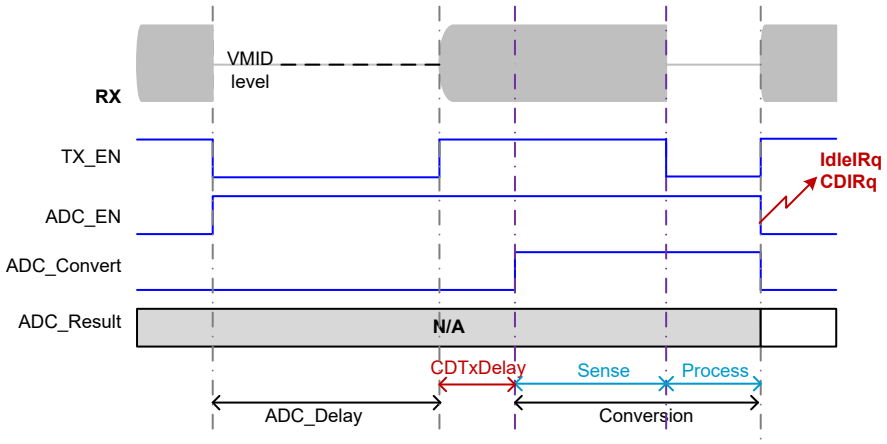
The ADC voltage reference, which refers to full range input RF amplitude voltage, can be adjusted by ADC_FullScaleAdj bits (Sector1-0x05.[1:0]). The RF amplitude step size is as shown in following table. By the way, the shown RF step size is the projected amplitude to I and Q phase. Therefore, the actual step size could be increased in the factor of sine or cosine function. Only in field detection operation, Setting FD_MinLvl bit (Sector0-0x25.3) to "1" enhance sensitivity, but trading off with reducing full scale range by a half.

ADC_FullScaleAdj [1:0]	Effective RF Input Amplitude (mVp) Step Size	
	ADC_RsIn=0 (7 bits)	ADC_RsIn=1 (8 bits)
00	10.6mVp	5.3mVp
01	8.0mVp	4.0mVp
10	13.1mVp	6.6mVp
11	15.9mVp	7.9mVp

Effective RF Input Amplitude Step Size for ADC_FullScaleAdj and ADC_RsIn at RX Pin

The following figure shows the basic operation in CardDetect mode. After CardDetect command is executed, the device will automatically disable transmitter by clearing TX_EN to 0. Then ADC and VREF circuit will be enabled by ADC_EN signal. The ADC_Delay bit field (Sector0-0x25.[5:4]) are used to configure delay time for analog signal settle before transmitter is re-enabled. After transmitter is turned on, ADC will wait for a short time setting by CDTxDelay bit (Sector0-0x31.2) for RF signal settle before start conversion by setting ADC_Convert to 1. The conversion period splits into 2 phases. First is the "sense" phase, in which transmitter drives RF field and ADC monitors RF amplitude changing when card or tag is loaded into field. The other is "process", in which transmitter is turned off and ADC data is calculated. After the conversion is completed, IdleIRq is set. And if the value of register ADC_Result_I (Sector0-0x26) or ADC_Result_Q (Sector0-0x27) are beyond threshold level, CDIRq will be set. The following table shows the conversion time for each configuration.

CardDetect Mode



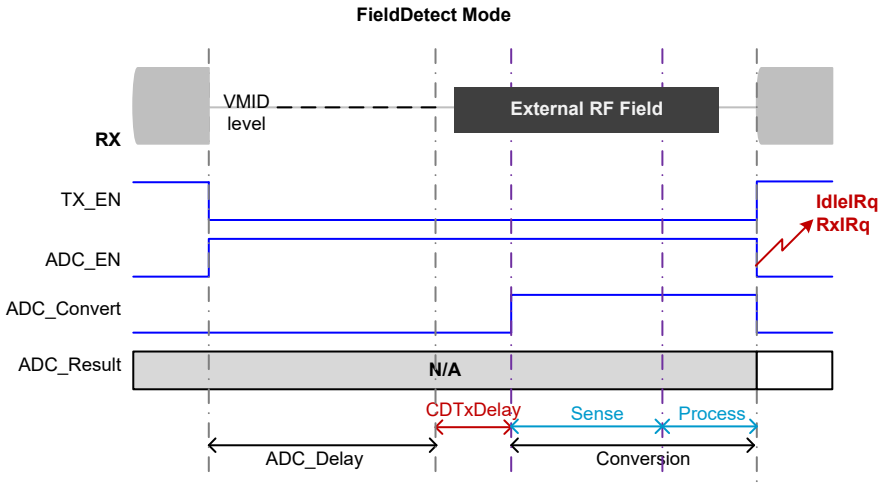
Basic Timing for CardDetect Mode

ADC_FastMode	ADC_RsIn	Sense Period (T_sense)	Max Conversion Time ("T_sense" + "T_process")
0	0 - 7bits	4.72μs	14.12μs
	1 - 8bits	4.72μs	23.60μs
1	X - 8bits	9.44μs	28.32μs

Note: T_process defined timing in "process" is varied with RF input amplitude.

ADC Conversion Time for ADC_FastMode and ADC_RsIn Configurations

For FieldDetect operation, the basic timing is quite similar to CardDetect operation. The timing is shown in the following figure. The different point is that in "sense" period, transmitter is still disabled to sense external RF field. When operation is completed, IdleIRq is set. And if the value of register ADC_Result_I (Sector0-0x26) or ADC_Result_Q (Sector0-0x27) are beyond threshold level, RxIRq will be set.



Basic Timing for FieldDetect Mode

The configuration of ADC_Delay and CDTxDelay are shown in the following tables respectively.

ADC_Delay[1:0]	ADC Delay Time
00	76μs
01	151μs
10	227μs
11	302μs

ADC Delay Time for Analog Signal Settling

CDTxDelay	TX Delay Time
0	2.36μs
1	4.72μs

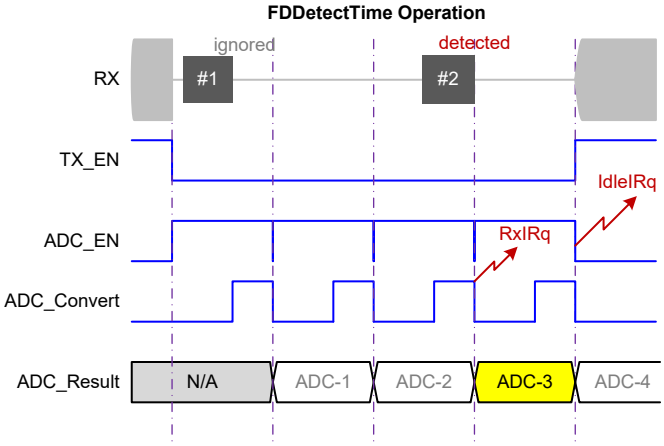
Transmitter Delay Time for RF Signal Settling

For more accurate measurement for both CardDetect and FieldDetect modes, the average function is implemented in the circuit. The control circuit repeats conversion phase multiple rounds and collects ADC output, ADC_Out, for each round. Then it calculates average value before returning ADC_Result. The number of average times for CardDetect mode is controlled by CDAverage bits (Sector0-0x31.[1:0]). While FDAverage bits (Sector0-0x30.[1:0]) defines average times for FieldDetect Mode. The average configuration is shown in the following table.

CDAverage [1:0]	Card Detection Average Time	FDAverage [1:0]	Field Detection Average Time
00	1	00	1
01	2	01	2
10	4	10	4
11	8	11	8

Average Time Configuration for CardDetect and FieldDetect Mode

In FieldDetect mode, if external RF source emits RF for a short time, like NFC phone, the device sometimes is unable to sense the external field. The FDDetectTime bits (Sector0-0x30.[6:4]) increases the possibility to catch up the field by repeating the Field Detection operation as shown in the following figure. The first external RF burst (#1) does not appear in the conversion period (ADC_Convert=1), threfore it is ignored. However, the second burst (#2) occurs in the sense period and can be detected by the device. If the third ADC_Result, ADC-3, is more than FDThreshold, RxIRq will be set. The number of repeating time is described in the following table.



Field Detection Operation when FDDetectTime="010"

FdDetectTime [2:0]	Repeating Times	FDDetectTime [2:0]	Repeating Times
000	1	100	16
001	2	101	32
010	4	110	64
011	8	111	128

FDDetectTime Configuration

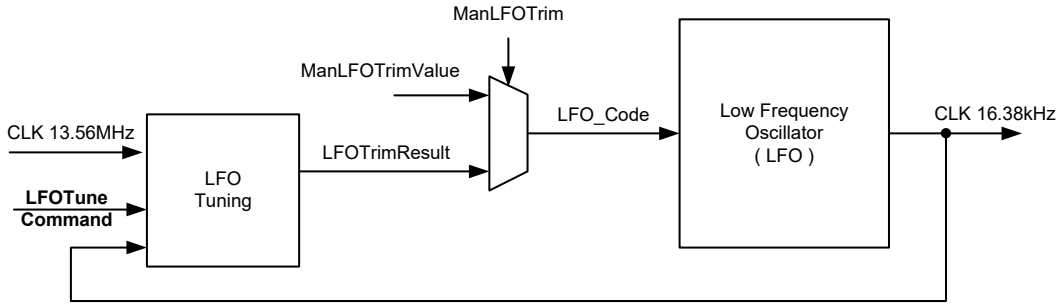
Normally, the system offset may induce error to conversion result. ADCCalibrate command should be prior executed to measure system offset and keep in internal buffer.

The registers associated with the RF amplitude detector are summarized in the following table.

Register	Address.Bit	Indication	Type	Default Value
ADC_Rsln	Sector0-0x25.1	Configure ADC resolution which defines RF amplitude input at RX pin	Read/Write	1
ADC_FastMode	Sector0-0x25.2	Define ADC mechanism and timing for conversion	Read/Write	0
ADC_FullScaleAdj	Sector1-0x05.[1:0]	Define maximum input RF amplitude at pin RX for ADC	Read/Write	00
FD_MinLvl	Sector0-0x25.3	Define step size of ADC in Field Detection operation	Read/Write	0
ADC_Delay	Sector0-0x25.[5:4]	Define delay time for starting ADC conversion after all related analog circuits are enabled	Read/Write	10
CDTxDelay	Sector0-0x31.2	Define wait time for RF amplitude settle, after transmitter is enabled	Read/Write	1
CDAverage	Sector0-0x31.[1:0]	Define the number of average time in each conversion in CardDetect Mode	Read/Write	00
FDAverage	Sector0-0x30.[1:0]	Define the number of average time in each conversion in FieldDetect Mode	Read/Write	00
FDDetectTime	Sector0-0x30.[6:4]	Define the number of repetitive Field Detection operation	Read/Write	100
ADC_Result_I	Sector0-0x26	ADC Conversion output, I-phase, which defines RF amplitude at pin RX from FieldDetect and CardDetect	Read Only	—
ADC_Result_Q	Sector0-0x27	ADC Conversion output, Q-phase, which defines RF amplitude at pin RX from FieldDetect and CardDetect	Read Only	—

Registers Associated with Field Detection and Card Detection

Low Frequency Oscillator



Low Frequency Oscillator and Tuning Block Diagram

The device contains tuneable low frequency oscillator, which generates clock 16.38kHz for wake up card detection system. The above figure shows the block diagram of oscillator system. Output clock frequency is tuneable by 8-bit LFO_Code signals, which is determined by ManLFOTrim bit (Sector1-0x03.0). If ManLFOTrim is set to 1, the value of ManLFOTrimValue (Sector1-0x02) is passed to LFO_Code. While clearing this bit to 0, the LFOTrimResult (Sector1-0x01) from automatic tuning system will be applied for tuning.

The LFO Tuning circuit trims output clock to desired frequency by comparing to the standard clock 13.56MHz. The tuning mechanism is start when LFOTune command is executed, or after the device is power up.

FIFO Buffer

The device contains a 64-byte FIFO for buffering input and output data stream between the external microcontroller and the internal codec. In normal transmission and reception to/from air, transmitted data should be written into the FIFO before executing. In contrast, reading received data from FIFO can be performed immediately after a single byte of data becomes available. Functions of registers associated with the FIFO are listed as below.

Register	Address.Bit	Indication	Set By	Clear By
FIFOData	Sector0-0x02	Input end and Output end of buffer for external microcontroller	—	—
FIFOLength	Sector0-0x04	Number of bytes already stored in the FIFO-buffer (distance between write-and read-pointer)	Write data to FIFO Read data from FIFO	Set FlushFIFO
HiAlert	Sector0-0x03.1	Flag to indicate amount of data in FIFO ≥ (64 - WaterLevel)	FIFO ≥ (64 -WaterLevel)	FIFO < (64 - WaterLevel)
LoAlert	Sector0-0x03.0	Flag to indicate amount of data in FIFO ≤ WaterLevel	FIFO ≤ WaterLevel	FIFO > WaterLevel
HiAlertIEn	Sector0-0x06.1	HiAlert interrupt enable	External Controller	External Controller
LoAlertIEn	Sector0-0x06.0	LoAlert interrupt enable	External Controller	External Controller
HiAlertIRq	Sector0-0x07.1	HiAlert interrupt flag	HiAlert changes from 0 to 1	External Controller
LoAlertIRq	Sector0-0x07.0	LoAlert interrupt flag	LoAlert changes from 0 to 1	External Controller
FIFOOvf	Sector0-0x0A.4	Flag to indicate FIFO was written while FIFO is already full	Write FIFO while FIFOLength=64	Set FlushFIFO
FlushFIFO	Sector0-0x09.0	Clear FIFO. FIFOLength becomes to zero	External Controller	—
WaterLevel	Sector0-0x29	Define the level of FIFO for overflow and underflow warning	External Controller	—

Registers Associated with FIFO

Writing to or reading from the FIFO can be performed through the register FIFOData (Sector0-0x02), while the amount of data remaining in the FIFO is shown by the register FIFOLength (Sector0-0x04). Handling data streams with lengths more than 64 bytes is possible by monitoring the status of flags LoAlert (Sector0-0x03.0) and HiAlert (Sector0-0x03.1), or using interrupt from LoAlertIRq (Sector0-0x07.0) or HiAlertIRq (Sector0-0x07.1). The LoAlert and HiAlert are warning flags indicating the amount of data in the FIFO has gone beyond boundary defined by WaterLevel (Sector0-0x29).

The warning flag HiAlert is set to 1 by the following equation:

$$\text{FIFOLength} \geq (64 - \text{WaterLevel})$$

The warning flag LoAlert is set to 1 by the following equation:

$$\text{FIFOLength} \leq \text{WaterLevel}$$

The FlushFIFO is a write-only bit for content clearance, and resetting the FIFOLength and FIFO-overflow flag FIFOOvf to zero. To properly access the FIFO, the external microcontroller has to know commands being executed and current states of the internal codec. When the internal state machine of the device grasps either the input end or the output end of the FIFO, accessing such end is prohibited because the higher priority of the internal state machine prevents violated access/interrupt to an executing command. For example, when the device is in the receiving state, the FIFO is being written by the internal, the microcontroller cannot write data to the FIFO. Otherwise, such reading or writing to the FIFO will not be successful and wrong data may return. The following table gives an overview of FIFO accessing during command processing.

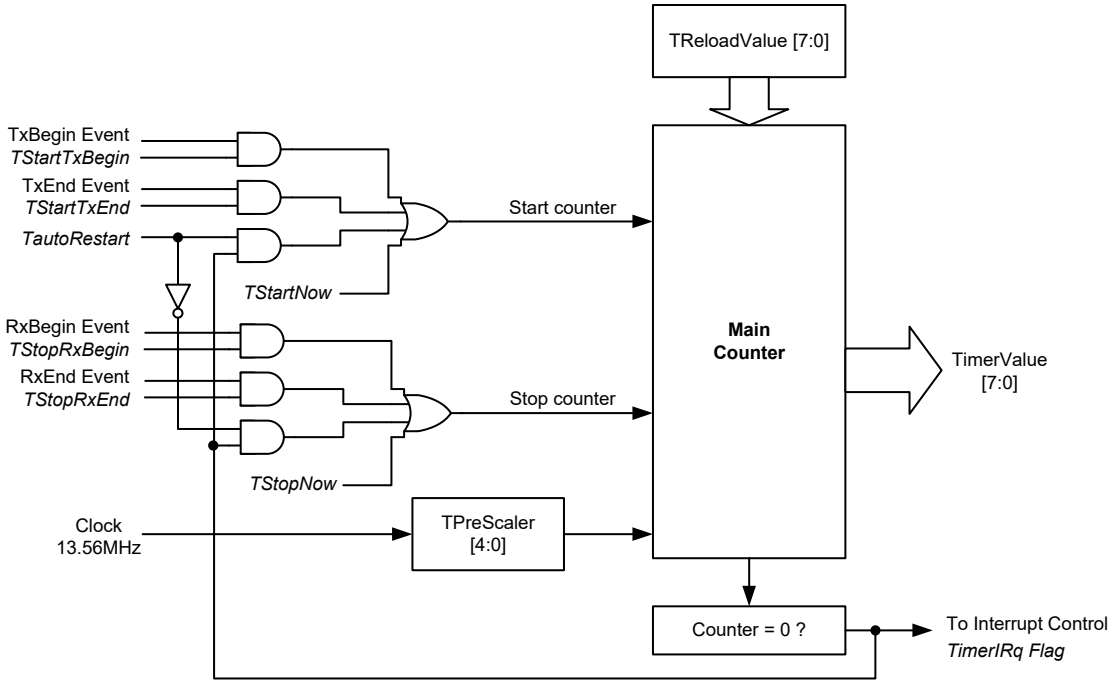
Command	Writing FIFO	Reading FIFO	Comment
Idle	OK	OK	Microcontroller can freely access the FIFO.
Transmit	OK	—	Appending data to the FIFO to transmit to air is possible as long as the codec is still in the transmission state.
Transceive	OK	OK	Microcontroller must know the operation state for accessing. Writing the FIFO is allowed in transmitting state. Reading the FIFO is allowed in receiving state. (More information in Transmit and Receive)
Receive	—	OK	Reading data from the FIFO as soon as data available is recommended to provide ample space of the FIFO especially in case of large amount of data transfer. However, the FIFOLength must be monitored to not interpret data from reading when the FIFO is empty (FIFOLength=0).
CalCRC	OK	—	Appending data to the FIFO to use in execution is possible as long as the command is in operating state.
LoadKeyFIFO	OK	—	
Authent	OK	—	
ReadSignature	OK	—	
RxFilterTune	OK	OK	Microcontroller can freely access the FIFO. No effect to the FIFO from executing this command
LFOTune	OK	OK	
ADCCalibrate	OK	OK	
CardDetect	OK	OK	
FieldDetect	OK	OK	

FIFO Accessible during Command Processing

Timer Unit

General Timer

The device contains a general timer unit where various events from the RF signal can trigger to start and stop. This feature aids the external microcontroller in monitoring RF events and enables interrupt-oriented programming. Especially in case of no response from air, interrupt from timer can indicate absence of the incoming signal within a given time. Conceptual diagram of the timer system is depicted in the following figure.



Timer Block Diagram

The timer system consists of a main counter, a clock prescaler, a zero-capturing comparator and an RF event trigger control. The main counter is an 8-bit count-down counter and decreases at the rate of the pre-scaled clock controlled by the prescaler register TPreScaler bit field (Sector0-0x2A.[4:0]), in a range from 0 to 21, and defined as shown in the relation below.

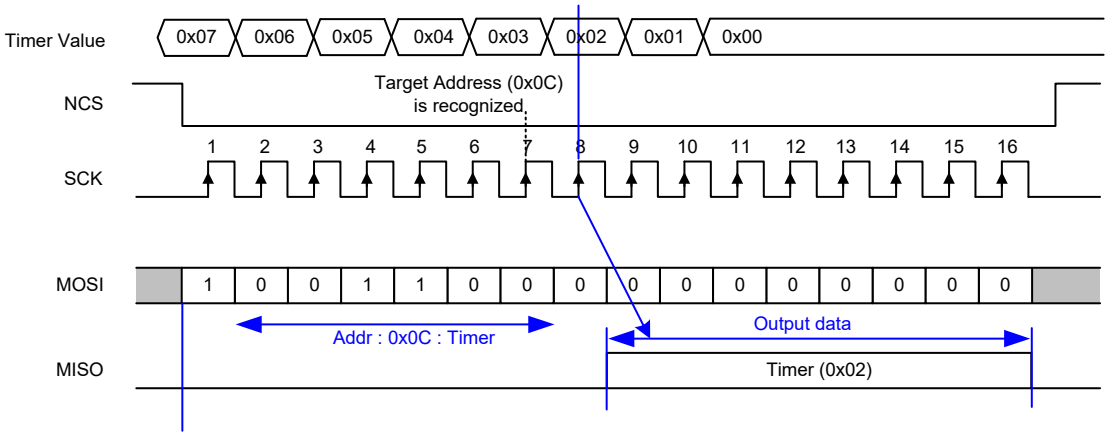
$$Tclk=(2^{TPreScaler})/13.56MHz$$

When the counter is started from defined events, the TReloadValue (Sector0-0x2C) is initialized to the counter. The timer is stopped when the counter value is equal to zero or defined stop event occurs. Once the timer counter value becomes to zero, the timer interrupt flag TimerIRq (Sector0-0x07.5) is set. So that the period for each TimerIRq events can be expressed below.

$$TimerIRq=TReloadValue\times(2^{TPreScaler})/13.56MHz$$

If TAutoRestart (Sector0-0x2A.5) is set, the TReloadValue will be reloaded into the main counter when the value in the main counter reaches 1. Then, this will generate interrupt request periodically. However, changing value in the TReloadValue during counting will not immediately affect the counter in the current round but it will exhibit in the next start of the trigger.

The external microcontroller can read the current value of the timer from the register TimerValue (Sector0-0x0C). As show in the following figure, the timer value transferring via SPI is latched in the eighth SPI clock after the address is recognized. Therefore, the timer value perceived by the microcontroller lags from the actual value by the period of SPI data transfer.



Point Timer Value is Latched

The timer can be controlled by events listed below.

- Manually start through setting the TStartNow bit (Sector0-0x09.1).
- Manually stop through setting the TStopNow bit (Sector0-0x09.2).
- Automatically start when
  - Transmission-beginning event occurs and the TStartTxBegin bit (Sector0-0x2B.0) is set.
  - Transmission-end event occurs and the TStartTxEnd bit (Sector0-0x2B.1) is set.
- Automatically stop when
  - Reception-beginning event occurs and the TStoptRxBegin bit (Sector0-0x2B.2) is set.
  - Reception-end event occurs and the TStopRxEnd bit (Sector0-0x2B.3) is set.

The definitions of ending and beginning in the transmission and reception are described in the following table.

Event	Definition
Transmission-beginning	Start of frame of downlink telegram begins to be transmitted
Transmission-end	End of frame or last bit of downlink telegram is transmitted
Reception-beginning	1st valid bit from uplink is received
Reception-end	End of frame of uplink telegram is received or Error occurs during receiving

Definitions of Beginning and End in the Transmission and Reception

Apart from using a time-out feature for no-card-response indicator, the timer can be used for programmable one-shot or periodic trigger. The registers associated with the timer are summarized as follows.

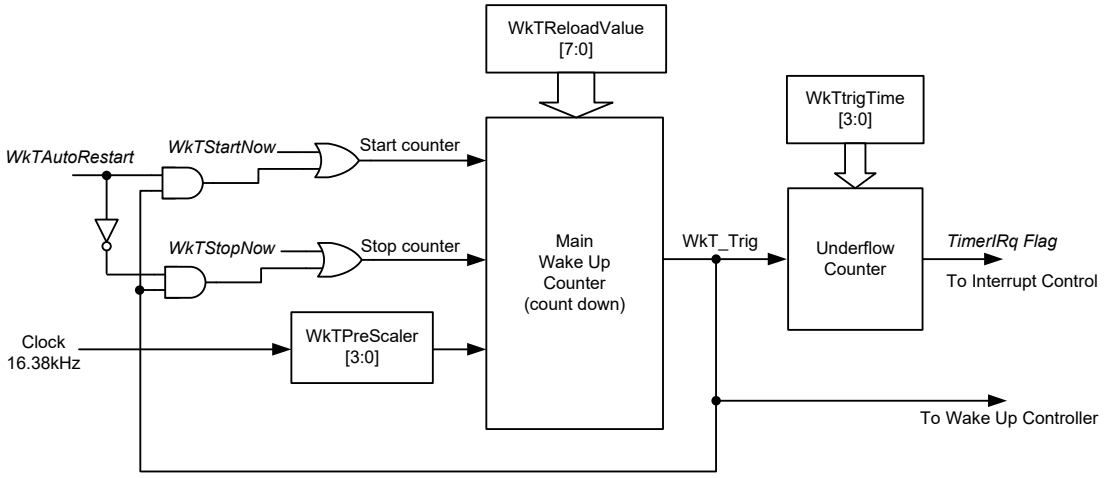
Register	Address.Bit	Indication	Type	Default Value
Trunning	Sector0-0x05.7	The timer is operating	Read Only	0
TimerIEn	Sector0-0x06.5	The timer interrupt enable	Read/Write	0
TimerIRq	Sector0-0x07.5	The timer interrupt request occurring if the timer value reaches 0	Read/Write	0
TStopNow	Sector0-0x09.2	Stop the timer immediately	Write Only	0
TStartNow	Sector0-0x09.1	Start the timer immediately	Write Only	0
TimerValue	Sector0-0x0C	Display the current timer value	Read Only	0xFF
TAutoRestart	Sector0-0x2A.5	Configure the timer to restart automatically after the counter reaches zero. The timer restarts from TReloadValue	Read/Write	0
TPreScaler	Sector0-0x2A.[4:0]	Clock Prescaler for timer clock	Read/Write	00111
TStopRxEnd	Sector0-0x2B.3	Set to stop the timer automatically after RX EOF is found	Read/Write	0
TStopRxBegin	Sector0-0x2B.2	Set to stop the timer automatically after RX SOF is found	Read/Write	1

Register	Address.Bit	Indication	Type	Default Value
TStartTxEnd	Sector0-0x2B.1	Set to start the timer automatically after TX EOF is transmitted	Read/Write	1
TStartTxBegin	Sector0-0x2B.0	Set to stop the timer automatically after TX SOF is transmitted	Read/Write	0
TReloadValue	Sector0-0x2C	Set the timer start values	Read Write	0x0A

Registers Associated with the General Timer

Wake Up Timer

In addition to the general timer explained above, the device has another timer, Wake Up Timer, that operates with low frequency clock 16.38kHz. This timer is used to control the timing operation in Wake Up Card Detection mode, that the device automatically alternates between Active and Power Down mode. The block diagram of Wake Up Timer is shown below.



Wake Up Timer Block Diagram

The system contains of two counters, a wake up counter and an underflow counter. A wake up counter is 8 bit count-down and decreases at the rate of pre-scaled clock which controlled by WkTPreScaler bit field (Secter0-0x2D.[3:0]). When the counter is started from writing WkTStartNow bit (Secter0-0x2D.7), the WkTReloadValue (Secter0-0x2E) is initialized to counter. Once the wake up counter decreases to zero, the WkT_Trig signal will be set. If WkTAutoRestart (Secter0-0x2D.4) is set, the WkTRelaodValue will be reloaded into a wake up counter and the counter will restart. So that the period of WkT_Trig event can be shown as follow.

$$TwkUp=WkTReloadValue \times (2^{WkTPreScaler})/16.38kHz$$

The WkT_Trig signal is sent to Wake Up controller for starting Active state in Wake Up Card Detection mode, described in "Wake Up Card Detection Mode" section. Furthermore, it also input trigger of an underflow counter. The underflow counter counts the number of WkT_Trig event, when the number of WkT_Trig equals to setting point configured by WkTtrigTime bit field (Sector-0x2F.[3:0]), it generates TimerIRq sent to interrupt control system. The setting point for underflow counter is expressed below.

$$WkT\_Trig\_number=2^{WkTtrigTime}$$

So that the TimerIRq period generated by Wake Up Timer can be defined as follow.

$$TwkIRq=(2^{WkTtrigTime})\times WkTReloadValue\times(2^{WkTPreScaler})/16.38kHz$$

Register	Address.Bit	Indication	Type	Default Value
WkTStartNow	Sector0-0x2D.7	Start the wake up timer immediately	Write Only	0
WkTStopNow	Sector0-0x2D.6	Stop the wake up timer immediately	Write Only	0
WkTRunning	Sector0-0x2D.5	The wake up timer is operating	Read Only	0

Register	Address.Bit	Indication	Type	Default Value
WkTAutoRestart	Sector0-0x2D.4	Configure the wake up timer to restart automatically after the counter reaches zero. The timer restarts from WkTReloadValue	Read/Write	1
WkTPreScaler	Sector0-0x2D.[3:0]	Clock Prescaler for wake up timer clock	Read/Write	1001
WkTReloadValue	Sector0-0x2E	Set the wake up timer start values	Read Write	0x20
WkTtrigTime	Sector0-0x2F.[3:0]	Define the number of wake up timer underflow event to create TimerIRq flag	Read/Write	0110

Registers associated with the Wake Up Timer

Power Management

The device offers schemes in reducing power during the idle state, namely Hard Power Down, Soft Power Down, Standby and Receiver Power Down and Wake Up Card Detection modes.

Hard Power Down Mode

If the RSTPD pin is set high, the device will enter the Hard Power Down mode. In this mode, all internal circuits are turned off. The input pin is disconnected from all input pins excluding the pin RSTPD itself. Also, accessing to FIFO and registers from the external microcontroller is inhibited. After releasing RSTPD to low, the device enters the initializing phase. The external microcontroller can start operating the device when the value in the Command register changes from Startup to Idle.

Soft Power Down Mode

The Soft Power Down mode is enabled by setting the bit PowerDown (Sector0-0x09.4) in the Control register. In this mode, all internal circuits are turned off but the input and output pins still remain their functionalities. After the PowerDown is cleared by the external microcontroller, it takes 1024 clocks, counting from the internal circuit that can detect the first clock signal, for the clock stable period before leaving this mode. The device will completely leave the Soft Power Down mode, if PowerDown, where the external microcontroller can monitor, resets itself to zero. If the internal oscillator is used, the time for the oscillator to start-up including clock stable period is typically around 2ms. Accessing neither FIFO nor registers is allowed except the Control register during this power down mode.

Standby Mode

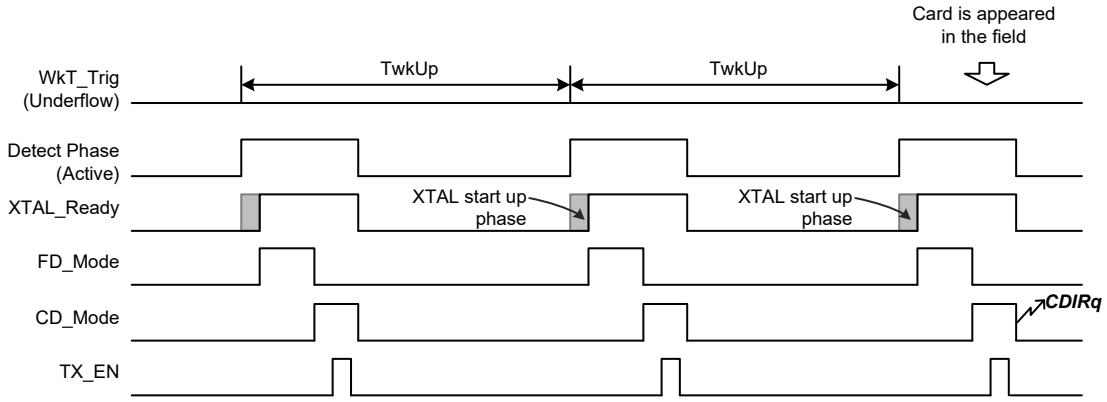
The Standby mode is enabled when the bit Standby (Sector0-0x09.5) in the Control register is set. In this mode, all internal circuits except the internal oscillator are turned off. After clearing Standby by the microcontroller, it takes 4 clocks to leave this mode. Therefore, this mode is suitable for applications which requires fast wake-up. The input and output pins still remain their functionalities as same as that of the soft power down mode.

Receiver Power Down Mode

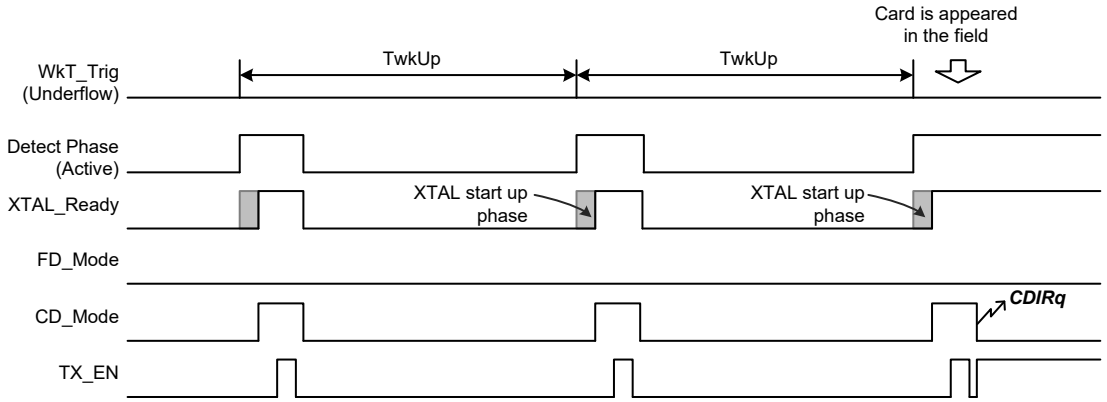
The receiver power down mode is a power saving mode that turns the receiver circuit off when it is not required for operations, such as in Transmit state or Idle state. By setting the bit RxAutoPD (Sector0-0x1E.6) in RxControl2 register, the receiver is only active in the RxPrepare and Receiving states. If this bit is cleared, the receiver circuit will always be turned on. It is recommended to enable this mode.

Wake Up Card Detection Mode

The Wake Up Card Detection mode, WkUpCD, is enabled when WkUpCD bit (Sector0-0x09.6) is set. In this mode, the device is not fully powered constantly. The WkUpCD operates in two phases, Sleep and Detect. In Sleep phase, the operation is similar with Soft Power Down Mode, which all internal circuit is turned off except low frequency oscillator (LFO) and Wake Up Timer. In other phase, Detect phase, the device will sense and detect RF signal at RX pins by turn on receiver and transmitter.



WkUpCD Mode Example Timing Diagram when WkFDEn=1 and WkCDGoActive=0

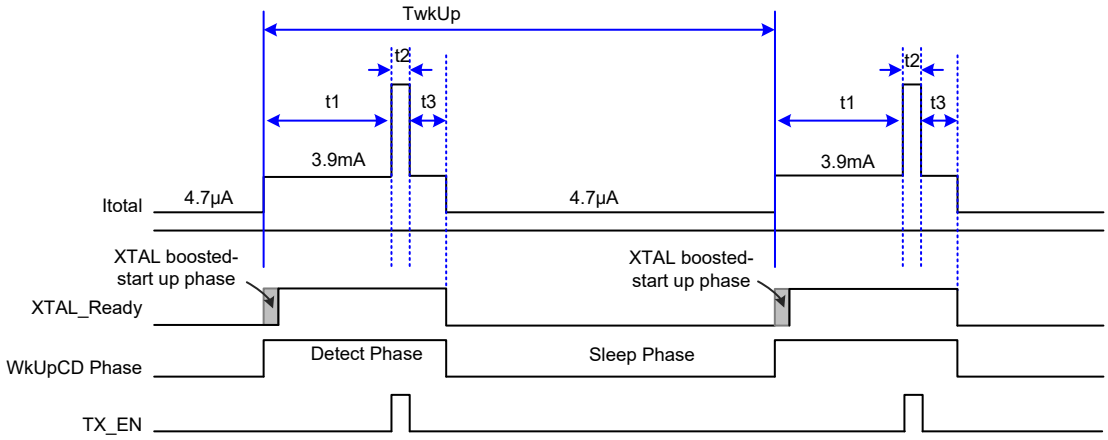


WkUpCD Mode Example Timing Diagram when WkFDEn=0 and WkCDGoActive=1

The two figures above show the example timing of WkUpCD mode. When WkT_Trig signal from wake up counter is asserted, the device will change from Sleep phase to Detect phase. The system waits until clock from crystal oscillator is stabled, XTAL_Ready="1", for starting the sequence. If WkFDEn bit (Sector0-0x31.4) is cleared, the system skips FieldDetect mode and directly executes CardDetect mode. When WkFDEn bit (Sector0-0x31.4) is set, FieldDetect mode is firstly executed to prevent RF Field collision. If external RF field is occurred, RxIRq is set and system will go to Sleep phase immediately. On the other side, if external RF level is lower than set FDThreshold, CardDetect mode is executed.

After CardDetect mode is finished, the CDIRq is set when measured RF amplitude is fluctuated beyond CDThreshold level. The system re-enters Sleep phase when WkCDGoActive bit (Sector0-0x31.6) is cleared. If WkCDGoActive is set and CdIRq is set, the system will automatically go to active state and ready to execute further operation.

The current consumption load profile in the Wake Up Card Detection mode is roughly shown in following figure. After WkTimer is underflowed, the device is woken up. In t_0 phase, initial wake up, current consumption and period are depended on crystal oscillator start up time. At t_1 period, the internal circuit is enabled and delay for voltage stable before measurement. While transmitter is enabled with a short time configured by CDTxDelay, t_2 period, the additional current consumption from transmitter is depended on antenna tuning. The last t_3 period is ADC conversion period depends on configuration. The timing, t_1, t_2 and t_3 can be configured by register described in the "RF Amplitude Detector System" section.



Current Load Profile in Wake Up Card Detection Mode

The register related to Wake Up Card Detection mode is shown as follow.

Register	Address.Bit	Indication	Type	Default Value
WkCDGoActive	Sector0-0x31.6	Define operation in WkUpCD mode when CDIRq is set 0: Device remains in WkUpCD mode 1: Device automatically goes to active state	Read/Write	0
WkIgnoreFD	Sector0-0x31.5	Define operation in WkUpCD mode when WkFDEn is set and external RF field is detected, RxIRq="1" 0: Device skips Card Detection operation 1: Device still executes Card Detection operation	Read/Write	0
WkFDEn	Sector0-0x31.4	Enable Field Detection operation in WkUpCD mode	Read/Write	1
WkTStartNow	Sector0-0x2D.7	Start the wake up timer immediately	Write Only	0
WkTStopNow	Sector0-0x2D.6	Stop the wake up timer immediately	Write Only	0
WkTRunning	Sector0-0x2D.5	The wake up timer is operating	Read Only	0
WkTAutoRestart	Sector0-0x2D.4	Configure the wake up timer to restart automatically after the counter reaches zero The timer restarts from WkTReloadValue	Read/Write	1
WkTPreScaler	Sector0-0x2D.[3:0]	Clock Prescaler for wake up timer clock	Read/Write	1001
WkTReloadValue	Sector0-0x2E	Set the wake up timer start values	Read/Write	0x20
WkTtrigTime	Sector0-0x2F.[3:0]	Define the number of wake up timer underflow event to create TimerIRq flag	Read/Write	0110

Registers Associated with the WkUpCD Mode

Interrupt System

The device is comprised of seven sources of interrupts available to serve interrupt-oriented programming. The interrupts indicate key events related to the BC45B4523 peripherals, i.e., CODEC, FIFO, ADC and timer. When the interrupt requests occur, they are reported in three ways: a register InterruptFlag (Sector0-0x07), a bit IRQ (Sector0-0x03.3) in PrimaryStatus register and a signal level on pin IRQ. If one of the interrupt flags in the InterruptFlag register is set while its corresponding interrupt enable bit (0-0x06.x) is also set, the register bit IRQ will be set and the pin IRQ will toggle to its active state. Polarity of the pin IRQ can be suitably set either active high or low for the microcontroller by the register IRQInv (0-0x39.0). The following table summarizes indications of the interrupt flags and suggested next actions for the microcontroller. To set or clear bits in the InterruptFlag or InterruptEnable register, the external microcontroller can perform through writing the target interrupt bit with writing-control bits SetIEn or SetIRq (Sector0-0x06.7 or Sector0-0x07.7) respectively. If SetIEn or SetIRq is written by value 1, the set bits in InterruptEnable or InterruptFlag will be set. The unset bit in such register remains unchanged. Also, if SetIEn or SetIRq is written by value 0, the set bits in InterruptEnable or InterruptFlag register will be cleared. Multiple bits of InterruptFlag or InterruptEnable register can be written concurrently. For example, writing 0x7F to the InterruptEnable register clears all interrupt enable bits. Writing 0xFF to the InterruptEnable

register sets all interrupt enable bits. The InterruptFlag is usually set by the internal state machine and cleared by the external microcontroller, while InterruptEnable is always set and cleared by the external microcontroller.

Interrupt Flag	Indication when Interrupt is Set	Suggested Action for Microcontroller
CDIRq	In Card Detection operation, both direct command or WkUpCD mode ADC_Result > CDThreshold_H or ADC_Result < CDThreshold_L	Begin to start RF communication
TimerIRq	General Timer (13.56MHz) decreases from 1 to 0 or set-up time is up	Investigate cause of time out
	Wake Up Timer (16.38kHz) underflow counter is decreased to 0	
TxIRq	One of these events in these commands occurs - Transmit: All data have been transmitted - Transceive: All data have been transmitted	Start Receive command or start other commands
	One of these events in these commands occurs: - RxFilterTune: Tuning process is finished - CalCRC: All data have been processed	Begin to start other commands
	One of these events in these commands occurs: - LoadKeyFIFO: Key is already in buffer	Start Authent command
RxIRq	Receiver finishes reception in both cases of successful and error	Read Data from the FIFO Investigate received data and process for the next transmission
	In Field Detection operation, both direct command or WkUpCD mode ADC_Result > FDThreshold_H	Turn off RF to avoid RF collision
IdleIRq	Operation of command is finished and state is changed to idle. End of operation of all commands causes IdleIRq set to 1. Setting power down or standby during executing or starting Idle command does not set IdleIRq.	Begin to start other commands
HiAlertIRq	The FIFO is getting full and FIFOLength ≥ 64 - WaterLevel	Read Data from the FIFO to prevent the FIFO Full
LoAlertIRq	The FIFO is getting empty and FIFOLength ≤ WaterLevel	Write Data to the FIFO if need

Source of Interrupt Trigger and Suggested Action for Microcontroller

Crypto_M Engine

The device incorporates a Crypto_M engine to encrypt the transmitted data and decrypt the received data. A diagram of transmission and reception systems with a crypto engine is shown below. Before processing encryption and decryption in read/write operations from/to Crypto_M card, the 48-bit keys of the data section being accessed in the card must be previously loaded to the key buffer and the authentication process must be successful. The following block diagram shows inter-block activities for commands associated with key loading. Bit Crypto_MOn (Sector0-0x09.3) indicates the completion of the authentication process. This Crypto engine is only applicable for transactions in ISO14443A at 106kbps.

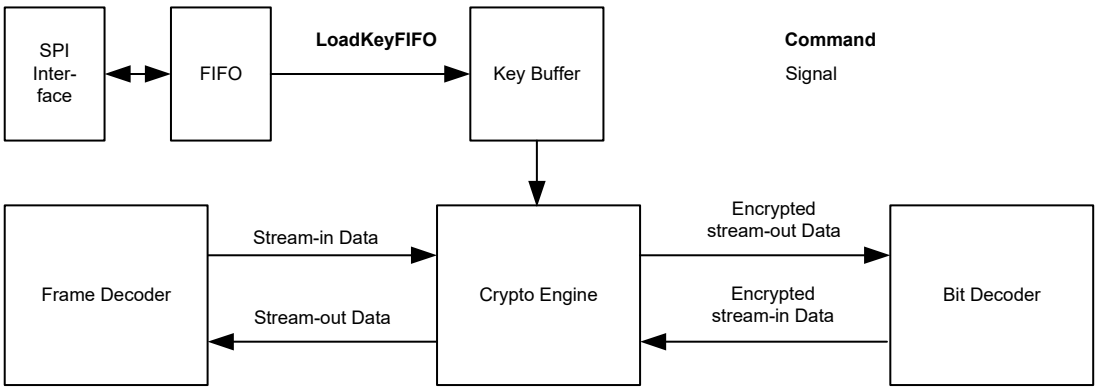
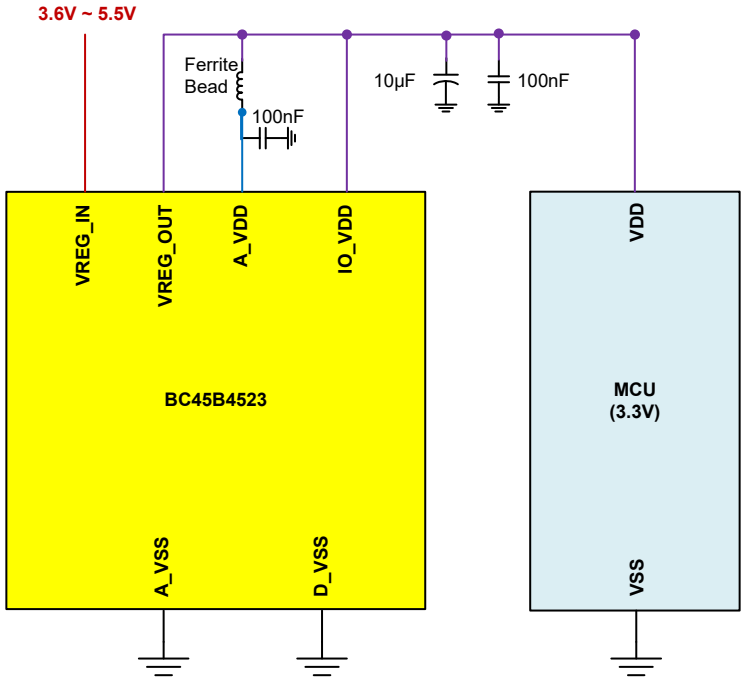


Diagram of Transmission and Reception Systems with a Crypto Engine

Regulator

The device contains an ultra low quiescent current on-chip 150mA regulators, which provides an output voltage of 3.3V. The typical connection is shown in the following figure. A 100nF ceramic capacitor and a 10μF tantalum capacitor are suggested to connect to the regulator output pin VREG_OUT for stability and supplying high frequency current to a particular section. As shown in the following figure, the output connects to analog power supply pin (A_VDD), digital input/output power supply pin (IO_VDD) of the device and also external microcontroller. In applications where noise is a major concern, for example, mid/long-range readers, ferrite beads can be inserted in supply buses to attenuate interference among each other. The electrical parameters are defined in the "Regulator Characteristics". More important point, the regulator also generates additional heat due to drop-in voltage and current passing through. This amount of heat must be taken into account for heat dissipation design.



Typical Power Supply Connection

Commands

To perform RF interface or internal activities of the device, an external microcontroller has to write a specific command to the Command register (Sector0-0x01). Available commands and input/output data associated with the FIFO are summarized in the following table.

Command	Code	Action	Input Data Required in FIFO	Return Data Read from FIFO
Startup	0x30	Indicate external microcontroller that the device is in initializing state	—	—
Idle	0x00	Idle or cancel current executing command except LoadKeyFIFO	—	—
Transmit	0x1A	Transmit data in the FIFO buffer to air	Data stream	—
Receive	0x16	Enable receiving circuit and decode signal from air into data in the FIFO	—	Data stream
Transceive	0x1E	Transmit Data in the FIFO buffer to card and enable receiving circuit after transmission complete. Then, put the received data into the FIFO	Data stream	Data stream

Command	Code	Action	Input Data Required in FIFO	Return Data Read from FIFO
CalCRC	0x12	Perform CRC calculation from available data in the FIFO	Data stream	—
LoadKeyFIFO	0x19	Read data in the FIFO and put into the key buffer. Key data must be in the specific format	Byte0 (LSB) + Byte1+… +Byte10+Byte11	—
Authent	0x1C	Execute authentication to turn crypto engine on	Tag's Authent command + Tag's Block Number + Tag's UID(LSB) + … +Tag's UID(MSB)	—
RxFilterTune	0x10	Execute receiver filter corner frequency tuning process	—	—
LFOTune	0x20	Execute low frequency oscillator tuning process	—	—
ADCCalibrate	0x21	Perform ADC Calibration for RF amplitude detector system	—	—
CardDetect	0x22	Perform Card Detection operation by enabling transmitter and measure RF input amplitude at pin RX	—	—
FieldDetect	0x23	Perform Field Detection operation by disableing transmitter and measure external RF input amplitude at pin RX	—	—
ReadSignature	0x31	Execute read out device signature	MaskSet + ProductionParam + Revision	—

BC45B4523 Commands

Startup Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x30	Indicate external microcontroller that the device is in initializing state	—	—	—

The Startup command is started by the internal state machine automatically after reset. It is used to indicate the external microcontroller that the device is initializing and the external microcontroller should wait until the Command register switches from the Startup to 0x00 (idle state) before performing any execution. This command is for the internal state machine only, users cannot start this command from the external microcontroller.

Idle Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x00	Idle or cancel the current executing command except LoadKeyFIFO	—	—	—

The Idle command stops the current executing command. Consequently, the current state is set to idle state while non-processing data in the FIFO buffer remains unchanged. Note that the IdleIRq flag in the InterruptFlag register is not set by the activation of this command. However, LoadKeyFIFO command is not affected from issuing Idle. The command still continues to operate to prevent detrimental effects to the IC system i.e. memory damage.

Transmit Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x1A	Transmit Data in FIFO buffer to card	Data stream	—	TxIRq, IdleIRq

The Transmit command conveys data from the FIFO buffer to the transmitter to modulate carriers. The RF bit pattern of the transmitted data is formed by following the defined protocol, configurable in transmitter-related register page (page 2). Basically, there are two basic schemes in transmitting data on air: Write-FIFO-before-Transmit and Transmit-before-Write-FIFO. Assuming that the current state of the codec is idle; steps and results of both schemes are described below.

Step		Results
1	Write data to be transmitted to the FIFO	- Data is in the FIFO
2	Write Transmit to the Command Register	- Data in the FIFO is transmitted on air until the FIFO is empty - The TxIRq and IdleIRq interrupt flags are set

Transmit Command: Write FIFO before Transmit

The maximum data that can be transferred by this "Write-FIFO-before-Transmit" method is 64 bytes.

Step		Results
1	Write Transmit to the Command Register	- The CODEC is in a transmission preparation state
2	Write data to be transmitted to FIFO	- The CODEC starts transmission as soon as the first byte is written to the FIFO - Data in the FIFO is transmitted as long as the FIFO is not empty - The CODEC stops transmission and appends EOF when the FIFO has reached empty state - The TxIRq and IdleIRq interrupt flags are set

Transmit Command: Transmit before Write FIFO

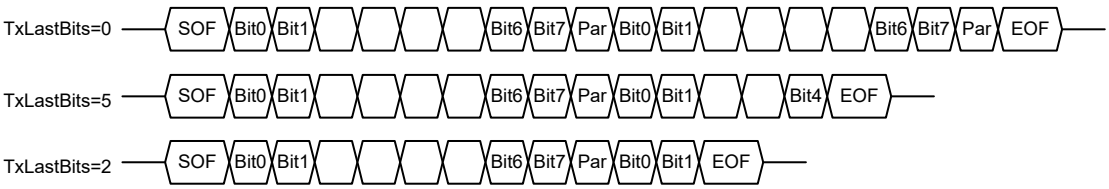
This method continues transmission as long as the data of the next byte still available in the FIFO. This method allows transmission of the data more than 64 bytes. The microcontroller must put the data stream in the FIFO buffer soon before the FIFO becomes empty. A combination of these two methods, which is writing some data to the FIFO first and appending after transmission, is possible. It does yield an effective transmission for long data stream. If no more data available in the FIFO, the CODEC appends CRC and EOF at the end, and switches to idle state. The state machine leaves the transmission state to idle state, and the TxIRq and IdleIRq flags are set.

CRC and Parity

The transmission telegram can be composed of CRC and parity bits, by enabling the bit TxCRCEn and the bit ParityEn in ChannelRedundancy register (Sector0-0x22). The CRC result is relied on the CRC calculation method in the MSBFirst, CRC3309 bits and preset values in CRCPresetLSB and CRCPresetMSB registers. If TxCRCEn is set, two CRC bytes are appended following the last byte from the FIFO. Except the bit-oriented transmission and the short frame in ISO14443A, the TxCRCEn should be used in all protocols. If the bit ParityEn in ChannelRedundancy register is set, parity bits are inserted between each transmitted byte in the telegram. The polarity of the parity bit is controlled by the ParityOdd bit in the ChannelRedundancy register. The parity bit is only allowed in ISO14443A.

Bit-Oriented Transmission in ISO14443A

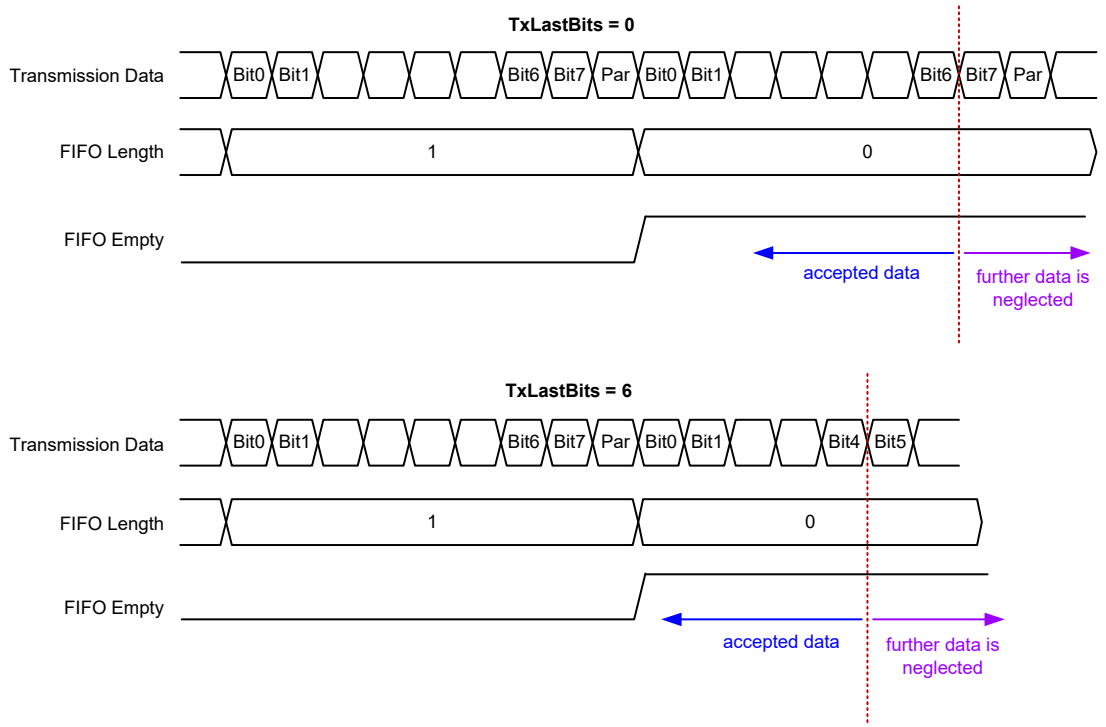
For bit-oriented transmission in ISO14443A, the number of bits in the last transmitted byte can be controlled via the TxLastBits bit field in the register BitFraming (Sector0-0x0F). The TxLastBits is a three-bit bit field, its value reflects the number of bits in the last byte. Only the least significant bit of the last byte following the defined number is transmitted. If the TxLastBits bit field value is cleared to 0, the whole last byte will be transmitted. The following figure illustrates the example of bit-oriented transmission telegram with effect of TxLastBits. The TxLastBits is only applicable to the ISO14443A setting and have no effect on other standard settings.



Effect of TxLastBits in Bit-Oriented Transmission Telegram (Assuming two bytes in the FIFO)

Transmission Timing

In case of transmitting data more than 64 bytes, the external microcontroller must input data to the FIFO during transmission before the last bit, where the FIFOLength is zero, is transmitted on-air. To transfer data without interruption, the FIFO level monitoring through low-alert interrupt must be employed. New data written after last-bit transmission is neglected and remains in the FIFO. If TxLastBits bit field value is not equal to "0", the data for transmission must be available in the FIFO before the indicated last bit is transmitted. The following figure illustrates the time line that the codec decides to end or continue the transmitting stream.



Timing for Appending Data before Transmission End

Sent1Pulse

In ISO15693, there is a requirement to send a single RF gap on air to indicate next slot during anti-collision. Regardless of data in the FIFO, setting bit Sent1Pulse (Sector0-0x14.7) and then writing Transmit to the Command register produces a gap on the RF signal. Note that it is required that CoderRate[2:0] and TxCoding[2:0] must be set in ISO15693 mode.

Register Related to Transmission

The registers related to transmission and transmitter configurations are summarized in the following table.

Register	Address.Bit	Indication/Usage	Type	Default Value
Command	Sector0-0x01	Activate Transmit or Transceive command	Dynamic	0x00
TxIEn	Sector0-0x06.4	Configure interrupt enable for TxIRq	Read/Write	0
TxIRq	Sector0-0x07.4	Indicate data was transmitted	Dynamic	0
TxLastBits	Sector0-0x0F.[2:0]	Define the number of bits in the last transmitted byte	Dynamic	000
TxControl	Sector0-0x11	Configure driving behaviour of the transmitter	Read/Write	0x18
TxCfgCW	Sector0-0x12	Configure output conductance of the transmitter during carrier transmission	Read/Write	0x3F
TxCfgMod	Sector0-0x13	Configure output conductance of the transmitter during carrier modulation	Read/Write	0x10
Send1Pulse	Sector0-0x14.7	Configure to sent 1 pulse in ISO15693	Read/Write	0

Register	Address.Bit	Indication/Usage	Type	Default Value
CoderRate	Sector0-0x14.[5:3]	Configure transmitter data rate	Read/Write	011
TxCoding	Sector0-0x14.[2:0]	Configure transmitter coding	Read/Write	001
ModWidth	Sector0-0x15	Define modulation width of data bit in ISO14443A and ISO15693	Read/Write	0x0F
ModWidthSOF	Sector0-0x16	Define modulation width of SOF bit in ISO14443A and ISO15693	Read/Write	0x0F
NoTxSOF	Sector0-0x17.7	Suppress SOF transmission in ISO14443B	Read/Write	0
NoTxEOF	Sector0-0x17.6	Suppress EOF transmission in ISO14443B	Read/Write	0
EOFWidth	Sector0-0x17.5	Define width of EOF in ISO14443B	Read/Write	1
CharSpacing	Sector0-0x17.[4:2]	Define the number of EGT in ISO14443B	Read/Write	110
SOFWidth	Sector0-0x17.[1:0]	Define width of SOF in ISO14443B	Read/Write	11
MSBFirst	Sector0-0x22.6	Define method in calculation CRC	Read/Write	0
CRC3309	Sector0-0x22.5	Define method in calculation CRC	Read/Write	0
CRC8	Sector0-0x22.4	Define method in calculation CRC	Read/Write	0
TxCRCEn	Sector0-0x22.2	Enable CRC in transmitted frame	Read/Write	0
ParityOdd	Sector0-0x22.1	Set odd parity in transmitted frame	Read/Write	1
ParityEn	Sector0-0x22.0	Enable parity in transmitted frame	Read/Write	1
CRCPresetLSB	Sector0-0x23	Define preset CRC value in LSB	Read/Write	0x63
CRCPresetMSB	Sector0-0x24	Define preset CRC value in MSB	Read/Write	0x63

Register Related to Transmission

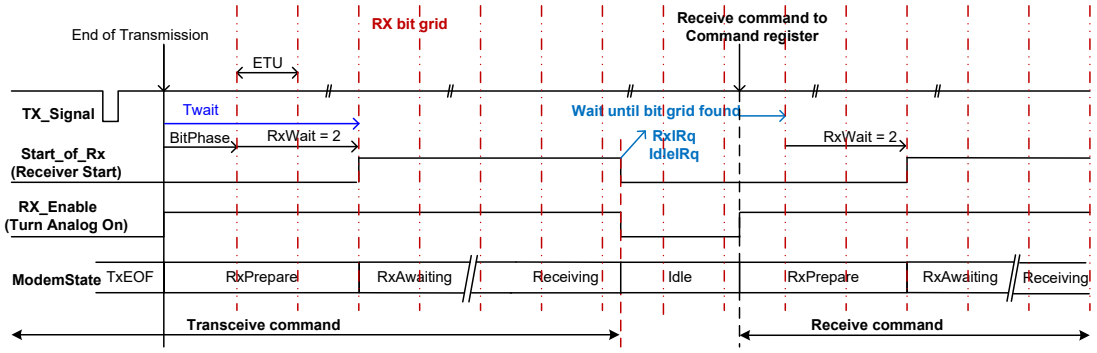
Receive Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x16	Enable Receiving circuit	—	Data stream	RxIRq, IdleIRq

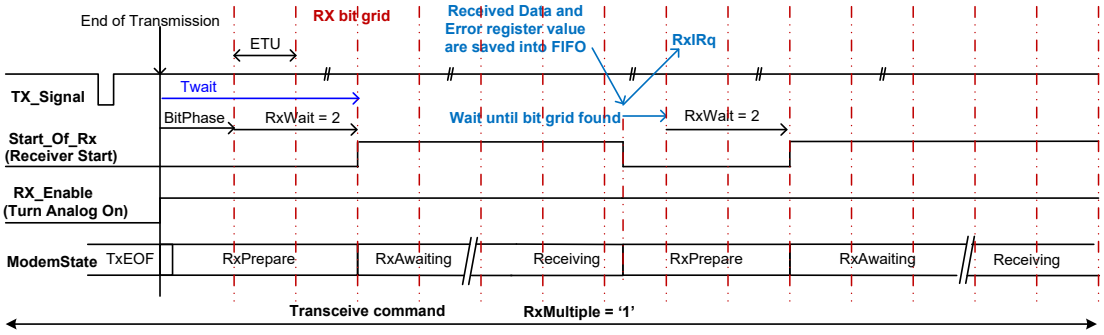
The Receive command starts the receiver circuit and returns decoded data in byte to the FIFO. Also, the Receive command, starting automatically after the transmission has finished, is the second part of Transceive command.

After executing the Receive command from SPI, the CODEC state-machine changes to “RxPrepare” state and delays start of the receiver by the number of ETU defined in register RxWait (Sector0-0x21). If the Receive command is automatically issue as a part of the Transceive command, the time delay defined by register BitPhase (Sector0-0x1B) will be inserted to adjust RX bit grid suitably align for tag response. The timing in the “Timing of Transceive and Receive Command” figure shows behavior of Receive command in the device. Firstly, the receiver is restarted synchronously to the previous running RX bit grid, referring from end of last transmission. Then, state changes to “RxAwaiting” state and CODEC looks for the data pattern that matches the predefined SOF. Once the SOF is detected, the state machine changes to “Receiving” state and continues to decode the incoming signal into data byte and store in the FIFO. The state machine leaves “Receiving” state if no further data is received or an error occurs during receiving. If the bit RxMultiple (Sector0-0x1A.7) is cleared, the state will change to “Idle” state and the RxIRq and IdleIRq will be set. On the other hands, if the bit RxMultiple is set, only the RxIRq will be set. Then, the state returns to “RxPrepare” state and delay start of receiver following register RxWait, which also synchronize to the previous RX bit grid as shown in “Timing of Transceive Command with RxMultiple Bit is Set” figure.

For long received data stream more than 64 bytes, the microcontroller must manage FIFO accessing routine to prevent overflow. Therefore, HiAlert interrupt can be employed in monitoring. The state of reception is shown in the State diagram presented in the “State Machine” section. Note that the analog receiver circuitry requires time to initialize and warm-up before decoding signal. It is necessary to set the register RxWait with the minimum value for RxWait of 3.



Timing of Transceive and Receive Command



Timing of Transceive Command with RxMultiple Bit is Set

CRC and Parity

If the bit RxCRCEn in the ChannelRedundancy register is set to expect CRC in received telegram, the last two bytes of the received frame will be treated as a CRC of the preceding data stream. If the received CRC is identical to the calculated CRC from the CODEC, the preceding received data is successful without a CRC error and the CRC is not loaded to the FIFO buffer. The result of CRC is displayed in registers CRCResultLSB and CRCResultMSB. On the other hand, the received mismatched CRC will be forwarded to the FIFO and the bit CRCErr in the Error register (Sector0-0x0A) will be set.

In case of parity, if the bit ParityEn is set in the ChannelRedundancy register, the parity is expected after the end of each byte. If the received parity is not equal to the expected setting from the bit ParityOdd in the ChannelRedundancy register, the bit ParityErr in the Error register will be set. The parity checking only performs in ISO14443A standard. The ParityEn bit have no effect on reception of other standard settings.

Collision Detection

If more than one card presents in the same RF-field, the data collision will occur. If there is a collision, the bit CollErr in the Error Register will be set and the collision position of the received bit stream will be displayed in the collision position register CollPos (Sector0-0x0B). When collision occurs at parity bit, for ISO14443A Manchester pattern, both CollErr and ParityErr will be set, while the CollPos value will remains at the last uncollision bit position. Therefore, software should be checked both CollErr and ParityErr to acquire the correct collision position. The following table shows examples of CollPos values and the meaning of collision bits.

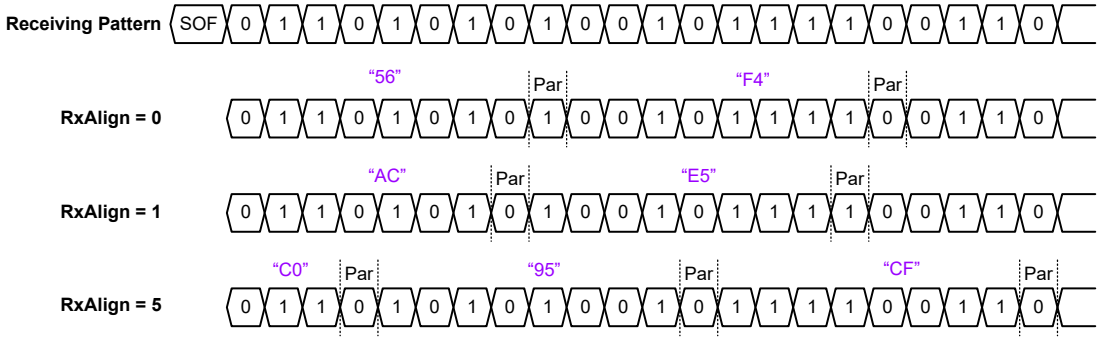
As stated in the above "Frame Decoder" chapter, the collided bits can be set to a value in CollMarkVal and the receiving bit after collision can be forced to zero by setting the bit ZeroAfterColl. This feature is to ease software in manipulating anti-collision mechanism in ISO14443A at the data rate of 106kbps and ISO15693 at all rates.

Position	CollPos Value	Comment
SOF	0	CollErr, FramingErr are set
1st bit of 1st byte	1	CollErr is set
2nd bit of 1st byte	2	
8th bit of 1st byte	8	
Parity of 1st byte	8	CollErr, ParityErr are set
1st bit of 2nd byte	9	CollErr is set
7th bit of 2nd byte	15	
Parity of 2nd byte	16	CollErr, ParityErr are set

Example of Collision Position and Reported Value of CollPos

Bit-Oriented Reception in ISO14443A

During anti-collision process in ISO14443A, the first received byte may be partially transmitted from the card. For reception of such split byte, RxAlign in the BitFraming register defines the first received bit position in the first decoded byte. The following figure shows the evaluated data byte when setting RxAlign to different values. Assume that the bit ParityEn equals to 1, if RxAlign is not equal to zero, the parity of the first byte is not checked.



Example of Evaluated Data for Different RxAlign Settings

Error in Reception

At the end of reception, some errors in reception are indicated via the error flags in the Error register. The meaning of the error flags related to the reception is described as follows.

Error Flag	Event
FramingErr	Invalid frame format, namely – SOF and EOF do not conform to the standard defined in the receiver. – EGT in ISO14443B is incomplete.
ParityErr	Wrong parity is received in ISO14443A
CRCErr	Wrong CRC is received
CollErr	Collision is detected in ISO14443A and ISO15693

Error Flags Related to RF Reception

EMD Suppression

Conventionally, to handle frame containing EMD, microcontroller must consider received frame if it is EMD by relying on interrupt signal after end of reception and already-received data in FIFO. Although, the RxMultiple bit or Receive command can assist this operation, such operation takes significant time from transaction between microcontroller and the device via SPI. Then, response time is quite long.

The device contains EMD suppression function, which is a feature designed to reduce microcontroller task in handling EMD frame reception. When bit EMD_Suppress (Sector0-0x1F.1) is set, if the number of received data byte is less than 3 bytes and frame contains errors related to reception, namely CRCErr, FramingErr, ParityErr, CollErr, system will automatically discard the received data and returns to "RxAwaiting" state to receive next frame as shown in the State diagram presented in the "State Machine" section. If the number of receiving byte is

more than 3 bytes, EMD suppression feature will not function because it is treated as normal data frame which is usually consisted of one data byte and two associated CRC. The EMD suppression is applicable for ISO14443A protocol, ISO14443B protocol, RxMultiple setting and Receive command. For some reception frame such as ATQA or part of UID in which response is less than 3 bytes and no error, received data will be passed to FIFO. Therefore, RxCRCEn shall be set correctly for expected response. When any suppression is detected, EMD_Det bit (Sector0-0x05.4) is set.

Register Related to Reception

The registers related to reception are summarized in the following table.

Register	Address.Bit	Indication/Usage	Type	Default Value
Command	Sector0-0x01	Activate Receive or Transceive command	Dynamic	0x00
RxLastBit	Sector0-0x05.[2:0]	Displays the number of valid bits in the last received byte	Read Only	000
RxIEn	Sector0-0x06.3	Configure interrupt enable for RxIRq	Read/Write	0
RxIRq	Sector0-0x07.3	Indicate end of reception	Dynamic	0
CRCErr	Sector0-0x0A.3	Report CRC error in received frame	Read Only	0
FramingErr	Sector0-0x0A.2	Report Framing error in received frame	Read Only	0
ParityErr	Sector0-0x0A.1	Report Parity error in received frame	Read Only	0
CollErr	Sector0-0x0A.0	Report data collision in received frame	Read Only	0
CollPos	Sector0-0x0B	Report collision position in ISO14443A / ISO15693	Read Only	0
RxAlign	Sector0-0x0F.[6:4]	Define the position of the first received data bit to be stored in the first received byte in the bit oriented frame in ISO14443A	Dynamic	000
SubCPulses	Sector0-0x19.[7:5]	Define the number of subcarrier pulses per bit	Read/Write	011
SubCCarrier	Sector0-0x19.[4:3]	Define the number of carrier clocks used in subcarrier	Read/Write	01
LP_Off	Sector0-0x19.2	Switch off all Lowpass filters to extend incoming signal bandwidth	Read/Write	0
Gain	Sector0-0x19.[1:0]	Define Gain of Amplifier manually	Read/Write	11
RxMultiple	Sector0-0x1A.7	Set to execute consecutive reception	Read/Write	0
CollMaskVal	Sector0-0x1A.6	Setup value of collided bit	Read/Write	0
ZeroAfterColl	Sector0-0x1A.5	Setup value of data after collided bit to be zero	Read/Write	0
RxFraming	Sector0-0x1A.[4:3]	Define decoder framing	Read/Write	01
RxCoding	Sector0-0x1A.[1:0]	Define receiving pattern for decoder	Read/Write	00
BitPhase	Sector0-0x1B	Define the fractional guard time of decoder in unit of clock	Read/Write	0x3D
MinLevel	Sector0-0x1C.[7:5]	Define the minimum signal strength at the decoder input that shall be accepted	Read/Write	101
CollLevel	Sector0-0x1C.[3:1]	Define the relative minimum signal strength at the decoder input that has to be reached by the weaker half-bit of the Manchester and FSK-coded signal	Read/Write	101
NoRxSOF	Sector0-0x1D.7	Suppress error from SOF-missing frame	Read/Write	0
NoRxEGT	Sector0-0x1D.6	Suppress error from EGT not conforming to the standard	Read/Write	0
NoRxEOF	Sector0-0x1D.5	Suppress error from EOF-missing frame	Read/Write	0
HP2Off	Sector0-0x1D.4	Switch off the 2nd high pass filter	Read/Write	0
TauD	Sector0-0x1D.[3:2]	Defines time constant of internal PLL	Read/Write	01
AGCEn	Sector0-0x1D.1	Enable Automatic gain control	Read/Write	1
TauAGC	Sector0-0x1D.0	Define time constant of AGC	Read/Write	0
Cont_Int	Sector0-0x1E.7	Boost correlator gain by 4x in low data rate of ISO15693	Read/Write	0

Register	Address.Bit	Indication/Usage	Type	Default Value
ByPassEnv	Sector0-0x1E.2	Select type of analog input signal present at RX pin for extension in long range application	Read/Write	0
DecoderSrc	Sector0-0x1E.0	Select input signal for internal decoder	Read/Write	1
BPSKDecMeth	Sector0-0x1F.7	Define the BPSK Decoding Method	Read/Write	1
BPSKDataRec	Sector0-0x1F.6	Enable BPSK Data Recognition block	Read/Write	0
SOFSel15693	Sector0-0x1F.5	Define the method of ISO15693 header recognition	Read/Write	1
EMD_Suppress	Sector0-0x1F.1	Enable EMD frame suppression	Read/Write	0
SOF43A_5Bits	Sector0-0x1F.0	Define the ISO14443A SOF condition	Read/Write	0
RxWait	Sector0-0x21	Define guard time counting from TxEOF to start of receiving time of decoder in unit of one-bit duration	Read/Write	0x06
MSBFirst	Sector0-0x22.6	Define method in calculation CRC	Read/Write	0
CRC3309	Sector0-0x22.5	Define method in calculation CRC	Read/Write	0
CRC8	Sector0-0x22.4	Define method in calculation CRC	Read/Write	0
TxCRCEn	Sector0-0x22.2	Enable CRC in transmitted frame	Read/Write	0
ParityOdd	Sector0-0x22.1	Set odd parity in transmitted frame	Read/Write	1
ParityEn	Sector0-0x22.0	Enable parity in transmitted frame	Read/Write	1
CRCPresetLSB	Sector0-0x23	Define preset CRC value in LSB	Read/Write	0x63
CRCPresetMSB	Sector0-0x24	Define preset CRC value in MSB	Read/Write	0x63
RxCorrIntTime	Sector0-0x3C.[6:5]	Adjust integration time of half bit evaluation in correlator for ISO14443A – Manchester receiving	Read/Write	00
SOFSel43A	Sector0-0x3C.3	Define the method of ISO1444A – Manchester pattern header recognition	Read/Write	1
Gain_ST3	Sector0-0x3F.[5:3]	Define gain of the last state amplifier for systems requiring extensive gain	Read/Write	000
M_HP1	Sector1-0x2E.[7:6]	Define high-pass cut-off frequency for 1st stage high pass filter	Read/Write	00
M_LP1	Sector1-0x2E.[5:4]	Define low-pass cut-off frequency for 1st stage low pass filter	Read/Write	01
M_HP2	Sector1-0x2E.[3:2]	Define high-pass cut-off frequency for 2st stage high pass filter	Read/Write	10
M_LP2	Sector1-0x2E.[1:0]	Define low-pass cut-off frequency for 2st stage low pass filter	Read/Write	01
ManFilterSel	Sector1-0x2F.7	Define to configure frequency corner of filter manually	Read/Write	0

Register Related to Reception

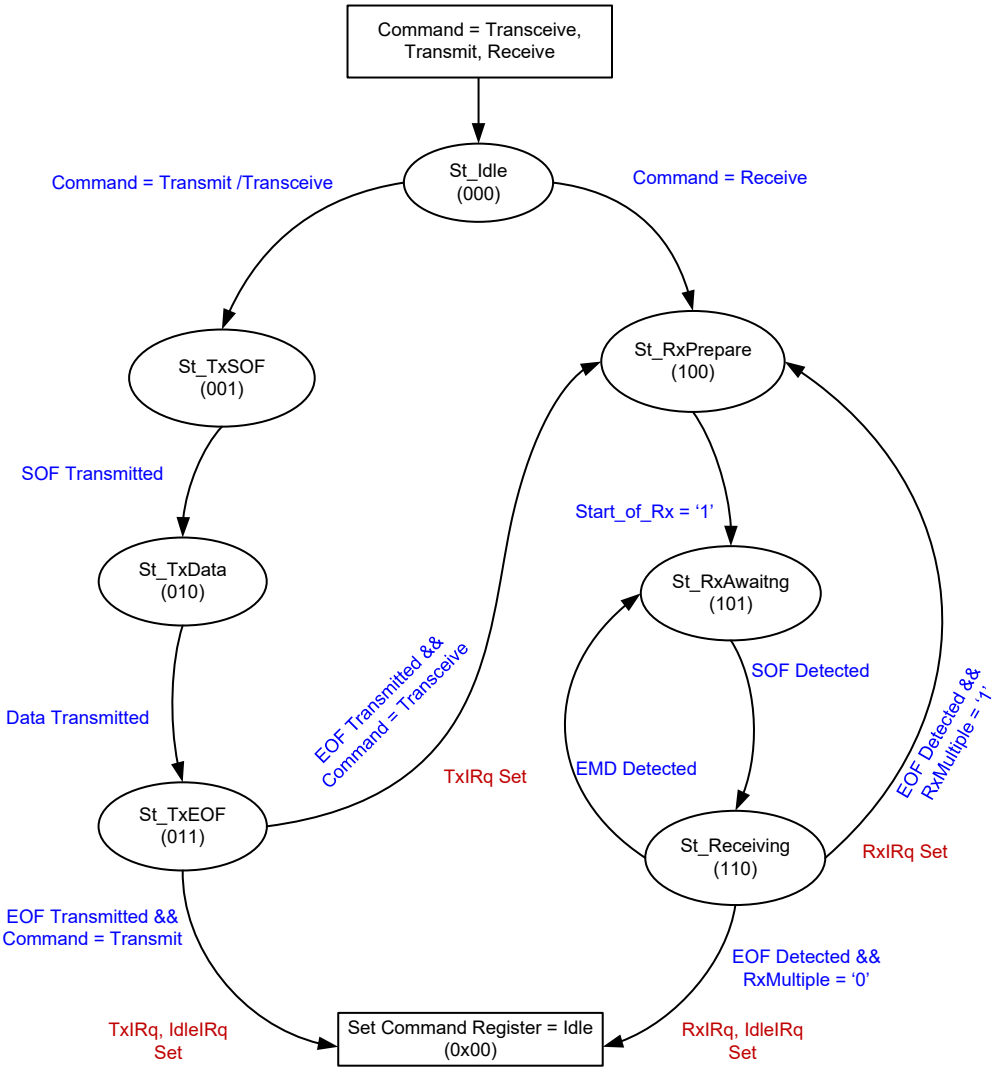
Transceive Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x1E	Transmit Data in the FIFO to card and enable receiving circuit after transmission is completed.	TX Data stream	RX Data stream	TxIRq, RxIRq, IdleIRq

The Transceive command starts the Transmit command first and then automatically executes the Receive command when the Transmit is finished. Therefore, the transmitted data must be written to FIFO during transmission process and the received data stream is returned into FIFO during reception. In transceiving data with more than 64 bytes, the FIFO handling routines through interrupt indication, such as HiAlert and LoALert similar to that of Transmit and Receive, must be employed.

State Machine

The state of CODEC can be monitored via the ModemState value in the PrimaryStatus register. The state transition diagram including the triggering events, related interrupt flags are shown in the following diagram.



State Diagram in Transceive, Transmit and Receive Command

CalCRC Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x12	Turn on CRC calculation process and data in FIFO buffer is calculated CRC	Data stream	—	IdleIRq

The CalCRC command activates the CRC calculation of the data stream in the FIFO. The preset value is defined in registers CRCPresetMSB and CRCPresetLSB, and the calculation algorithm is configured by the ChannelRedundancy register. After the calculation is completed, the calculation result is shown in registers CRCResultMSB and CRCResultLSB and the flag IdleIRq is set. This command is automatically terminated when the FIFO is empty. If the data stream is more than 64 bytes, the microcontroller should continuously feed the data to the FIFO as in Transcieve command.

CRC 16-Bit

When bit CRC8 (Sector0-0x22.4) is cleared to 0, CRC coprocessor performs 16-bit CRC calculation. The polynomial for 16-bit CRC calculation is $X^{16}+X^{12}+X^{5}+1$. For ISO14443A, bit CRC3309 (Sector0-0x22.5) must be cleared to 0. For ISO14443B and ISO15693, bit CRC3309 (Sector0-0x22.5) must be set to 1. If bit CRC3309 is set, final CRC value is Xored with 0xFFFF based on ISO/IEC3309.

CRC 8-Bit

When bit CRC8 (Sector0-0x22.4) is set to 1, CRC coprocessor performs 8-bit CRC calculation. The polynomial for 8-bit CRC calculation is $X^8+X^4+X^3+X^2+1$. Preset value for 8-bit CRC calculation is defined in CRCPresetMSB (Sector0-0x23). The output from CRC calculation is displayed in CRCResultMSB.

LoadKeyFIFO Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x19	Read data in FIFO and put into a key buffer	Byte0 (LSB) + Byte1+… +Byte10+Byte11	—	TxIRq, IdleIRq

The LoadKeyFIFO command reads 12-bytes data in the FIFO. The data must be in key storage format. If the data format is correct, the key is loaded into the internal key buffer and the bit KeyErr in the Error register is cleared, otherwise it will be set. When this command is finished, bits TxIRq and IdleIRq are set. The FIFO cannot be accessed from the external microcontroller when this command is executed.

Key Format

Before execution of the LoadKeyFIFO command, a specific key format must be written into the FIFO respectively. Each byte of the 6-byte Crypto_M key must be splitted into 4 MSB, high nibble, and 4 LSB, low nibble. Each nibble is written in one byte, containing its inverted bit version in high nibble and itself in low nibble. An example of the key format is shown in the following table.

Key (Hex)	Data Written to the FIFO (Hex)
F0 F1 F2 F3 F4 F5	0F F0 0F E1 0F D2 0F C3 0F B4 0F A5
A2 B8 73 93 64 CF	5A D2 4B 78 87 C3 69 C3 96 B4 3C 0F

Example of Key Format

Authent Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x1C	Execute the authentication between reader and card	Card's Authent command + Card's Block address + Card's UID(LSB) + … + Card's UID(MSB)	—	IdleIRq TxIRq RxIRq

The Authent command executes the authentication routine to card(s) containing Crypto_M engine. It is a combination of 2 consecutive transactions between reader and card. This command requires 6 bytes of data in arguments consisting of card authentication command, the address of blocks to be authenticated and the card UID repectively. Before executing this command, the associated key must be loaded into the key buffer. In the first part of the authentication process, 6-byte data in the FIFO is transmitted to the card. The card response is verified. Then, the second transaction is performed. The verification output from the first response is retransmitted to the card. The second card response is verified again. If all verifications are completed, the bit Crypto_MOn in the Control register will be set to indicate the completion of the authentication, and all communications onwards will be encrypted. This bit cannot be set directly by the external microcontroller, except the execution from the Authent command. Moreover, interrupt flag IdleIRq, TxIRq and RxIRq are set in case of authentication successful after Authent command is finished. If the authentication is unsuccessful, some interrupt flags are set depending on RF event as shown in the following table.

RF Event	Interrupt Flag	Crypto_MOn
No card response*	TimerIRq	0
No card response in second transaction*	TimerIRq, TxIRq	0
Wrong response in second transaction	TxIRq, IdleIRq, RxIRq	0
Complete authentication	TxIRq, IdleIRq, RxIRq	1

*: In this case, the value in Command register is still in Authent command state.

Interrupt Flag Result from Authent Command

RxFilterTune Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x10	Activate the filter-frequency-corner-tuning process in receiver amplifier	—	—	IdleIRq

The RxFilterTune command activates the filter-frequency-corner-tuning process in the receiver amplifier. This command is for adjusting the filter frequency corner due to variations in temperature and manufacturing process. After operating the command, all frequency corners are set back to the proper values and the frequency deviation is eliminated. The tuning process takes 302μs. However, this command is automatically performed every time the system is powered up. Therefore, it is not required to tune the filter by users frequently.

LFOTune Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x20	Activate the low frequency tuning process to generate clock 16.38kHz	—	—	IdleIrq

The LFOTune command activates the low frequency oscillator tuning process. This command is for adjusting the low frequency clock frequency due to variations in temperature and manufacturing process. After operating the command, output frequency is set back to suitable value, 16.38kHz. However, this command is automatically performed every time the system is powered up. Therefore, it is not required to tune the LFO by users frequently.

ADCCalibrate Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x21	Calibrate ADC to record the ADC offset value	—	—	IdleIrq

The ADCCalibrate command enables ADC calibration process. This command will start ADC conversion without input signal by disabling transmitter. The ADC result output, ADC_Result_Offset, both I and Q channel are kept into internal buffer. These offset values will be later used for compensating ADC_Result value both in Card Detection and Field Detection operation.

Note that this command should be re-executed when ADC configuration parameters in the “Registers Associated with Field Detection and Card Detection” table presented in the “RF Amplitude Detector System” section are changed. Furthermore, users should be ensured that there is no external RF source device near by the reader.

CardDetect Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x22	Activate ADC to measure RF amplitude at pin RX by enabling the device’s transmitter	—	—	IdleIRq, CDIRq

The CardDetect command starts the Card Detection operation as described in the “RF Amplitude Detector System” section. The device senses RF amplitude, driving from its transmitter, at pin RX, and uses ADC to convert into digital ADC Result. After operation is completed, IdleIRq flag is set. If the ADC_Result is more than CDThreshold_H, or lower than CDThreshold_L, CDIRq flag will also be set at the same time. To ensure suitable operation of card detection, users should firstly find the ADC baseline level, ADC_Result run on free air.

FieldDetect Command

Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x23	Activate ADC to measure external RF amplitude at pin RX from other RF source by disabling the device’s transmitter	—	—	IdleIRq, RxIRq

The FieldDetect command starts the Field Detection operation as described in the "RF Amplitude Detector System" section. The device measures RF amplitude induced from other external device at pin RX, and uses ADC to transform into digital result. In this mode, the device's transmitter is automatically turned off. After operation finish, IdleIRq flag is set. If the ADC_Result is more than FDThreshold_H, RxIRq flag will also be set at the same time.

ReadSignature Command

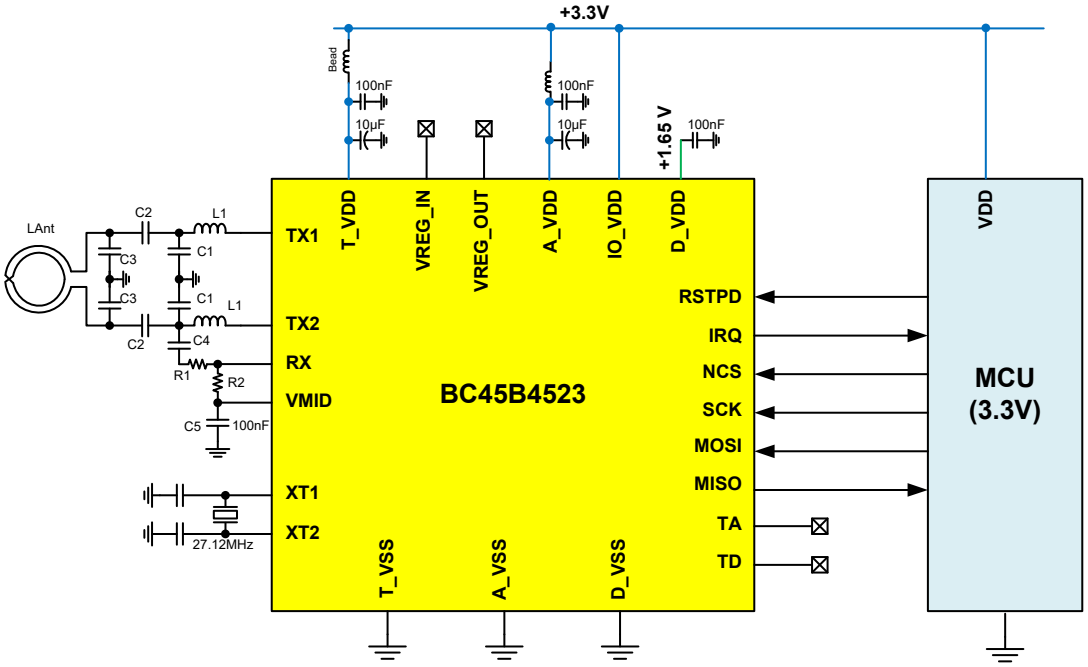
Command Code	Action	Input Data Required in FIFO	Return Data Read from FIFO	Interrupt Flag
0x31	Read device's mask set, parameter and revision then return into FIFO	—	MaskSet + ProductionParam + Revision	IdleIRq

The ReadSignature command returns the BC45B4523's device parameter and production into FIFO. Note that, MaskSet, ProductionParam and Revision can be directly read via SPI from registers at Sector1-0x0D, Sector1-0x0E and Sector1-0x0F consecutively.

Typical Operating Circuit and Design Considerations

Circuit Configuration

Typical circuit configuration of the device for closed coupling is shown in the following figure. The transmitter is set to drive a differential antenna from pin TX1 and TX2, and the internal envelope detector is employed. L1, C1, C2 and C3 form a transmitter antenna matching network, while LAnt is a loop antenna, which can be realized by a PCB trace. The signal tapping point for the receiver is directly from the loop antenna via C4. R1 and R2 are used as a carrier-divider to feed the receiver input signal to the pin RX. Signal swing must be divided properly and accommodated within an operating range of the internal envelope detector. C5 is a decoupling capacitor for mid rail reference voltage. Defined from the baseband line coding, the bandwidth of the antenna network should be wide enough to cover the bandwidth of both transmission and reception to prevent inter-symbol interference. For examples, ISO14443A and ISO14443B require the bandwidth around 1MHz, while ISO15693 requires only 500kHz. Reciprocally, rising and falling time of the modulation in the transmission must be within a limit of an operating standard. Examples of component values to cover the bandwidth of all standards are shown in the following table as a guideline. However, the antenna network fine trimming is required to meet specifications for each operating standard especially for rising time, falling time and overshoot of transient response of carrier.

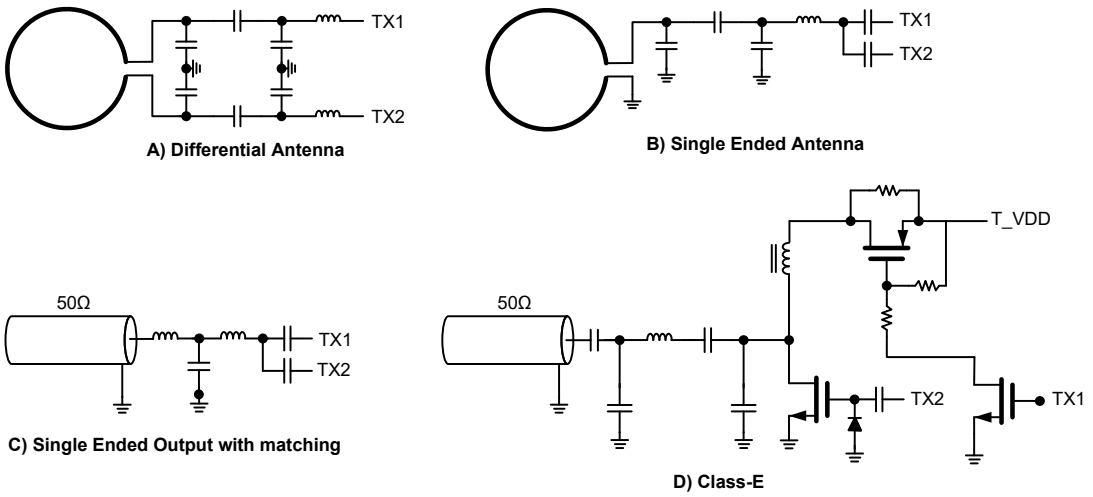


Typical Circuit Configuration of BC45B4523 for Closed Coupling

Component	Example 1	Example 2
LAnt	0.4μH (Q=50)	0.4μH (Q=50)
L1	0.47μH	0.33μH
C1	260pF	370pF
C2	33pF	47pF
C3	650pF	645pF
C4	15pF	15pF
R1	1kΩ	1kΩ
R2	180Ω	180Ω

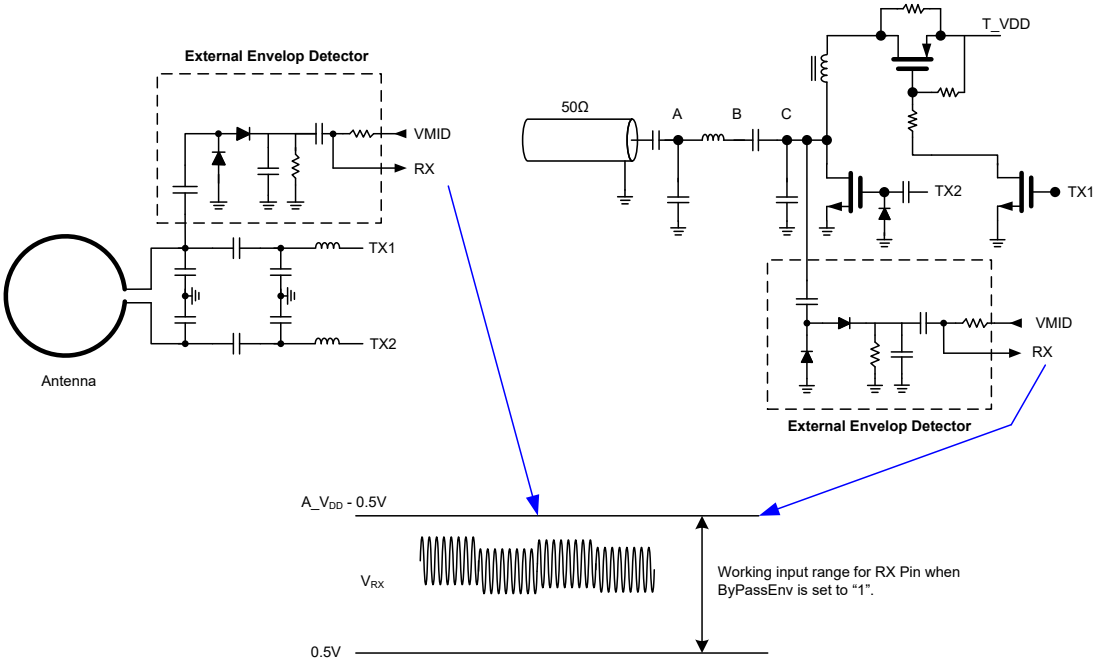
Example of Component Values to Cover Bandwidth

Moreover, the device is capable of connecting to various RF topologies. The transmitter driver can be designed to connect to not only a differential-drive antenna but also a single-ended-drive antenna and a Class-E amplifier. The following figure illustrates possible driver connections. The differential and single-ended types are suitable for driving an on-board antenna for closed coupling applications. The single-ended with 50Ω output matching and a Class-E amplifier are used for connection to a remote antenna through 50Ω cable. In addition, the Class-E amplifier can provide high power required by mid/long range reader. The device transmitter supports in-phase driving for a single-ended or plain carrier and a base band in Class-E topology.



Various Transmitter Configurations that BC45B4523 Supports

The device is capable to receive demodulated baseband from an external envelope detector. Employing the external envelope detector can yield better sensitivity than performing through the internal one because large amount of carrier is removed, while the baseband signal is not significantly attenuated comparing to the carrier dividing scheme. Note that the ByPassENV bit must be set if the external envelope detector is used. A simple external envelope detector connection is shown in the following figure. For an on-board antenna reader, the signal tapping point for the receiver is typically at the antenna where the largest modulation from card presents. For 50Ω cable driving type in which the antenna is located remotely, the tapping point can be selected from one of the local points (i.e., A, B or C) where the largest modulation exhibits.



External Envelope Detector Connection

Power Supply & Grounding

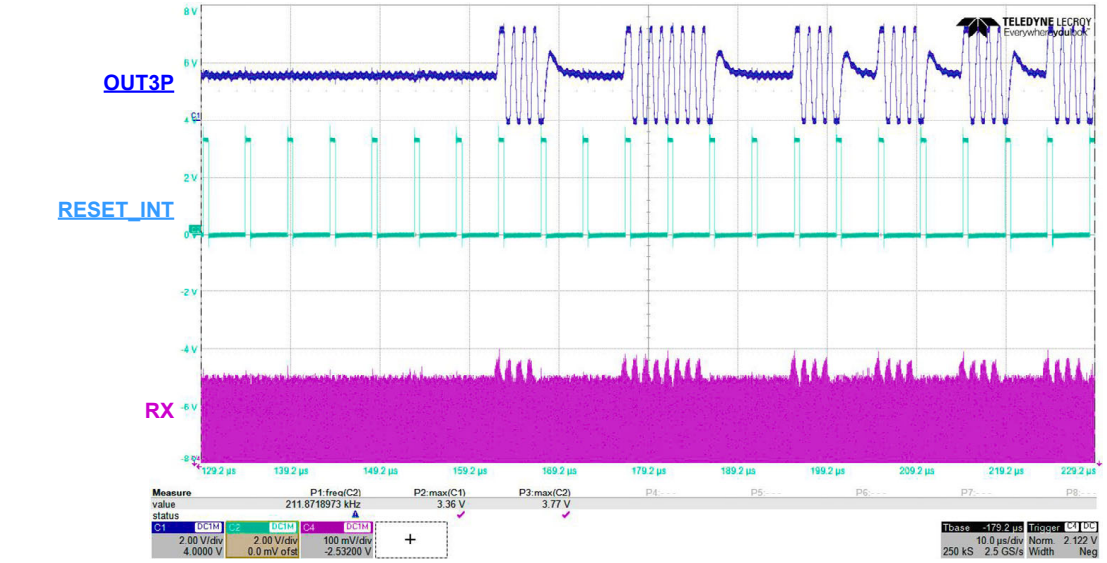
In NFC systems, the receiver extracts the card-response signal from the envelope of the RF carrier on the antenna. Except for some smartcards where their operating range is deliberately limited by their designs, the noise in transmitter, which inevitably reflects back to receiver system, is a limiting factor for the reading performance, especially in ISO15693. The noise in the transmitter is mainly stemmed from the transmitter power supply ripple and clock jitter. The clock jitter is from the analog power supply noise, in which the oscillator relies on, and the cleanliness of the clock source.

To achieve the highest reading performance, the noise in both transmitter and receiver parts should be as low as possible. The noise in the receiver is fundamentally limited to electronic noise as stated in the "Reveiver Characteristics". Therefore, common techniques, such as power supply separation, decoupling capacitor and grounding, should be employed. The device provides three power-supply sets for a transmitter, an analog part and a digital input/output part. Positive power supply of each part can be simply separated by ferrite beads. A more effective measure is to use dedicated regulators to block the noise feeding through other parts. Local decoupling capacitors, 10μF tantalum and 0.1μF ceramic, must be provided to supply high-frequency current and placed close to each power supply input. In floor-planning, external high-current sections, unrelated to RF transmission and noise-generating components, must be grouped and placed far away from sensitive analog parts such as oscillator, external envelope detector and RF transmitter. For example, the high current component can be a switching power supply, while the noise generating component can be a microcontroller or host interface components. For NFC reader applications, the analog ground A_VSS and the transmitter ground T_VSS must be on the same ground to keep the same potential for both the receiver and the transmitter. Physically, the analog and transmitter ground can be connected by a unified solid ground plane. As typical technique used in mixed-signal system, the analog part and the digital part, digital section of the device and the external microcontroller, can be on the same ground plane. However, the power source direction and the ground return path from such noisy components should be carefully designed to avoid current superimposition causing a bouncing between the analog and the transmitter ground. A switching power supply and a heavy driver for the interface must be placed on the isolated ground plane with the isolated return path. In case of the switching power supply, the operating frequency must carefully be designed so that it is not overlap the operating bandwidth. Magnetic shield inductor and component selection can be employed to reduce such effect.

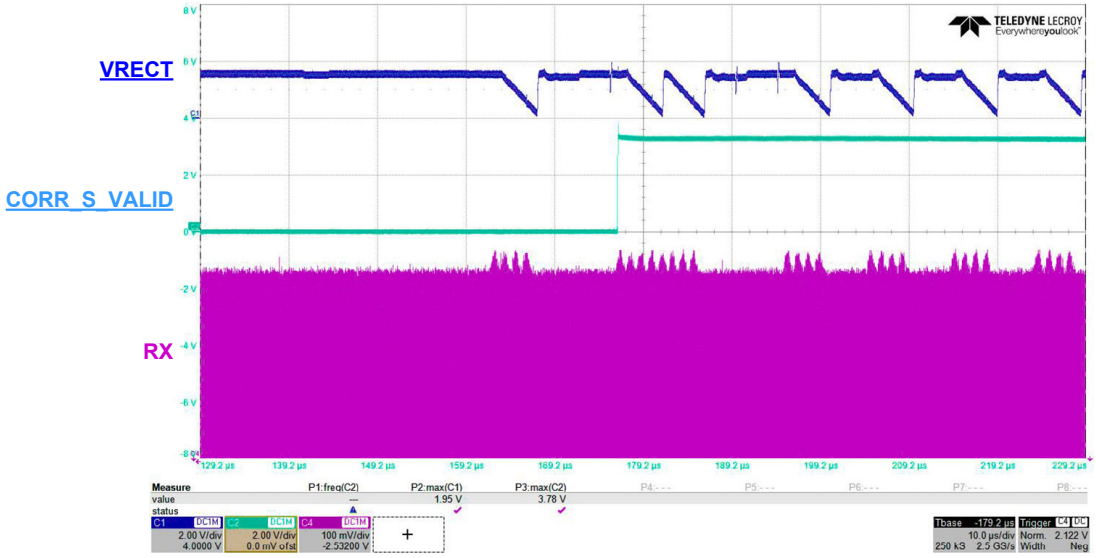
Test Signals

The device internal signal can be probed out via TA and TD pins for multiples purpose. These pins are applied for monitoring and debugging signal for both Manchester and BPSK pattern. Furthermore, they can be fed to external MCU to decode other protocols which the device does not support.

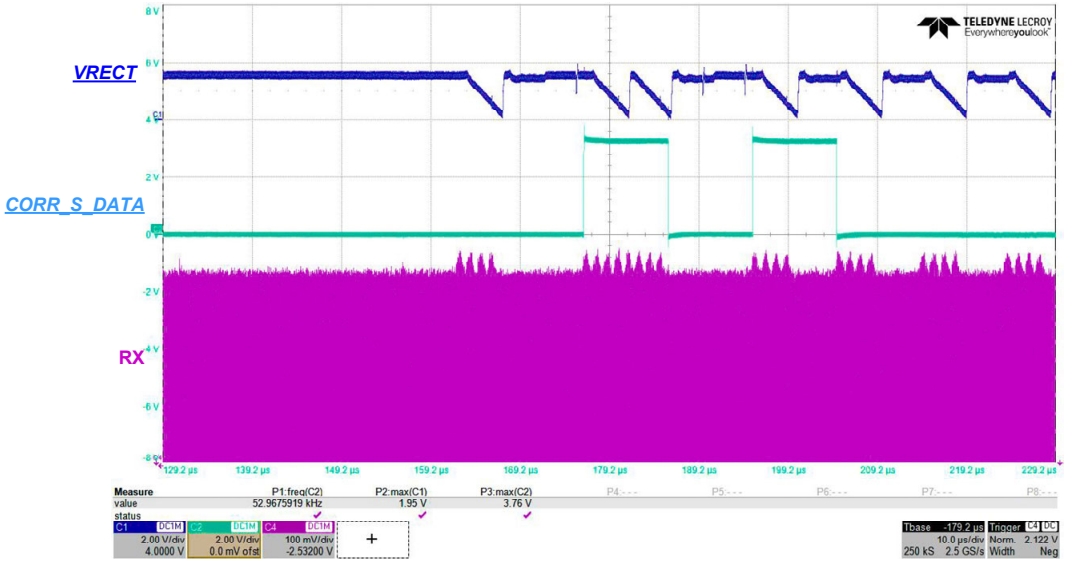
For Manchester-and-FSK decoder in ISO14443A and ISO15693, the purpose of test signal is for monitoring and fine-tuning the time wait, Twait, between EOF of the transmitted data and SOF of the received data. The Twait, defined by BitPhase and RxWait registers, must be synchronously set to make the decoder evaluate correctly. The following "OUT3P and RESET_INT" figure shows internal signals during Manchester-coding reception in ISO14443A, RESET_INT used in resetting evaluation results of each half bit and input analog signal, and OUT3P is for the Manchester-and-FSK decoder. Also, the OUT3P is the amplifed envelope from the last state amplifier. Active state of RESET_INT, indicating point in resetting for each half bit, must be set to coincide with the beginning point the Manchester-and-FSK-decoder input signal burst, OUT3P. By adjusting registers BitPhase and RxWait, the proper alignment of OUT3P and RESET_INT as shown in the figure can be achieved. Note that the period of RESET_INT is equal to half ETU of the operating standard. This results in a complete integration of each half bit, VRECT, as shown in the other three figures below, which display the evaluation result CORR_S_VALID, CORR_S_DATA and CORR_S_COLL respectively. CORR_S_VALID shows the validity of data evaluation, CORR_S_DATA displays the evaluation result while CORR_S_COLL expresses the collision result of data stream.



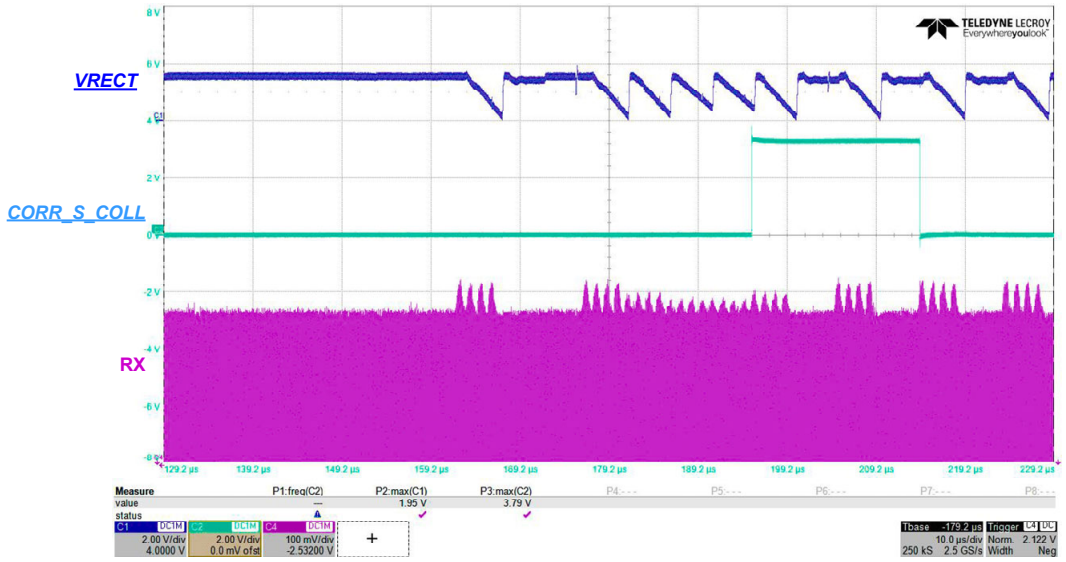
OUT3P and RESET_INT (Test Register is Set to 0x10)



VRECT and CORR_S_VALID (Test Register is Set to 0x1E)

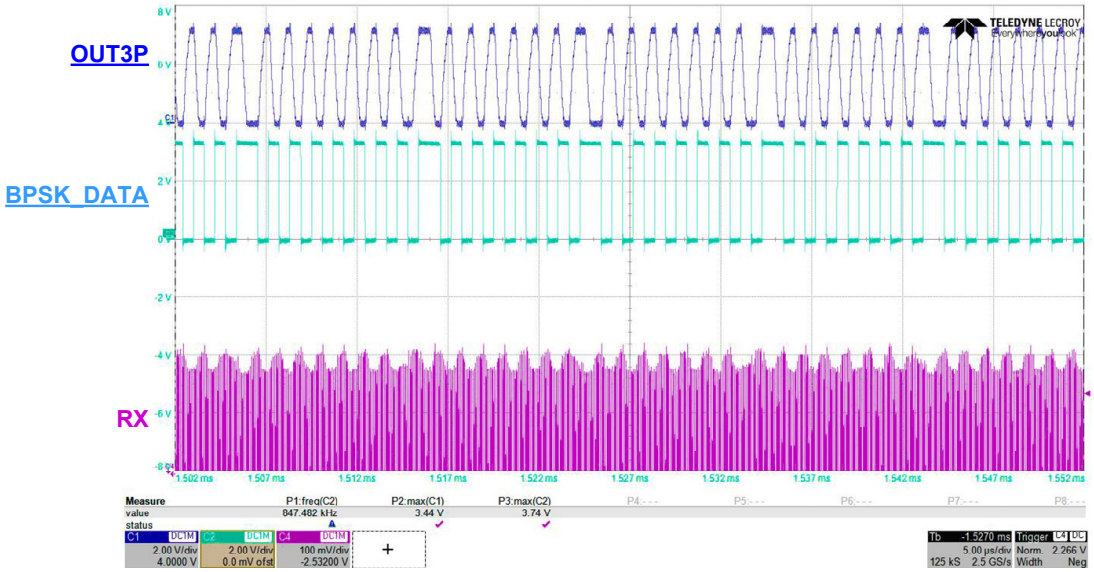


VRECT and CORR_S_DATA (Test Register is Set to 0x0E)

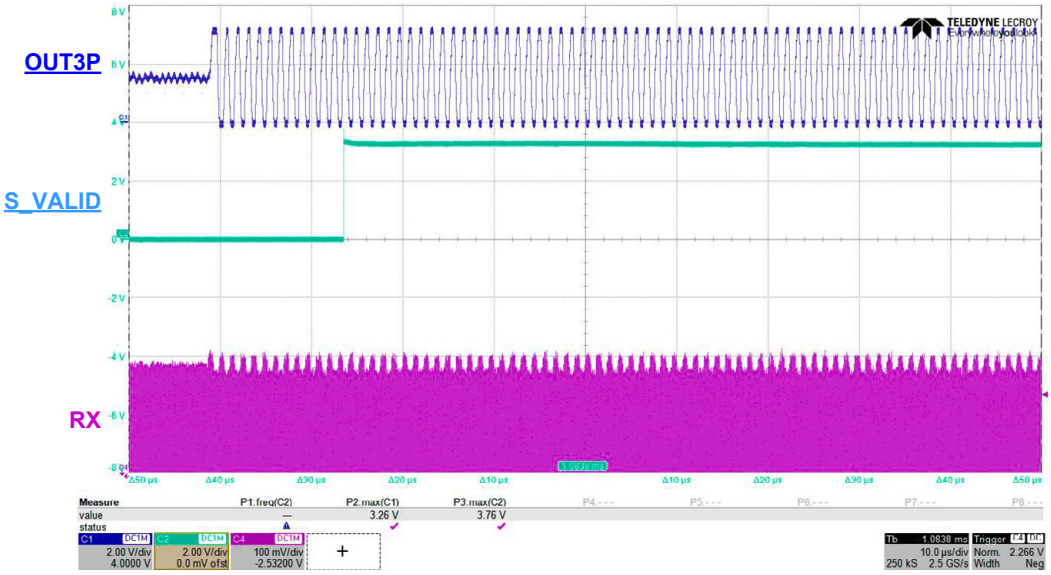


VRECT and CORR_S_COLL (Test Register is Set to 0x1F)

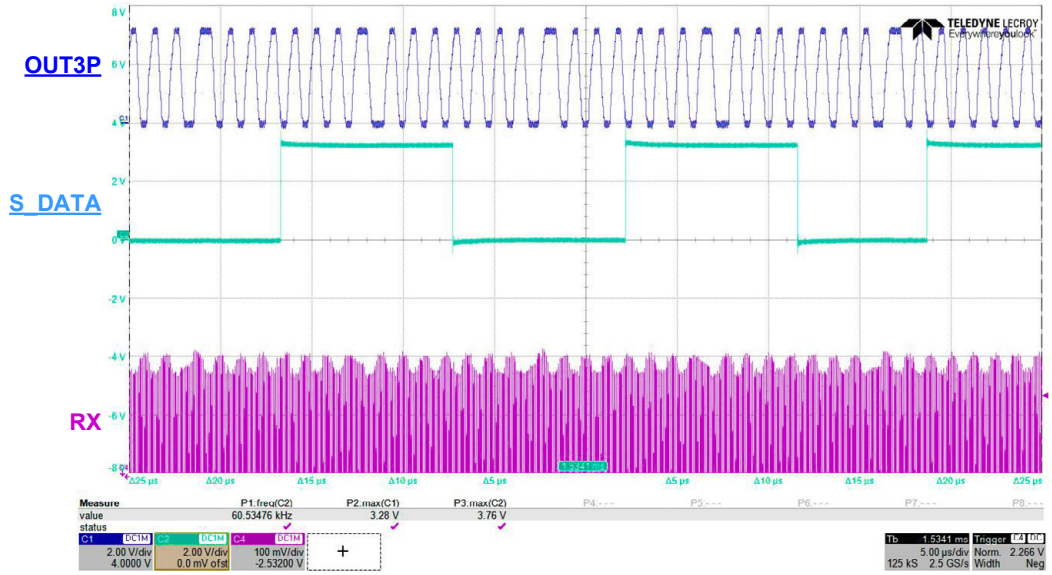
For BPSK decoder in ISO14443A at higher rate and ISO14443B, the Twait must be set to assert before SOF of the card response. Also, some test signals can be used to see phase distortion from the antenna and its effect. The following “OUT3P and BPSK_DATA” figure shows the amplified envelope signal OUT3P and recovery data from the slicer BPSK_DATA. While the other two figures below show valid evaluation results S_VALID and evaluated data S_DATA and the amplified envelope OUT3P.



OUT3P and BPSK_DATA (Test Register is Set to 0x11)

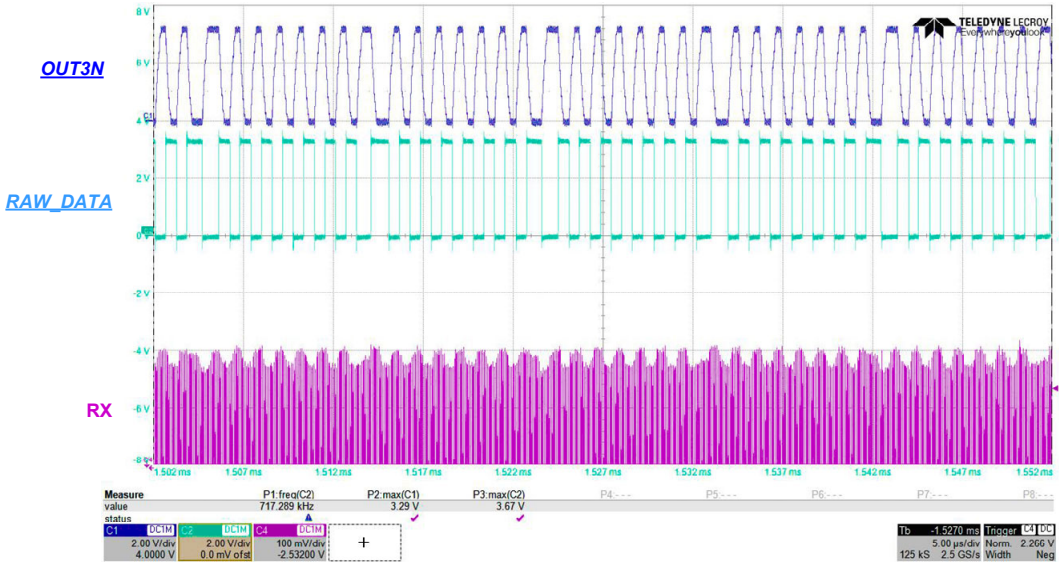


OUT3P and S_VALID (Test Register is Set to 0x12)

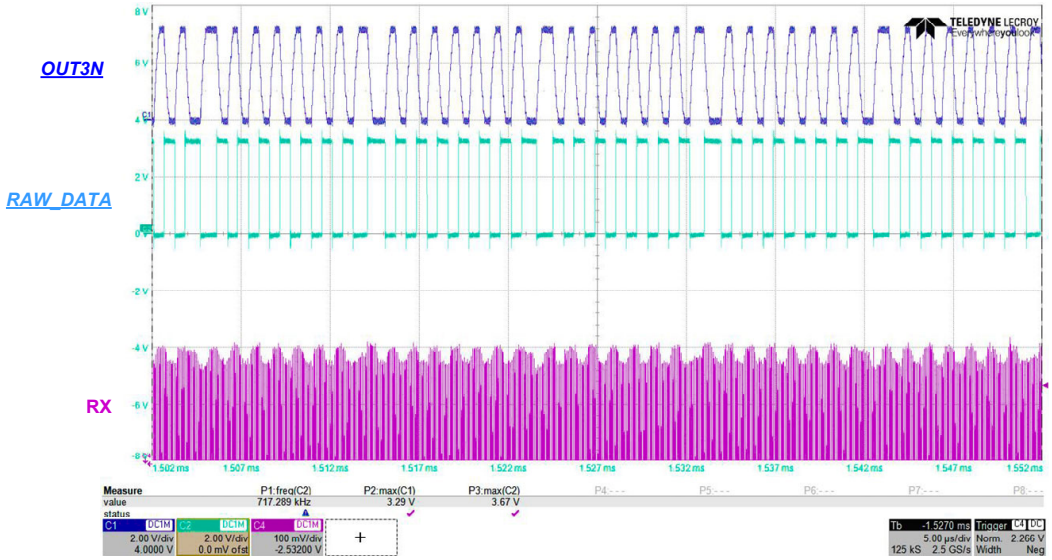


OUT3P and S_DATA (Test Register is Set to 0x13)

Furthermore, when the proprietary protocol is implemented, external MCU need to decode baseband itself by probing out RAW_DATA as shown in the following figures.



OUT3N and RAW_DATA (Test Register is Set to 0x19) for Manchester Pattern



OUT3N and RAW_DATA (Test Register is Set to 0x19) for BPSK Pattern

The following table summarizes key test codes for configuring the Test[6:0] bit field (Sector0-0x3A.[6:0]) to route internal key signals to monitor for adjustment of the above parameters. While the meanings of such signals are explained in the accompanying "Meaning of Key Test Signal" table.

Test[6:0] (Hex)	TDSelect Bit (Sector0-0x39.3)	Pins			
		TD	Related Block	TA	Related Block
0x0E	0	CORR_S_DATA	Manch/FSK decoder	VRECT	Manch/FSK decoder
0x10	0	RESET_INT	Manch/FSK decoder	OUT3P	RX Amplifier
0x11	0	BPSK_DATA	BPSK Decoder	OUT3P	RX Amplifier
0x12	0	S_VALID	BPSK Decoder	OUT3P	RX Amplifier
0x13	0	S_DATA	Manch/FSK/BPSK decoder	OUT3P	RX Amplifier
0x19	1	RAW_DATA	RX Amplifier	OUT3N	RX Amplifier
0x1C	1	MANCH_WO_SUB	Manch/FSK decoder	VRECT	Manch/FSK decoder
0x1E	0	CORR_S_VALID	Manch/FSK decoder	VRECT	Manch/FSK decoder
0x1F	0	CORR_S_COLL	Manch/FSK decoder	VRECT	Manch/FSK decoder
0x4D	0	TX_EN	Transmitter	VRECT	Manch/FSK decoder

Key Test Signal and Indication

Signal	Description
OUT3P	A positive phase amplified output from the 3rd state amplifier
OUT3N	A negative phase amplified output from the 3rd state amplifier
VRECT	An integrated output from Manchester decoder The last value of VRECT is used to evaluate the output bits together with Minlevel and CollLevel
RESET_INT	Signal indicating new slots used in Manchester decoder
CORR_S_VALID	Validity of output data from Manchester decoder
CORR_S_COLL	Collision of output data from Manchester decoder
CORR_S_DATA	Evaluate output data from Manchester decoder
BPSK_DATA	BPSK pattern recovery signal from DPLL
S_DATA	Evaluate output data from Machester / BPSK decoder, feeding to frame decoder
S_VALID	Validity of output data from Manchester / BPSK decoder, feeding to frame decoder
RAW_DATA	RX Amplifier - comparator output, converting analog signal into digital signal

Signal	Description
MANCH_WO_SUB	Process Manchester without subcarrier signal
TX_EN	Signal indicating transmitter is enabled following register configuration

Meaning of Key Test Signal

Thermal Considerations

Silicon temperature during operation should not exceed the maximum limit at 125°C for best performance and long term reliability. The operating temperature of the silicon (T_J) can be calculated from total power consumption (P_{lossT}), thermal impedance (θ_{JA}) and ambient temperature (T_A) according to the following equation below.

$$T_J - T_A = \theta_{JA} \times P_{lossT}$$

Depending on power loss, the heat sink structure and heat dissipation path must be sufficiently provided to maintain the silicon temperature within the maximum operating range.

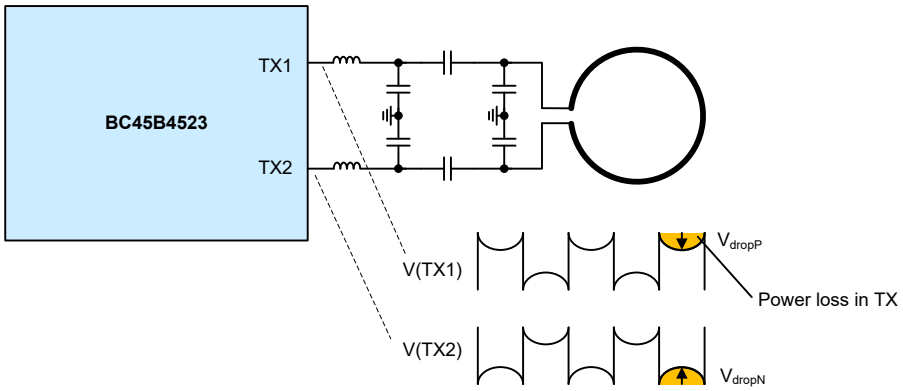
The transmitter and regulator are the main heat source of the device. Then, the total power consumption is approximately the sum of power loss from both parts.

$$P_{lossT} = P_{lossTX} + P_{Reg}$$

For the first part P_{lossTX}, assuming worst case scenario, the transmitter drives the effective resistive load at the operating frequency. Thus, the sourcing and sinking current can be approximated to be half-sinusoidal shape as illustrated in the following figure. Therefore, the power loss from voltage drop across the driver is

$$P_{lossTX} = (I_{out})^2 \times R_{out}$$

Where the I_{out} is a peak output current from the driver and the R_{out} is an effective resistance of the driver output.



Assume load is resistive at carrier frequency

$$P_{lossTX} = (1/2)\frac{V_{dropP}^2}{R_{outP}} + (1/2)\frac{V_{dropN}^2}{R_{outN}} = \frac{V_{drop}^2}{R_{out}} = I_{out}^2 R_{out}$$

Assume load is resistive at carrier frequency: $V_{dropP} \cong V_{dropN}$, $R_{outP} \cong R_{outN}$

Power Loss from the Transmitter

Similarly, the above loss calculation can also be used in the single-ended configuration. For other configurations, the power loss in the transmitter must be calculated case-by-case depending on structure of the external circuit. For example, if an external amplifier is a Class-E as shown in the above figure, the power loss in the device transmitter can be calculated from the switching loss, i.e.,

$$P_{lossTX} = (V_{TX})^2 \times f \times C_{in}$$

Where the V_{TX} is an operating transmitter supply voltage, the f is an operating frequency which is 13.56MHz and the C_{in} is an input capacitance of MOSFET.

For the second part of the power loss P_{Reg}, the loss in the regulator can be calculated from the dropout voltage multiplying by the passing current.

$$P_{Reg}=I_{Out,Dig} \times (V_{InReg} - V_{OutReg}) + I_{Out,Ana} \times (V_{InReg} - V_{OutReg})$$

For example, the transmitter is designed to drive a differential antenna from a 5V power supply and deliver 250mA peak output current. Regulator supplies 150mA output current by relying on 5V input.

From the "Transmitter Characteristics", the effective resistance of the driver output is approximately at 5Ω, the transmitter loss is

$$PlossTX=(0.25)2 \times 5=0.312W$$

For the regulator, the loss is

$$PReg=(150mA \times (5V - 3.3V))=0.255W$$

The temperature coefficient θ_{JA} of an operating PCB is 34°C/W. (As shown in the "Absolute Maximum Rating")

The different temperature between the silicon and ambient $T_J - T_A$ is

$$T_J - T_A=(34°C/W) \times (0.314 + 0.255)\ W=19.3°C$$

T_J is set to 85°C. Then, the maximum T_A is approximately 65°C.

Practically, the designed PCB may be smaller from that stated in the JEDEC51-7 standard, so the temperature coefficient can be higher than the specification in the "Absolute Maximum Rating" (34°C/W). Designers must provide a proper heat sink with some margins to accommodate elevated temperature coefficient.

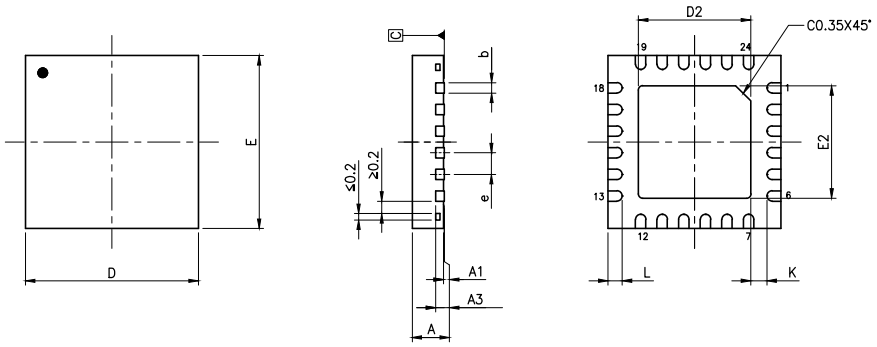
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the package information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

SAW Type 24-pin QFN (4mm×4mm×0.85mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.031	0.033	0.035
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.007	0.010	0.012
D	—	0.157 BSC	—
E	—	0.157 BSC	—
e	—	0.020 BSC	—
D2	0.104	0.106	0.108
E2	0.104	0.106	0.108
L	0.014	0.016	0.018

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	—	0.203 BSC	—
b	0.18	0.25	0.30
D	—	4.00 BSC	—
E	—	4.00 BSC	—
e	—	0.50 BSC	—
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
L	0.35	0.40	0.45