Features

- Frequency band: 2402MHz~2480MHz
- Complete 2.4GHz GFSK (BT=0.5) modulation transmitter
- Operating voltage range: V_{DD}=2.0V~3.6V
- Low Voltage Detection
- Programmable data rate: 125/250/500Kbps
- Programmable TX output power: up to 5dBm (Max. +8dBm)
- FUSE Data Memory: 320 bits
- Low current consumption
  - Deep sleep mode current: 0.5μA
  - I(LIRC_ON) current: 2.5μA
  - TX current consumption: Typ. 15.5mA @ 0dBm TX power
- On-chip VCO and Fractional-N synthesizer with integrated loop filter
- Support 32MHz crystal (±20ppm)
- Interface
  - Key mode (BC5161) – 2 key inputs for 8-pin SOP-EP, 8 key inputs for 16-pin QFN
  - I^2C mode (BC5162)
- FCC/ETSI Compliant
- Package types: 8-pin SOP-EP, 16-pin QFN

Development Tools

For rapid product development and to simplify device parameter setting, Holtek has provided relevant development tools which users can download from the following link:

https://www.holtek.com/rf-chip-parameters-setting-tool (BC5161 only)

General Description

The BC516x devices are high performance and low cost GFSK transmitters for wireless applications in the 2402MHz~2480MHz frequency bands. They incorporate a highly integrated 2.4GHz transmitter, a baseband modulator and an Encoder with programmable data rates from 125Kbps to 500Kbps. The frequency hopping function, which is informal and transmits the same data to each selected channel, can overcome the crowded frequencies.

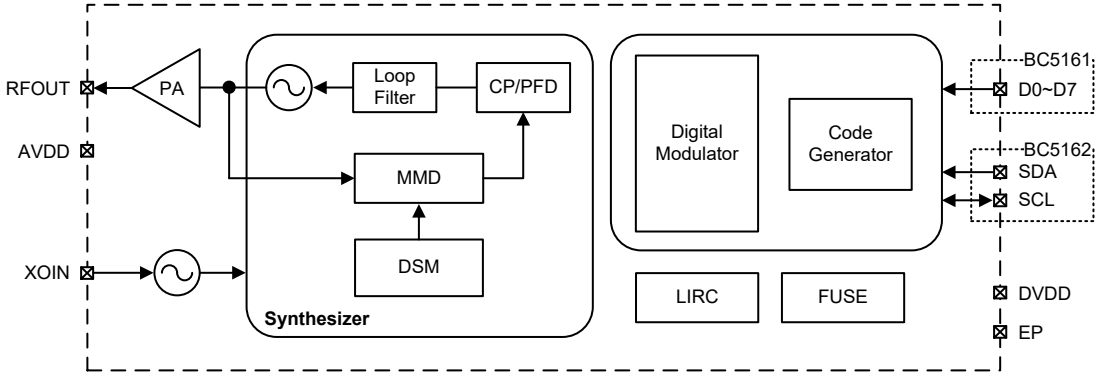
External host MCU can access the BC5162 through an I^2C interface. However, the BC5161 has Key/WOT modes, so it can be used for unidirectional wireless applications such as Student ID CARD, motorcycle/scooter keyless, etc. without MCU control.

Selection Table

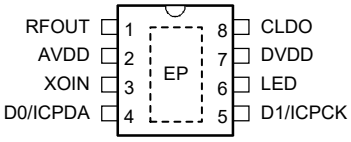
Part No.	V_{DD}	Frequency	Modulation	Data Rate
BC5161	2.0V~3.6V	2402MHz~2480MHz	GFSK	125/250/500Kbps
BC5162				

Part No.	Output Power	Cystal	Key Mode	Interface	Package
BC5161	-10dBm~+8dBm	32MHz	√	—	8SOP-EP, 16QFN
BC5162			—	I^2C	8SOP-EP

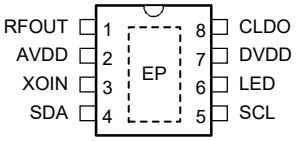
Block Diagram



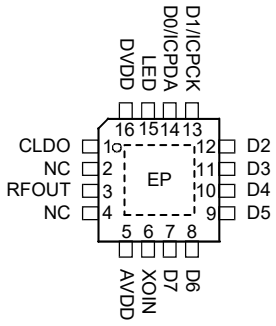
Pin Assignment



BC5161
8 SOP-EP-A



BC5162
8 SOP-EP-A



BC5161
16 QFN-A

Pin Description

BC5161

Pin No.		Pin Name	Type	Pin Description
8SOP-EP	16QFN			
1	3	RFOUT	AO	RF output signal from PA, connected to a matching circuit
2	5	AVDD	PWR	Analog power supply
3	6	XOIN	AI	Crystal input
4	14	D0/ICPDA	DI	Data input
			DI/DO	ICP data pin
5	13	D1/ICPCK	DI	Data input
			DI/DO	ICP clock pin
6	15	LED	DO	LED indicator
7	16	DVDD	PWR	Digital power supply
8	1	CLDO	PWR	LDO output, connected to a bypass capacitor
—	7~12	D7~D2	DI	Data input
—	2, 4	NC	—	No connection
—	—	EP	PWR	Exposed pad, must be connected to ground

Legend: DI: Digital Input; DI/DO: Digital Input/Output; AI: Analog Input; AO: Analog Output; PWR: Power

BC5162

Pin No.	Pin Name	Type	Pin Description
1	RFOUT	AO	RF output signal from PA, connected to a matching circuit
2	AVDD	PWR	Analog power supply
3	XOIN	AI	Crystal input
4	SDA	DI/DO	I^2C data pin
5	SCL	DI	I^2C clock pin
6	LED	DO	LED indicator
7	DVDD	PWR	Digital power supply
8	CLDO	PWR	LDO output, connected to a bypass capacitor
—	EP	PWR	Exposed pad, must be connected to ground

Legend: DI: Digital Input; DI/DO: Digital Input/Output; AI: Analog Input; AO: Analog Output; PWR: Power

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to V_{SS}+3.6V

Voltage on I/O Ports ..... V_{SS}-0.3V to V_{DD}+0.3V

Storage Temperature ..... -50°C to 125°C

Operating Temperature ..... -40°C to 85°C

ESD HBM ..... ±2kV

* These devices are ESD sensitive. HBM (Human Body Mode) is based on MIL-STD-883.

Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to these devices. Functional operation of these devices at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C, V_{DD}=3.3V, f_{XTAL}=32MHz, GFSK modulation with matching circuit, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{OP}	Operating Temperature	—	-40	—	85	°C
V_{DD}	Supply Voltage	—	2.0	3.3	3.6	V
Digital I/Os						
V_{IH}	High Level Input Voltage	—	0.7×V_{DD}	—	V_{DD}	V
V_{IL}	Low Level Input Voltage	—	0	—	0.3×V_{DD}	V
V_{OH}	High Level Output Voltage	I_{OH}=-5mA	0.8×V_{DD}	—	V_{DD}	V
V_{OL}	Low Level Output Voltage	I_{OL}=5mA	0	—	0.2×V_{DD}	V
Current Consumption						
I_{Sleep}	Deep Sleep Mode Current Consumption	BC5161/BC5162	—	0.5	1.0	μA
I_{IL}	Idle Mode Current Consumption	LIRC on, X'tal off (@WOT Idle mode)	—	2.5	—	μA
I_{Light}	Light Sleep Mode Current Consumption	X'tal on	—	1	—	mA
$I_{Standby}$	Standby Mode Current Consumption	X'tal on, Synthesizer on	—	5.5	—	mA
I_{TX}	TX Mode Current Consumption (High Power Matching)	TX mode @ -10dBm P_{OUT}	—	10.5	—	mA
		TX mode @ -5dBm P_{OUT}	—	12.5	—	
		TX mode @ -2dBm P_{OUT}	—	15.5	—	
		TX mode @ 5dBm P_{OUT}	—	19	—	
		TX mode @ 8dBm P_{OUT}	—	24	—	
	TX Mode Current Consumption (Low Power Matching)	TX mode @ -10dBm P_{OUT}	—	10.5	—	mA
		TX mode @ -5dBm P_{OUT}	—	11.5	—	
		TX mode @ 0dBm P_{OUT}	—	15.5	—	
		TX mode @ 2dBm P_{OUT}	—	17.5	—	
		TX mode @ 5dBm P_{OUT}	—	19.5	—	

A.C. Characteristics

Ta=25°C, V_{DD}=3.3V, f_{XTAL}=32MHz, GFSK modulation with matching circuit, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
RF Transmitter Characteristic						
f_{RF}	RF Operating Frequency Range	—	2402	—	2480	MHz
DR	Data Rate	GFSK modulation	125	—	500	Kbps
f_{DEV}	Frequency Deviation	Data Rate=125/250Kbps	—	160	—	kHz
		Data Rate=500Kbps	—	250	—	kHz
P_{OUT}	RF Transmit Output Power	—	-10	-2	8	dBm
$f_{channel}$	Channel Spacing	Non-overlapping channel spacing	—	1M	—	MHz
	Occupied Bandwidth	—	—	1M	—	MHz
S.E.$_{TX}$	TX Spurious Emission	f < 1GHz	—	—	-36	dBm
		47MHz < f < 74MHz 87.5MHz < f < 108MHz 174MHz < f < 230MHz 470MHz < f < 862MHz	—	—	-54	
		2^{nd}, 3^{rd} Harmonic	—	—	-30	
		1.8GHz ~ 1.9GHz	—	—	-20	
		5.15GHz ~ 5.3GHz	—	—	-30	

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Crystal (X'tal) Osicillator						
f_{XTAL}	X'tal Frequency	General cases	—	32	—	MHz
ESR	X'tal ESR	—	—	—	100	Ω
C_{LOAD}	X'tal Capacitor Load	—	12	—	16	pF
	X'tal Tolerance	—	-20	—	+20	ppm
$t_{Startup}$	X'tal Startup Time	49US with a 12pF C_{LOAD}	—	—	1	ms
		3225 SMD with a 12pF C_{LOAD}	—	3	—	
LO Characteristics						
f_{LO}	Frequency Coverage Range	—	2400	—	2500	MHz
PN_{LO}	Phase Noise	PN @ 100K offset	—	-85	—	dBc/Hz
		PN @ 1M offset	—	-95	—	

I²C Characteristics

Ta=-40°C~85°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I²C Characteristics						
f_{SCL}	Serial clock frequency	—	—	—	1	MHz
t_{BUF}	Bus free time between stop and start condition	SCL=1MHz	250	—	—	ns
t_{LOW}	SCL low time	SCL=1MHz	500	—	—	ns
t_{HIGH}	SCL high time	SCL=1MHz	500	—	—	ns
$t_{su(DAT)}$	Setup time SDA → SCL	SCL=1MHz	100	—	—	ns
$t_{su(STA)}$	Start condition setup time	SCL=1MHz	250	—	—	ns
$t_{su(STO)}$	Stop condition setup time	SCL=1MHz	250	—	—	ns
$t_{h(DAT)}$	Hold time SDA → SCL	SCL=1MHz	100	—	—	ns
$t_{h(STA)}$	Start condition hold time	SCL=1MHz	250	—	—	ns
$t_{r(SCL)}$	Rise time of SCL signal	SCL=1MHz	—	—	100	ns
$t_{f(SCL)}$	Fall time of SCL signal	SCL=1MHz	—	—	100	ns
$t_{r(SDA)}$	Rise time of SDA signal	SCL=1MHz	—	—	100	ns
$t_{f(SDA)}$	Fall time of SDA signal	SCL=1MHz	—	—	100	ns

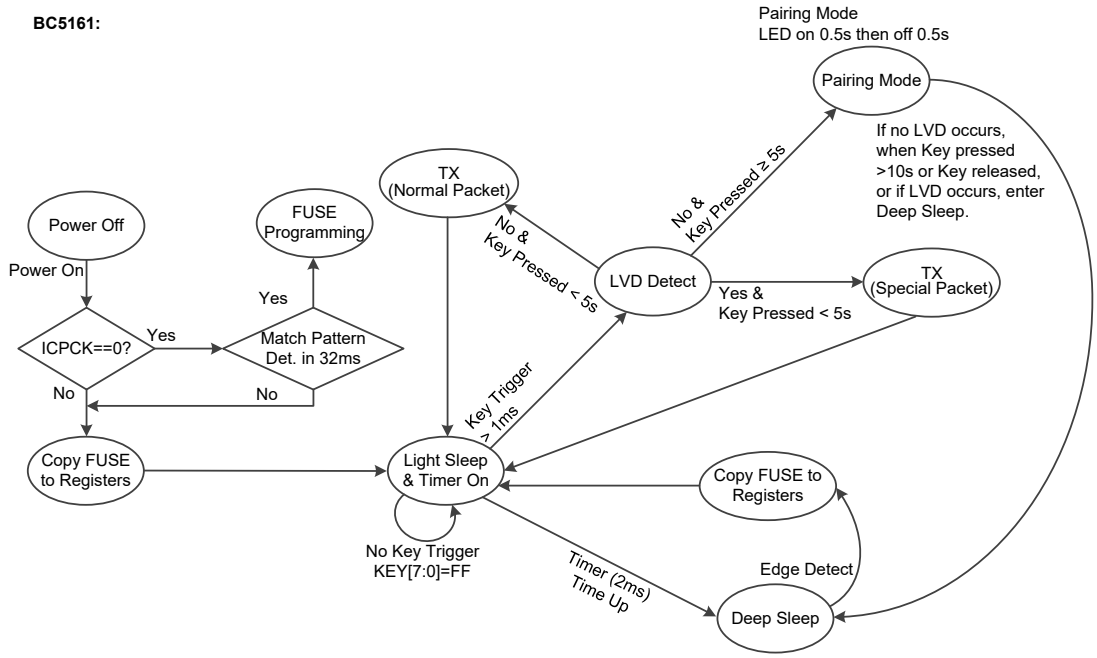
LVD Characteristics

Ta=25°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	—	2.0	—	3.6	V
V_{LVD}	Low Voltage Detection Voltage	LVD enable, voltage 2.2V	-10%	2.2	+10%	V
I_{OP}	Operating Current	LVD enable (@3V)	—	25	—	μA

Functional Description

State Machine – Key Mode (with LVD Function Enabled)



After power on, if the ICPCK pin is kept high, the FUSE data will be automatically copied to the corresponding registers and ready for key trigger.

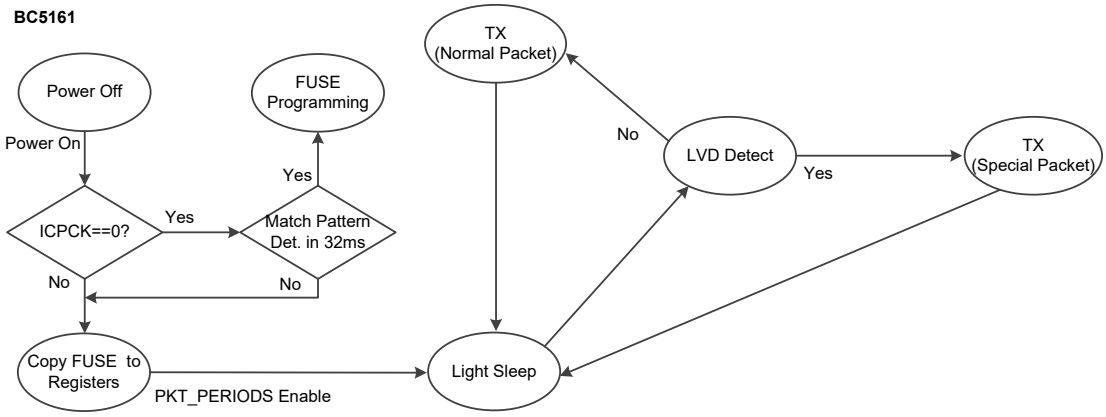
Note: 1. There are different conditons for the two modes to change them enter Deep Sleep, as described below.

(1) Key mode: If there is no any trigger event for 2ms.

(2) Pairing mode: If the key is still pressed for more than 10s or if the pressed key has been released.

2. In the Deep Sleep state, the only way to wake system up is Edge Detect. (All of I/Os should be pulled high, and active low.)
3. The Key De-bounce is Level trigger and the time is 1ms. The pressed key is valid when the pressing time exceeds 1ms.
4. When users press any individual key (one of 8 keys) for more than 5s, the device will enter the Pairing mode, the LED should flash (0.5s On/0.5s Off) to indicate this state. It will leave the Pairing mode when a 10s time is up or users release the pressed key, then go back to the Key mode and enter the Deep Sleep state. (Before entering or after leaving the pairing mode, the system should transmit all of packets for a complete hopping period then change state.)

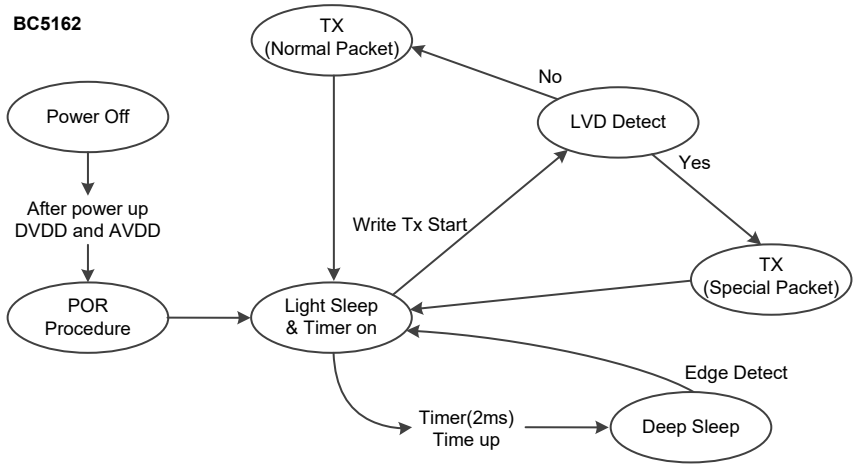
State Machine – WOT Mode (with LVD Function Enabled)



Note: 1. The WOT (Wake On TX), is used for period auto-send.

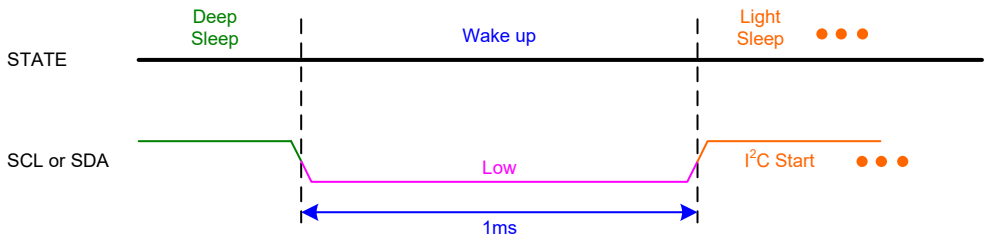
2. In the WOT mode, if a low voltage condition occurs, the LED will be continuously flashing.

State Machine – MCU Mode (with LVD Function Enabled)

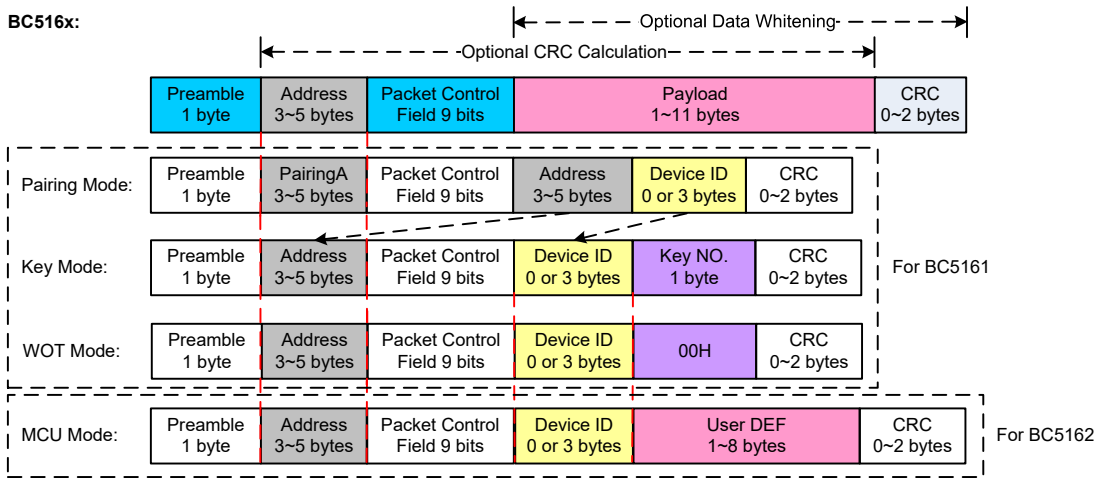


Note: The LVD function should first be enabled before Write TX Start.

Note that in the I²C mode, the device should be connected with an MCU and operate as an I²C slave. During the Light Sleep Mode, the timer will be on and will start counting. After a delay time of 2ms the device will enter the Deep Sleep Mode. If a toggle action occurs on the SDA or SCL pin, the timer will be reset and will restart counting. The device can be woken up from the Deep Sleep Mode if a falling edge is detected on pin SCL or SDA. Here it should be noted that the high-to-low pulse should be maintained for at least 1ms. In this situation the FUSE data will be copied to the registers again and the device will return to the Light Sleep Mode. In this way the MCU can generate a complete I²C format to initiate the follow-up state machine.



Packet Format



Note: 1. CRC is calculated over the Address, Packet Control Field and Payload.

2. Users can group by the LSB byte of Address.

3. Device ID can be enabled or disabled. If it is disabled, the packet format will skip Device ID.

4. In the Pairing mode, the TX power should be set to different power.

5. In the WOT mode, the packet format is similar to that in the Key mode, but the Key Field should be filled with "00H".

6. All of MSB of each field should be sent first, the low byte of Payload will be sent as well.

7. Payload length is automatically calculated by system through counting Payload bytes.

8. For the WOT mode, the original payload is 00H. When the LVD is enabled and a preset voltage is detected as well as the packet is sent, the payload will be 80H.

9. Key mode (LVD Disable) → The payload is still 1 byte.

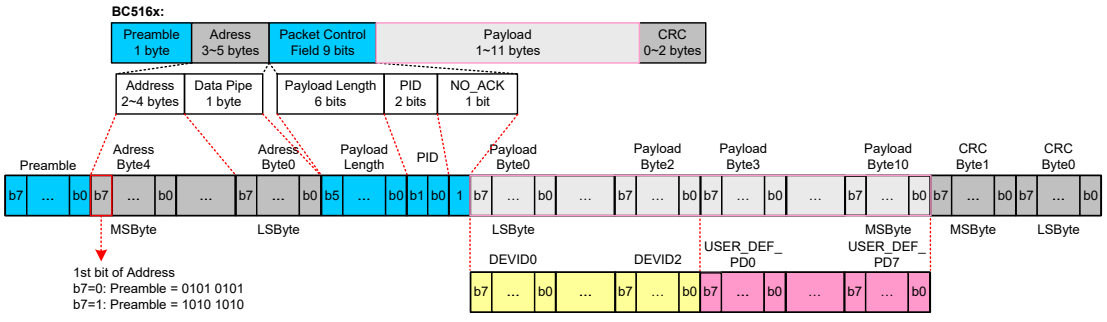
   Key mode (LVD Enable) → The payload bit 7 will become the LVD indicatior function.

   For example,

   When Key 0 is pressed and no low voltage condition occurs, the payload is 01111110b.

   When Key 0 is pressed and a low voltage condition occurs, the payload is 11111110b.

Packet Format On-Air Definition



Packet Format Field Definition

Function	FUSE Bits	Register Bits	Description
Preamble	0	0	0101 0101: The 1st bit of Address is 0 1010 1010: The 1st bit of Address is 1
Address	40	40	Address: 3~5 bytes
Pairing Address	40	40	Pairing Address: 3~5 bytes
Address Type	2	2	3~5 bytes
Packet Control Field	0	0	Packet length: 6 bits, automaticlly calculated by IC PID: 2 bits, Packet identification NO_ACK: 1-bit no acknowledge flag, this bit is set to 1 for the BC561x, i.e., NO_ACK=1
Device ID	24	24	Device Identification number
Enable Device ID	1	1	0: Disable Device ID, the packet format will neglect this field 1: Enable Device ID
User DEF Payload	0	64	User defined payload (Payload: last 1~8 bytes) in the MCU (I^2C) mode
Security	1	1	Bit 0: Disable/Enable encryption (LFSR→Whiting)
Encryption Key	8	8	Encryption Key
CRC (Optional)	2	2	Bit 0=0: Disable, 1: Enable Bit 1=0: 1 byte, 1: 2 bytes

Packet Format Control

Preamble

The BC516x have one-byte long Preamble which is a bit sequence of either 01010101 or 10101010. This sequence is calculated automatically by IC depending on the fist bit of Address. The definition is listed below:

1st bit of Address:

0: Preamble=01010101

1: Preamble=10101010

Address

The Address has a flexible length between 3 and 5 bytes for transmitters, users can set it by Address type of FUSE and PKT_ADDRT[1:0] (reference: CFG24). The BC516x have two Addresses, one is used for normal mode and another is used for pairing mode, the definition is listed below:

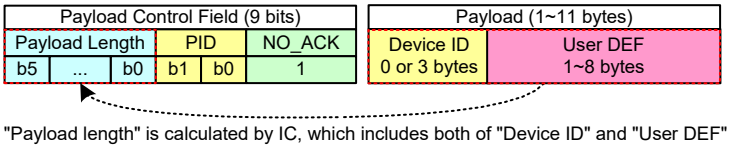
Support IC	Normal Mode			Pairing Mode
	Key Mode	WOT Mode	MCU Mode	
BC5161	Y	Y	X	Y
BC5162	X	X	Y	X

Y: Support; X: Doesn't support

- Normal mode: FUSE CFG14~CFG18, PKT_ADDRB4[7:0]~PKT_ADDRB0[7:0]
  Available Packet Format: Key mode, WOT mode, MCU mode
- Pairing mode: FUSE CFG19~CFG23, PKT_PAIRB4[7:0]~PKT_PAIRB0[7:0]
  Available Packet Format: Pairing mode

Packet Control Field

The Packet control field is a 9-bit long field, which defines “Payload length”, “PID”, and “NO_ACK”, the description is listed below:



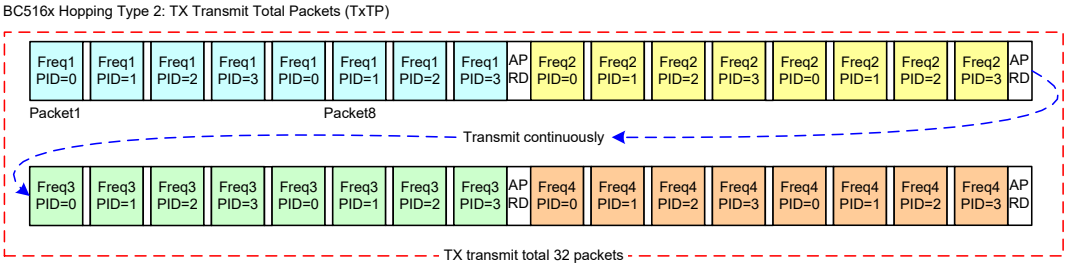
- Payload Length: 6 bits
  The Payload Length is calculated automatically by IC, depending on the type of packet format for the BC516x, which includes both of “Device ID” and “User DEF”. The length of the Payload can be 1 to 11 bytes, users do no need to care it exceeds 11 bytes.

Packet Format	Payload Length		Payload Description
	BC5161	BC5162	
Paring Mode	3~8	X	Address (3~5 bytes) + Device ID (0 or 3 bytes)
Key Mode	1~4	X	Device ID (0 or 3 bytes) + Key (1 byte)
WOT Mode	1~4	X	Device ID (0 or 3 bytes) + Dummy (1 byte, 00H)
MCU Mode	X	1~11	Device ID (0 or 3 bytes) + User DEF (1~8 bytes)

X: Doesn’t support

- PID (Packet Identification): 2 bits
  This PID is a 2-bit long Packet Identification filed which is used to reduce the packet being discarded chance from the other TX of the BC516x with the same Address but differenct Device ID. The PID of the BC516x starts with 0 and increases 1 for next packet and will be reset after the PID is equal to 3 for each next transmitting packet, it is not only for a new packet but also for a retransmitting packet.

  For example, the following figure is a complete period of Hopping Type 2, the Auto Resend is 7 and all of packets have the same payload. The Freq1 packet is transmitted 8 times, the PID starts with 0, and increases 1 for each next packet but will be reset after the PID is equal to 3 for each next transmitting packet.



  The PID value will be retained in 3V Domain, so even if the IC wakes up from Deep Sleep, the PID value will continue instead of starting from 0.

- NO_ACK: 1 bit
  This field is a 1-bit long no acknowledge indication and is always “1” for the BC516x. Since the BC516x is a transmitter only IC without receiver, it can not receive ACK signal.

Payload

The payload can be 0 to 11 bytes for the BC516x. Once the RFTXSTART bit is enabled, the payload is transmitted on-air. There are 4 kinds of packet format which include Pairing, Key, WOT and MCU modes, most of them have fixed length of payload after the FUSE is programmed, but only MCU mode has dynamic payload length.

- Device ID: 0 or 3 bytes
  FUSE CFG26~CFG28, PKT_DEVIDE2[7:0]~PKT_DEVIDE0[7:0]

  If PKT_DEVIDEE is 1, “Device ID” would be used (3 bytes), else the IC will ignore “Device ID” (0 byte).

- Key NO.: 1 byte
  It is generated by each Key which has been triggered from D0 to D7.

PKT_DEVID0[7:0]~PKT_DEVID2[7:0]									Key NO.		
Byte 0			Byte 1			Byte 2			1 Byte		
b7	...	b0	b7	...	b0	b7	...	b0	D7	...	D0

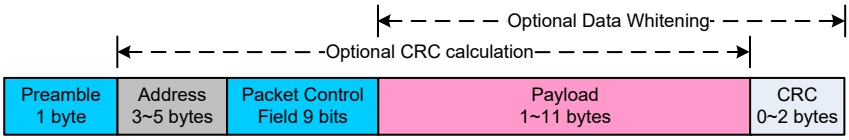
- User DEF: 0~8 bytes
  CFG40~CFG47, USER_DEF_PD0[7:0]~USER_DEF_PD7[7:0]

  The "User DEF" payload depends on each time the MCU consecutively writes via I²C Page Write command only, and start byte should be the lowest byte of User DEF for USER_DEF_PD0[7:0].

Payload 1~11 bytes																			
PKT_DEVID0[7:0]~PKT_DEVID2[7:0]									USER_DEF_PD0[7:0]~USER_DEF_PD7[7:0]										
Byte 0			Byte 1			Byte 2			Byte 0			Byte 1			...	Byte 7		
b7	...	b0	b7	...	b0	b7	...	b0	b7	...	b0	b7	...	b0		b7	...	b0

Note: Even though users can write the CFG40~CFG47 via I²C Byte Write command but it will not be counted by the IC internal pointer of payload.

CRC (Cyclic Redundancy Check)



The CRC is a optional field which is selected by PKT_CRCS[1:0] for the BC516x. It is recommended to always set the CRC enable bit PKT_CRCS[0] to 1 for data integrity checking. There are two CRC formulas selected by setting PKT_CRCS[1]. The CRC is either 1 or 2 bytes, both of formulas are calculated over the same fields which are Address, Packet Control Field and Payload.

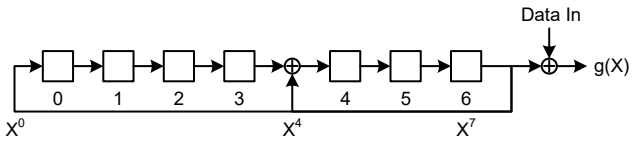
CRC	Polynomial	PKT_CRCS[1:0]		Description / Formula	Initial Value
		b1	b0		
Disable	/	X	0	CRC is disabled	X
CRC-8	0x07	0	1	$X^8 + X^2 + X + 1$	FFh
CRC-CCITT	0x1021	1	1	$X^{16} + X^{12} + X^5 + 1$	FFFFh

X: don't care

Security

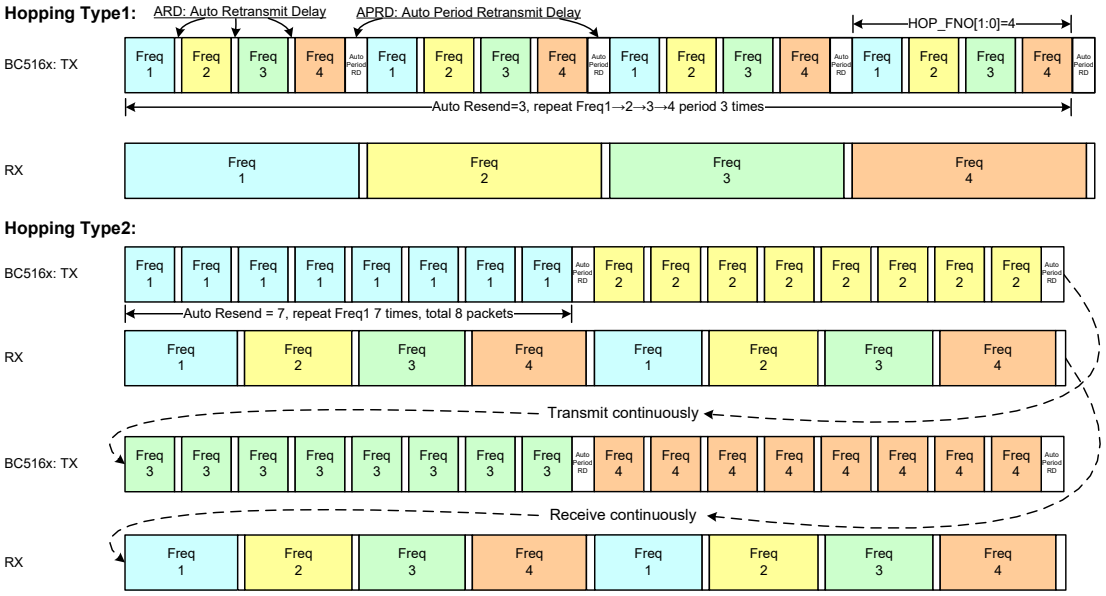
The security, which is optional and is set by the PKT_SECURIT bit, is implemented by LFSR (Data Whitening) for the BC516x. The formula listed below calculates both of payload and CRC field (Data In). The Packet Encryption Key is PKT_ENCRYPK[6:0], its initial value is 0x01, i.e., its initial bit 0=1.

$$g(X)=X^7 + X^4 + 1$$



0: PKT_ENCRYPK[0]
1: PKT_ENCRYPK[1]
2: PKT_ENCRYPK[2]
3: PKT_ENCRYPK[3]
4: PKT_ENCRYPK[4]
5: PKT_ENCRYPK[5]
6: PKT_ENCRYPK[6]

Hopping Timing Diagram



Rule:

1. Hopping Type1: The BC516x should send N (1~4) packets with different kinds of hopping frequency.

   If auto resend=3, N packets will repeatedly send 3 times, total send packets=N × (3+1)=N×4 packets, where N stands for total number of hoping frequency.

2. Hopping Type2: If auto resend=7, total number of hoping frequency=4, the BC516x will send (7+1) packets with the same frequency then hop to next frequency, until finish N. Total send packets=(7+1) × 4=32 packets.

3. If N=1, then the BC516x will only send hoping Freq 1.

4. The initial PID is 0 and it should increase by 1 for the next packet. Once it counts to 3, the next one should reset to 0.

5. The MCU mode (I^2C), Key mode, Pairing mode and WOT mode have the same rules as above.

6. The TX transmit total packet number is dependent on Auto Resend (CFG31) PKT_AUTORS[3:0], Hopping Mode (CFG31), HOP_MOD[1:0] and Hopping Frequency total number HOP_FNO[1:0].

I^2C Serial Programming – BC5162

The transmitter only supports the I^2C format for byte write, page write, byte read and page read formats.

It should be noted that the I^2C is a non-standard I^2C interface, which only supports a single device for connection.

Symbol definition:

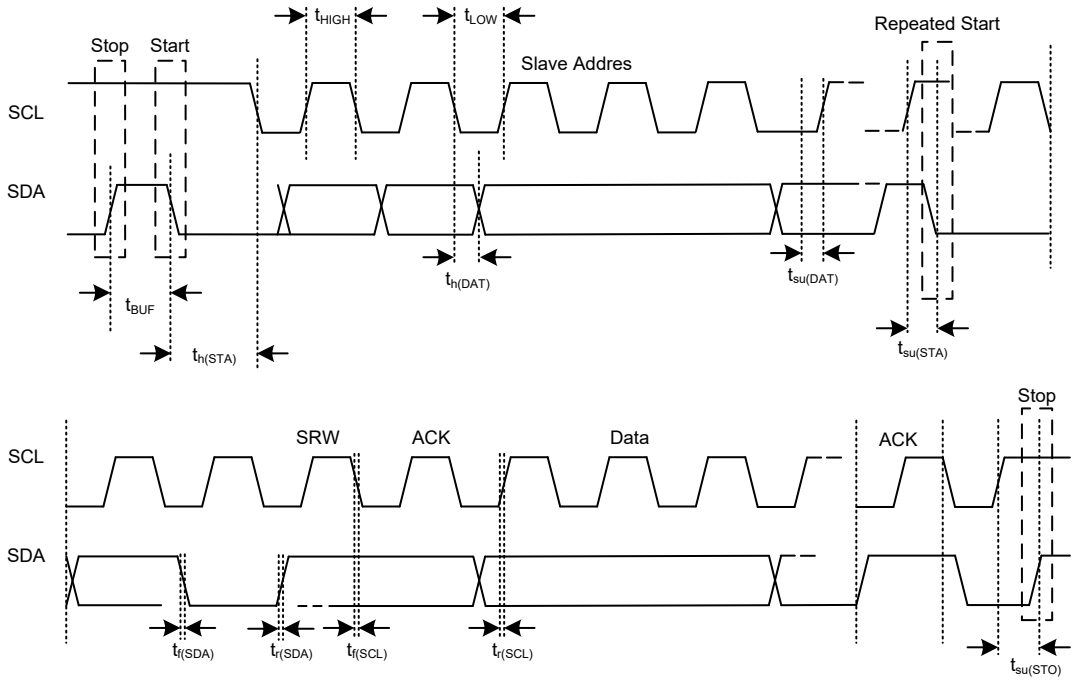
- S: Start symbol
- RS: Repeat Start
- P: Stop symbol
- DADDR[6:0]: Device address, 51h
- R/W: Read/Write select; R(0): Write; (1): Read
- RADDR[7:0]: Register address
- ACK: A(0): ACK; NA(1): NAK
- Bus Direction:
  Host to device:
  Device to host:

Byte Write

Page Write

Byte Read

Page Read



S = Start (1 bit)
SA = Slave Address (7 bits)
SR = SRW bit (1 bit)
M = Slave device send acknowledge bit (1 bit)
D = Data (8 bits)
A = ACK (RXAK bit for transmitter, TXAK for receiver, 1 bit)
P = Stop (1 bit)

Programming Methodology – BC5161

The device programming interface should utilise an adaptor with an integrated 32MHz crystal.

When programming the device need to be located on a Socket with a 32MHz crystal connected between pin XOIN and ground. Holtek provides an e-Link or e-WriterPro tool for communication with the PC.

Between the e-Link and the device there are four interconnecting lines, namely VDD, VSS, ICPCK and ICPDA pins.

Programming Function	Pin Name	Pin Description
ICPCK	ICPCK	ICP clock
ICPDA	ICPDA	ICP data/address
VDD	AVDD & DVDD	Power supply
VSS	Exposed-PAD	Ground
XTAL IN	XOIN	IC system clock

Configuration Registers

All control registers will be set to their initial value by power-on reset (POR).

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
00h	CFG0	—	EFPGM	XO_TRIM[5:0]					
03h	CFG3	—				USER_DR[2:0]			USER_LED_SWD
0Ch	CFG12	RFTXP_1							
0Dh	CFG13	RFTXP_2							
0Eh	CFG14	PKT_ADDRB0[7:0]							
0Fh	CFG15	PKT_ADDRB1[7:0]							
10h	CFG16	PKT_ADDRB2[7:0]							
11h	CFG17	PKT_ADDRB3[7:0]							
12h	CFG18	PKT_ADDRB4[7:0]							
13h	CFG19	PKT_PAIRB0[7:0]							
14h	CFG20	PKT_PAIRB1[7:0]							
15h	CFG21	PKT_PAIRB2[7:0]							
16h	CFG22	PKT_PAIRB3[7:0]							
17h	CFG23	PKT_PAIRB4[7:0]							
18h	CFG24	PKT_ADDRT[1:0]		PKT_DEVIDE	PCF_EN	LVD_FLASH_EN	PKT_CRCS[1:0]		—
19h	CFG25	PKT_SECURIT	PKT_ENCRYPK[6:0]						
1Ah	CFG26	PKT_DEVID0[7:0]							
1Bh	CFG27	PKT_DEVID1[7:0]							
1Ch	CFG28	PKT_DEVID2[7:0]							
1Dh	CFG29	PKT_PERIODS0[7:0]							
1Eh	CFG30	PKT_PERIODS1[7:0]							
1Fh	CFG31	HOP_MOD[1:0]		HOP_FNO[1:0]		PKT_AUTORS[3:0]			
20h	CFG32	PKT_ARD[3:0]				PKT_APRD[3:0]			
21h	CFG33	—	HOP_FREQ1[6:0]						
22h	CFG34	—	HOP_FREQ2[6:0]						
23h	CFG35	—	HOP_FREQ3[6:0]						
24h	CFG36	—	HOP_FREQ4[6:0]						
25h	CFG37	—					OPLVD[1:0]		LVDEN
26h	CFG38	EFCRC_L[7:0]							
27h	CFG39	EFCRC_H[7:0]							
28h	CFG40	USER_DEF_PD0[7:0]							
29h	CFG41	USER_DEF_PD1[7:0]							
2Ah	CFG42	USER_DEF_PD2[7:0]							
2Bh	CFG43	USER_DEF_PD3[7:0]							
2Ch	CFG44	USER_DEF_PD4[7:0]							
2Dh	CFG45	USER_DEF_PD5[7:0]							
2Eh	CFG46	USER_DEF_PD6[7:0]							
2Fh	CFG47	USER_DEF_PD7[7:0]							
30h	CFG48	RFTXSTART	—			USER_DEF_PD[3:0]			

Note: 1. For the addresses which are not listed in this table, it is suggested not to change their initial values.

2. The FUSE must not un-programmed, so the BC516x need to be programmed by Holtek RF chip parameters setting tool before use.

- **CFG0: Configuration Control Register 0**

Bit	7	6	5	4	3	2	1	0
Name	—	EFPGM	XO_TRIM[5:0]					
R/W	—	R	R/W	—	—	—	—	—
POR	0	0	1	0	0	0	0	0

Bit 7 Reserved bits, cannot be changed

Bit 6 **EFPGM:** FUSE programmed, read only by the Holtek RF Tool
0: FUSE is not programmed – FUSE data is not mapped to the configuration registers
1: FUSE is programmed – FUSE data is mapped to the configuration registers

Bit 5~0 **XO_TRIM[5:0]**: Trim value for the internal capacitor load of the crystal

- **CFG3: Configuration Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	—				USER_DR[2:0]			USER_LED_SWD
R/W	—	—	—	—	—	—	—	—
POR	0	1	1	0	0	0	0	0

Bit 7~4 Reserved bits, must be set to "0111"

Bit 3~1 **USER_DR[2:0]**: Data Rate setup
000: Reserved
001: 125Kbps
010: 250Kbps
011: 500Kbps
1xx: Reserved

Bit 0 **USER_LED_SWD:** LED flash
0: LED follows TX
1: LED follows symbol high

- **CFG12: Configuration Control Register 12**

Bit	7	6	5	4	3	2	1	0
Name	RFTXP_1							
R/W	R/W							
POR	1	0	1	0	0	0	0	1

- **CFG13: Configuration Control Register 13**

Bit	7	6	5	4	3	2	1	0
Name	RFTXP_2							
R/W	R/W							
POR	1	0	1	0	0	0	0	1

The recommended setting values (hexadecimal) for the CFG12 and CFG13 registers are listed below.

8-pin SOP-EP

TX Power	High Power Matching		Low Power Matching	
	CFG12 (RFTXP_1)	CFG13 (RFTXP_2)	CFG12 (RFTXP_1)	CFG13 (RFTXP_2)
8dBm	A1	AF		
5dBm	A2	67	A1	A7
2dBm			A2	63
0dBm			AF	D7
-2dBm	AF	D7		
-5dBm	AF	77	AF	73
-10dBm	AF	71	AF	51

16-pin QFN

TX Power	High Power Matching		Low Power Matching	
	CFG12 (RFTXP_1)	CFG13 (RFTXP_2)	CFG12 (RFTXP_1)	CFG13 (RFTXP_2)
8dBm	A1	AF		
5dBm	A2	83	A1	A7
2dBm			A2	83
0dBm			AF	D7
-2dBm	AF	73		
-5dBm	AF	71	AF	77
-10dBm	A1	AF	AF	71

- **CFG14: Configuration Control Register 14**

Bit	7	6	5	4	3	2	1	0
Name	PKT_ADDRB0[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PKT_ADDRB0[7:0]**: Packet Format Address byte 4

BC516x Packet Format:

Address: PKT_ADDRB4[7:0]~PKT_ADDRB0[7:0]

- **CFG15: Configuration Control Register 15**

Bit	7	6	5	4	3	2	1	0
Name	PKT_ADDRB1[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PKT_ADDRB1[7:0]**: Packet Format Address byte 3

- **CFG16: Configuration Control Register 16**

Bit	7	6	5	4	3	2	1	0
Name	PKT_ADDRB2[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PKT_ADDRB2[7:0]**: Packet Format Address byte 2

- **CFG17: Configuration Control Register 17**

Bit	7	6	5	4	3	2	1	0
Name	PKT_ADDRB3[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PKT_ADDRB3[7:0]**: Packet Format Address byte 1

- **CFG18: Configuration Control Register 18**

Bit	7	6	5	4	3	2	1	0
Name	PKT_ADDRB4[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

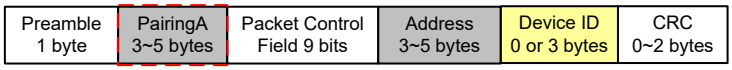
Bit 7~0 **PKT_ADDRB4[7:0]**: Packet Format Address byte 0

- **CFG19: Configuration Control Register 19**

Bit	7	6	5	4	3	2	1	0
Name	PKT_PAIRB0[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PKT_PAIRB0[7:0]:** Packet Format Pairing Address byte 4

Pairing Mode:



- **CFG20: Configuration Control Register 20**

Bit	7	6	5	4	3	2	1	0
Name	PKT_PAIRB1[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PKT_PAIRB1[7:0]**: Packet Format Pairing Address byte 3

- **CFG21: Configuration Control Register 21**

Bit	7	6	5	4	3	2	1	0
Name	PKT_PAIRB2[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PKT_PAIRB2[7:0]**: Packet Format Pairing Address byte 2

- **CFG22: Configuration Control Register 22**

Bit	7	6	5	4	3	2	1	0
Name	PKT_PAIRB3[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PKT_PAIRB3[7:0]**: Packet Format Pairing Address byte 1

- **CFG23: Configuration Control Register 23**

Bit	7	6	5	4	3	2	1	0
Name	PKT_PAIRB4[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PKT_PAIRB4[7:0]**: Packet Format Pairing Address byte 0

- **CFG24: Configuration Control Register 24**

Bit	7	6	5	4	3	2	1	0
Name	PKT_ADDRT[1:0]		PKT_DEVIDE	PCF_EN	LVD_FLASH_EN	PKT_CRCS[1:0]		—
R/W	R/W							
POR	0	0	0	1	0	0	0	1

Bit 7~6 **PKT_ADDRT[1:0]**: Packet Address type 3~5 bytes selection (Address / Pairing Address)
00: 3 bytes, only 3 lowest bytes of address will be sent for packet format on-air
01: 4 bytes, only 4 lowest bytes of address will be sent for packet format on-air
1x: 5 bytes, all of 5 bytes of address will be sent for packet format on-air

Bit 5 **PKT_DEVIDE:** Packet format Device ID enable control
0: Disable packet format Device ID, this field will not be sent
1: Enable packet format Device ID, this field should be sent following the packet control field

Bit 4 **PCF_EN**: Packet Control Field control
0: No Packet Control Field
1: With Packet Control Field

Bit 3 **LVD_FLASH_EN**: LED flash control when LVD occurs
0: LED does not flash
1: LED flashes, LED on 50ms then off 200ms

Bit 2 **PKT_CRCS[1:0]**: Packet CRC byte number selection
PKT_CRCS[1]: Packet format CRC byte option
0: 1 byte, the CRC fomular is X8 + X2 + X + 1, its initial value is 0xFF
1: 2 bytes, the CRC fomular is X16+ X12 + X5 + 1, its initial value is 0xFFFF
PKT_CRCS[0]: Packet format CRC enable control
0: Disable
1: Enable

Bit 0 Reserved bit
It is suggested that after power on this bit should be cleared to zero for the BC5161 and kept unchanged for the BC5162.

- **CFG25: Configuration Control Register 25**

Bit	7	6	5	4	3	2	1	0
Name	PKT_SECURIT	PKT_ENCRYPK[6:0]						
R/W	R/W							
POR	0	0	0	0	0	0	0	1

Bit 7 **PKT_SECURIT**: Security enable control
0: Disable
1: Enable encryption (==> Whitening: polynomial g(X)=X7+X4+1)

Bit 6~0 **PKT_ENCRYPK[6:0]**: Data whitening seed

- **CFG26: Configuration Control Register 26**

Bit	7	6	5	4	3	2	1	0
Name	PKT_DEVID0[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PKT_DEVID0[7:0]**: Packet Device ID 0, payload byte 0

- **CFG27: Configuration Control Register 27**

Bit	7	6	5	4	3	2	1	0
Name	PKT_DEVID1[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PKT_DEVID1[7:0]**: Packet Device ID 1, payload byte 1

- **CFG28: Configuration Control Register 28**

Bit	7	6	5	4	3	2	1	0
Name	PKT_DEVID2[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PKT_DEVID2[7:0]**: Packet Device ID 2, payload byte 2

- **CFG29: Configuration Control Register 29**

Bit	7	6	5	4	3	2	1	0
Name	PKT_PERIODS0[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PKT_PERIODS0[7:0]**: Period Send[15:0] low byte

- **CFG30: Configuration Control Register 30**

Bit	7	6	5	4	3	2	1	0
Name	PKT_PERIODS1[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PKT_PERIODS1[7:0]**: Period Send[15:0] high byte

Period Send[15:0]=

0000H: Disable, WOT is disabled

0001H~FFFFH: WOT is enabled and the counter follows it. Take 10ms as a step, 10ms×Period Send[15:0].

- **CFG31: Configuration Control Register 31**

Bit	7	6	5	4	3	2	1	0
Name	HOP_MOD[1:0]		HOP_FNO [1:0]		PKT_AUTORS[3:0]			
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~6 **HOP_MOD[1:0]**: Hopping Mode selection

HOP_MOD[1]: Hopping Mode Type selection

0: Hopping Type 1 – TX hops for all hopping channels then RX hops

1: Hopping Type 2 – TX resends several times then hops, RX hops for each channel whin the same TX channel

HOP_MOD[0]: Hopping Mode enable control

0: Disable, don't hop

1: Enable, hop by the specified Freq1~4 in sequence

Bit 5~4 **HOP_FNO[1:0]**: Hopping frequency number selection

00: 1 frequency (don't hop)

01: 2 frequencies

10: 3 frequencies

11: 4 frequencies

Bit 3~0 **PKT_AUTORS[3:0]**: Packet Auto Resend 0~15 times selection

- **CFG32: Configuration Control Register 32**

Bit	7	6	5	4	3	2	1	0
Name	PKT_ARD[3:0]				PKT_APRD[3:0]			
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~4 **PKT_ARD[3:0]**: Auto Retransmit Delay for each packet

Auto Retransmit Delay (ARD)=380μs+250μs×(PKT_ARD[3:0])

0000: 380μs

0001: 630μs

…

1111: 4130μs

Bit 3~0 **PKT_APRD[3:0]**: Auto Period Retransmit Delay for the last packet of each period (dependent on APRD)

Period Delay (APRD)=380μs+250μs×(PKT_APRD[3:0])

0000: 380μs

0001: 630μs

…

1111: 4130μs

- **CFG33: Configuration Control Register 33**

Bit	7	6	5	4	3	2	1	0
Name	—	HOP_FREQ1[6:0]						
R/W	R/W							
POR	0	0	0	0	0	0	1	0

Bit 7 Reserved bit, cannot be changed

Bit 6~0 **HOP_FREQ1[6:0]**: Hopping Frequency 1 channel selection
Hopping Frequency 1=2400+HOP_FREQ1[6:0] (MHz)
For example, HOP_FREQ1[6:0]=2, Hopping Frequency 1=2400+2=2402 (MHz)

- **CFG34: Configuration Control Register 34**

Bit	7	6	5	4	3	2	1	0
Name	—	HOP_FREQ2[6:0]						
R/W	R/W							
POR	0	0	0	0	0	0	1	0

Bit 7 Reserved bit, cannot be changed

Bit 6~0 **HOP_FREQ2[6:0]**: Hopping Frequency 2 channel selection
Hopping Frequency 2=2400+HOP_FREQ2[6:0] (MHz)
For example, HOP_FREQ2[6:0]=20, Hopping Frequency 2=2400+20=2420 (MHz)

- **CFG35: Configuration Control Register 35**

Bit	7	6	5	4	3	2	1	0
Name	—	HOP_FREQ3[6:0]						
R/W	R/W							
POR	0	0	0	0	0	0	1	0

Bit 7 Reserved bit, cannot be changed

Bit 6~0 **HOP_FREQ3[6:0]**: Hopping Frequency 3 channel selection
Hopping Frequency 3=2400+HOP_FREQ3[6:0] (MHz)
For example, HOP_FREQ3[6:0]=44, Hopping Frequency 3=2400+44=2444 (MHz)

- **CFG36: Configuration Control Register 36**

Bit	7	6	5	4	3	2	1	0
Name	—	HOP_FREQ4[6:0]						
R/W	R/W							
POR	0	0	0	0	0	0	1	0

Bit 7 Reserved bit, cannot be changed

Bit 6~0 **HOP_FREQ4[6:0]**: Hopping Frequency 4 channel selection
Hopping Frequency 4=2400+HOP_FREQ4[6:0] (MHz)
For example, HOP_FREQ4[6:0]=80, Hopping Frequency 4=2400+80=2480 (MHz)

- **CFG37: Configuration Control Register 37**

Bit	7	6	5	4	3	2	1	0
Name	—					OPLVD[1:0]		LVDEN
R/W	R/W							
POR	1	0	1	1	0	1	0	0

Bit 7~3 Reserved bits, cannot be changed

Bit 2~1 **OPLVD[1:0]**: LVD voltage selection

00: Reserved

01: 2.2V

10: Reserved

11: Reserved

Bit 0 **LVDEN**: LVD function enable control

0: Disable

1: Enable

If the LVD function is enabled, the payload bit 7 will become the LVD indicatior function.

For example, when Key 0 is pressed and no low voltage condition occurs, the payload is 01111110b. When Key 0 is pressed and a low voltage condition occurs, the payload is 11111110b.

- **CFG38: Configuration Control Register 38**

Bit	7	6	5	4	3	2	1	0
Name	EFCRC_L[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **EFCRC_L[7:0]**: EFCRC field low byte

- **CFG39: Configuration Control Register 39**

Bit	7	6	5	4	3	2	1	0
Name	EFCRC_H[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **EFCRC_H[7:0]**: EFCRC field high byte

The EFCRC field is used for FUSE CRC calculation. The address range of the CRC calculation is from 00h to 1Eh, which contains 31 bytes in total. The input order is LSB first, the CRC polynomial is X16 +X15+X2+1. The CRC on-line calculator can be accessed by the following website: http://www.sunshine2k.de/coding/javascript/crc/crc_js.html.

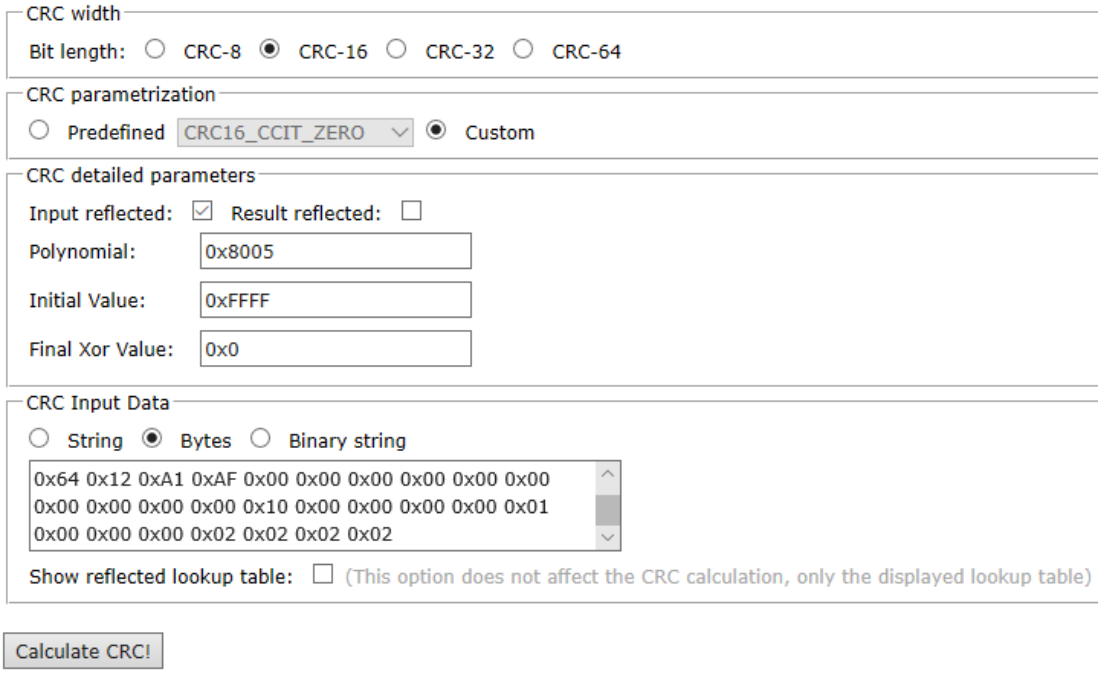
For example, data filled in the address range of 00h~24h are listed below: 0x60 0x00 0x00 0x70 0x02 0x30 0x66 0x95 0x4A 0x00 0x64 0x12 0xA1 0xAF 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x10 0x00 0x00 0x00 0x00 0x01 0x00 0x00 0x00 0x02 0x02 0x02 0x02.

The online calculator should be setup with the following configuration:

1. CRC width: select “CRC-16”
2. CRC parametrization: select “Custom”
3. CRC detailed parameters: select “Input reflected”
4. Polynomial: 0x8005
5. Initial Value: 0xFFFF
6. Final Xor Value: 0x0
7. CRC Input Data: select “Bytes” and fill in the data

8. Click on “Calculate CRC!”
9. Result CRC Value: 0x9172

As the following on-line calculator web interface screenshot shows:



- **CFG40: Configuration Control Register 40**

Bit	7	6	5	4	3	2	1	0
Name	USER_DEF_PD0[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **USER_DEF_PD0[7:0]**: User Defined Payload 0

- **CFG41: Configuration Control Register 41**

Bit	7	6	5	4	3	2	1	0
Name	USER_DEF_PD1[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **USER_DEF_PD1[7:0]**: User Defined Payload 1

- **CFG42: Configuration Control Register 42**

Bit	7	6	5	4	3	2	1	0
Name	USER_DEF_PD2[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **USER_DEF_PD2[7:0]**: User Defined Payload 2

- **CFG43: Configuration Control Register 43**

Bit	7	6	5	4	3	2	1	0
Name	USER_DEF_PD3[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **USER_DEF_PD3[7:0]**: User Defined Payload 3

- **CFG44: Configuration Control Register 44**

Bit	7	6	5	4	3	2	1	0
Name	USER_DEF_PD4[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **USER_DEF_PD4[7:0]**: User Defined Payload 4

- **CFG45: Configuration Control Register 45**

Bit	7	6	5	4	3	2	1	0
Name	USER_DEF_PD5[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **USER_DEF_PD5[7:0]**: User Defined Payload 5

- **CFG46: Configuration Control Register 46**

Bit	7	6	5	4	3	2	1	0
Name	USER_DEF_PD6[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **USER_DEF_PD6[7:0]**: User Defined Payload 6

- **CFG47: Configuration Control Register 47**

Bit	7	6	5	4	3	2	1	0
Name	USER_DEF_PD7[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **USER_DEF_PD7[7:0]**: User Defined Payload 7

- **CFG48: Configuration Control Register 48**

Bit	7	6	5	4	3	2	1	0
Name	RFTXSTART	—			USER_DEF_PD[3:0]			
R/W	R/W							
POR	0	0	0	0	1	0	0	0

Bit 7 **RFTXSTART**: RF start to transmit control

0: RF TX stops

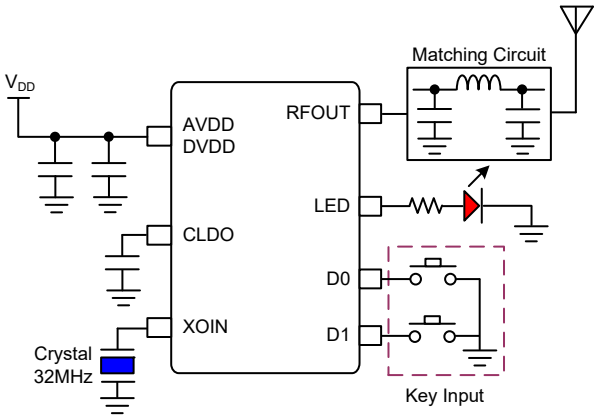
1: RF TX starts

After all of payload is transmitted, this bit will be cleared to zero or cleared by the MCU, the RF TX will stop.

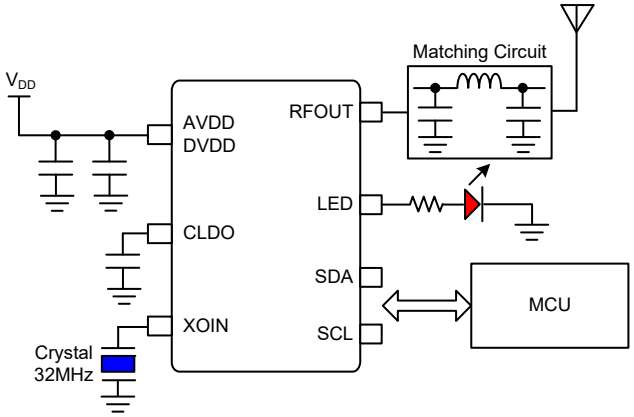
Bit 6~4 Reserved bits, cannot be changed

Bit 3~0 **USER_DEF_PF[3:0]**: 1~8 bytes (Max.)

Application Circuits



Key Mode – BC5161



I²C Mode – BC5162

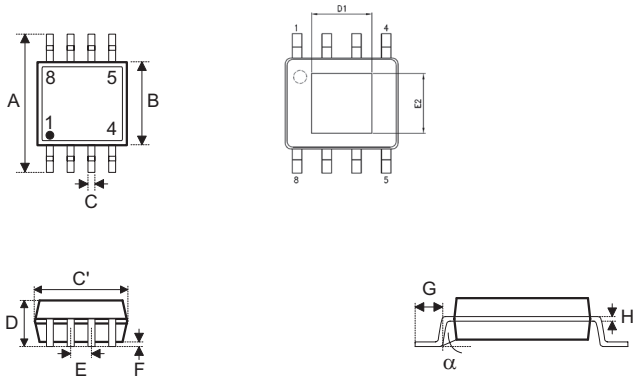
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the package information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

8-pin SOP-EP (150mil) Outline Dimensions

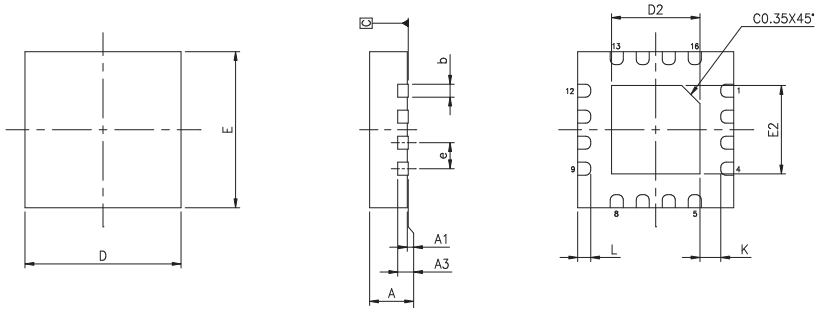


Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.020
C'	—	0.193 BSC	—
D	—	—	0.069
D1	0.076	—	0.090
E	—	0.050 BSC	—
E2	0.076	—	0.090
F	0.000	—	0.006
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.00 BSC	—
B	—	3.90 BSC	—
C	0.31	—	0.51
C'	—	4.90 BSC	—
D	—	—	1.75
D1	1.94	—	2.29
E	—	1.27 BSC	—
E2	1.94	—	2.29
F	0.00	—	0.15
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°

Note: For this package type, refer to the package information provided here, which will not be updated by the Holtek website.

SAW Type 16-pin QFN (3mm×3mm, FP0.25mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.007	0.010	0.012
D	—	0.118 BSC	—
E	—	0.118 BSC	—
e	—	0.020 BSC	—
D2	0.063	0.067	0.069
E2	0.063	0.067	0.069
L	0.008	0.010	0.012
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	—	0.20 BSC	—
b	0.18	0.25	0.30
D	—	3.00 BSC	—
E	—	3.00 BSC	—
e	—	0.50 BSC	—
D2	1.60	1.70	1.75
E2	1.60	1.70	1.75
L	0.20	0.25	0.30
K	0.20	—	—