HT32F52220/HT32F52230
Datasheet

32-Bit Arm® Cortex®-M0+ Microcontroller,
up to 32 KB Flash and 4 KB SRAM with 1 MSPS ADC,
USART, UART, SPI, I²C, GPTM, SCTM, BFTM, WDT

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1 General Description

The HOLTEK HT32F52220/52230 devices are high performance, low power consumption 32-bit microcontrollers based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The devices operate at a frequency of up to 40 MHz for HT32F52220/52230 with a Flash accelerator to obtain maximum efficiency. It provides up to 32 KB of embedded Flash memory for code/data storage and 4 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, I^2C, USART, UART, SPI, GPTM, SCTM, BFTM, WDT, SW-DP (Serial Wire Debug Port), etc., are also implemented in the device series. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the devices are suitable for use in a wide range of applications, especially in areas such as white goods application control, power monitors, alarm systems, consumer products, handheld equipment, data logging applications, motor control and so on.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 40 MHz operating frequency
- 0.93 DMIPS/MHz (Dhrystone v2.1)
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets; single-cycle I/O port; hardware multiplier and low latency interrupt respond time.

On-chip Memory

- Up to 32 KB on-chip Flash memory for instruction/data and options storage
- 4 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M0+ processor accesses and debug accesses share the single external interface to external AHB peripherals. The processor accesses take priority over debug accesses. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 shows the memory map of the HT32F522320/52230 series of devices, including code, SRAM, peripheral, and other pre-defined regions.

Flash Memory Controller – FMC

- Flash accelerator for maximum efficiency
- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer and cache are provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor:
  - Power On Reset / Power Down Reset – POR/PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by an external signal, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to ±2 % accuracy at 3.3V operating voltage and 25°C operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Phase Lock Loop (PLL), a HSE clock monitor, clock prescalers, clock multiplexers, APB clock divider and gating circuitry. The AHB, APB and Cortex®-M0+ clocks are derived from the system clock (CK_SYS) which can come from the HSI, HSE or PLL. The Watchdog Timer and Real Time Clock (RTC) use the LSI as their clock source.

Power Management – PWRCU

- Single V_{DD} power supply: 2.0 V to 3.6 V
- Integrated 1.5 V LDO regulator for CPU core, peripherals and memories power supply
- Two power domains: V_{DD}, 1.5 V.
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in these devices provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down mode. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge, or both edge
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 8 external analog input channels

A 12-bit multi-channel ADC is integrated in the device. There are multiplexed channels, which include 8 external analog signal channels and 2 internal channels which can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset threshold levels. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

I/O Ports – GPIO

- Up to 23 GPIOs
- Port A, B are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have a configurable output driving current.

There are up to 23 General Purpose I/O pins, GPIO, named Port A and Port B for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

PWM Generation and Capture Timers – GPTM

- 16-bit up/down auto-reload counter
- 16-bit programmable prescaler allowing counter clock frequency division by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General Purpose Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation, or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

Single Channel Generation and Capture Timers – SCTM

- 16-bit up and auto-reload counter
- One channel for each timer
- 16-bit programmable prescaler allowing counter clock frequency division by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned
- Single Pulse Mode Output

The Single-Channel Timer consists of one 16-bit up-counter, one 16-bit Capture/Compare Register (CCR), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as single pulse generation or PWM output.

Basic Function Timer – BFTM

- 32-bit compare/match count-up counter – no I/O control features
- One shot mode – counting stops after a match condition
- Repetitive mode – restart counter after a match condition

The Basic Function Timer is a simple count-up 32-bit counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM operates in two functional modes, repetitive or one shot mode. In the repetitive mode the BFTM restarts the counter when a compare match event occurs. The BFTM also supports a one shot mode which forces the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit down counter with 3-bit prescaler
- Reset event for the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect system failures due to software malfunctions. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter when the counter value is greater than the WDT delta value. This means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. There is a register write protect function which can be enabled to prevent it from changing the Watchdog Timer configuration unexpectedly.

Inter-integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provide an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode with maskable address

The I²C is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: (1) 100 kHz in the Standard mode, (2) 400 kHz in the Fast mode and (3) 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I²C bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The I²C also has an arbitration detect function and clock synchronization to prevent situations where more than one master attempts to transmit data to the I²C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave mode
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave mode. The SPI interface uses 4 pins, which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Asynchronous operating baud rate up to (f_{PCLK}/16) MHz and synchronous operating rate up to (f_{PCLK}/8) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8, or 9-bit character
  - Parity: Even, odd, or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8-level for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous data transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes a transmitter FIFO, (TX_FIFO) and receiver FIFO (RX_FIFO). The software can detect a USART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate up to (f_{PCLK}/16) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8, or 9-bit character
  - Parity: Even, odd, or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watchpoints

Package and Operation Temperature

- 24/28-pin SSOP, 33-pin QFN package
- Operation temperature range: -40°C to +85°C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F52220	HT32F52230
Main Flash (KB)		16	31
Option Bytes Flash (KB)		1	1
SRAM (KB)		4	4
Timers	GPTM	1	
	SCTM	2	
	BFTM	1	
	WDT	1	
Communication	SPI	1	
	USART	1	
	UART	1	
	I²C	1	
EXTI		16	
12-bit ADC Number of channels		1	
		8 Channels	
GPIO		Up to 23	
CPU frequency		Up to 40 MHz	
Operating voltage		2.0 V ~ 3.6 V	
Operating temperature		-40°C ~ +85°C	
Package		24/28-pin SSOP, 33-pin QFN	

Block Diagram

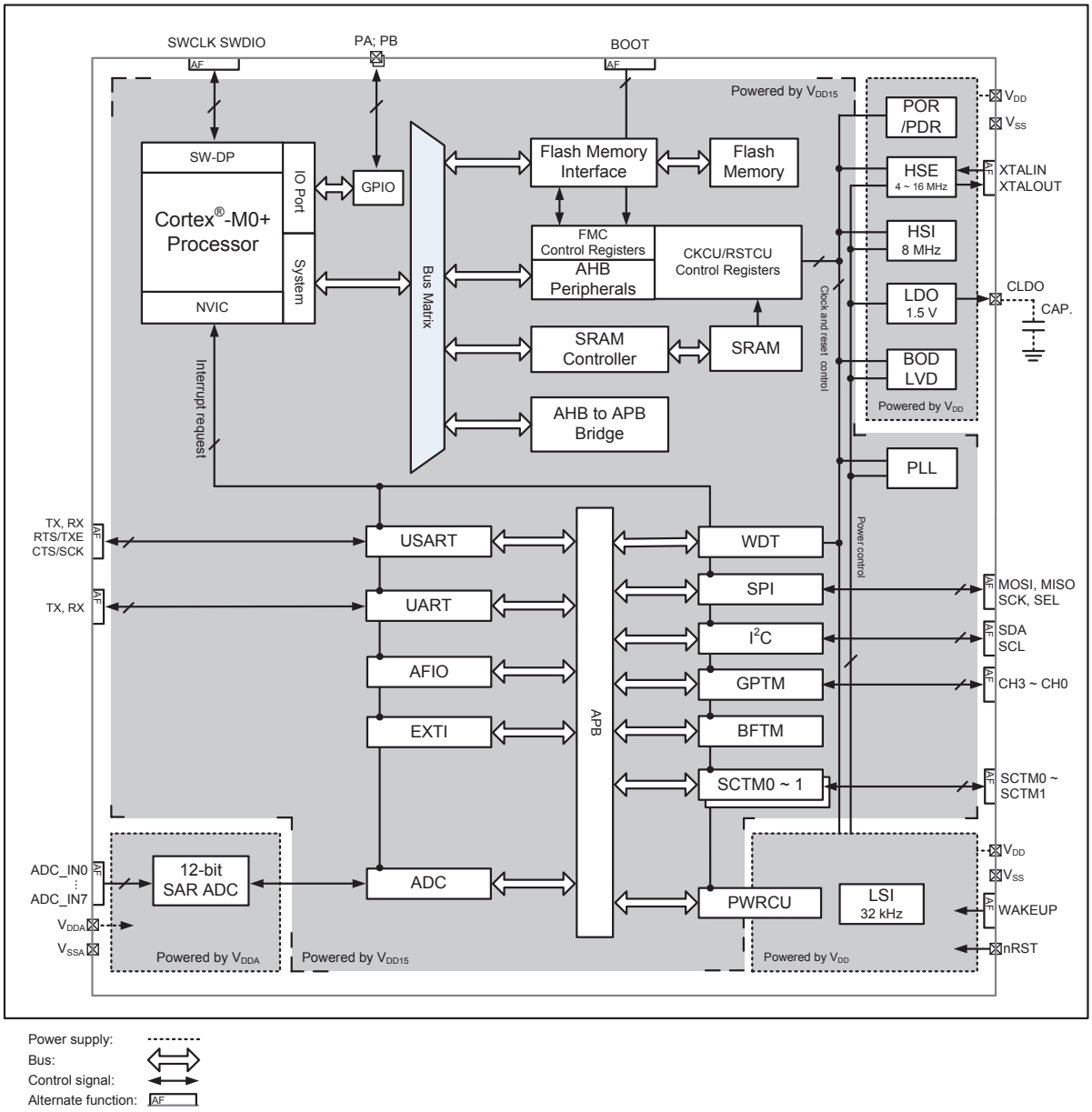


Figure 1. Block Diagram

Memory Map

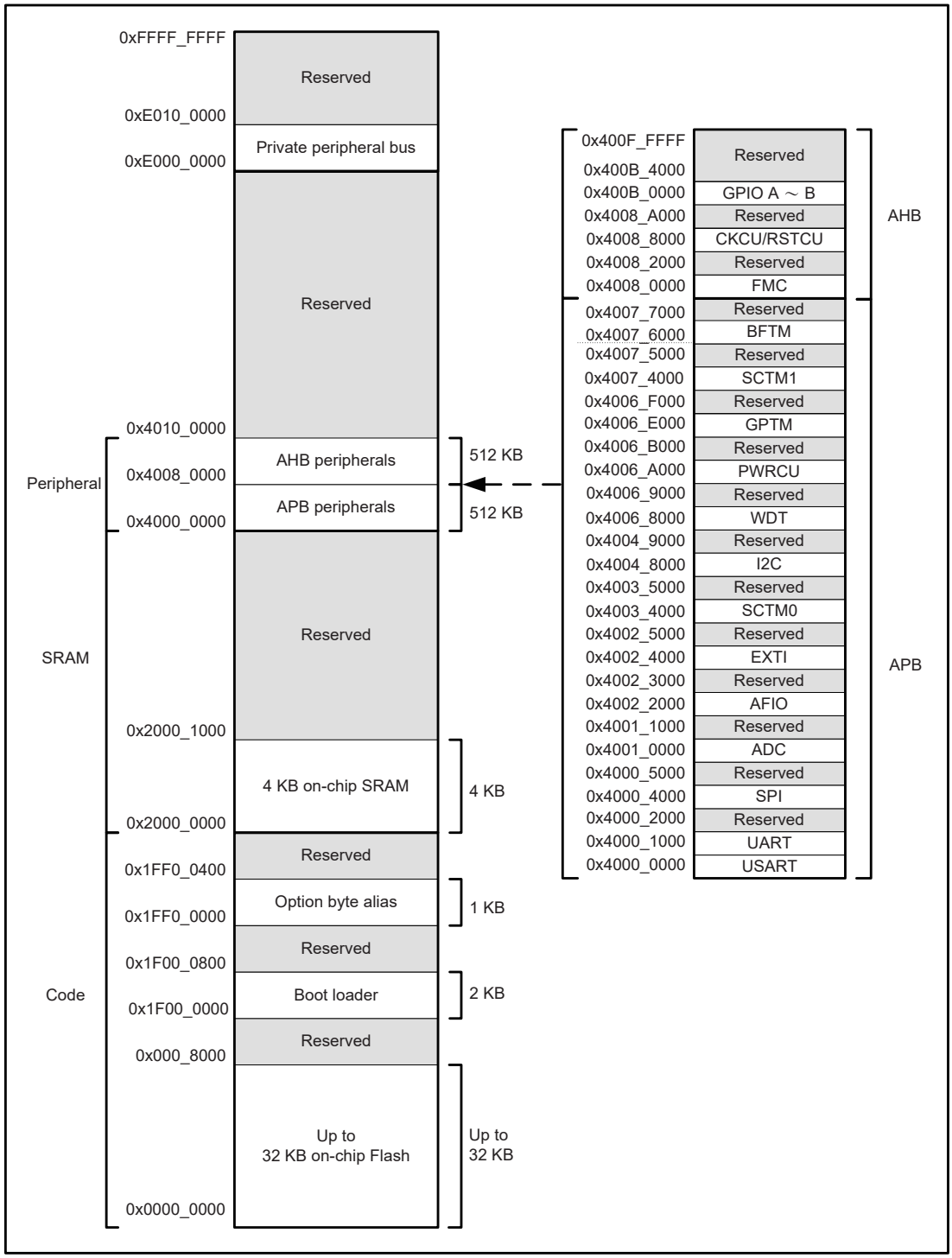


Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART	APB
0x4000_1000	0x4000_1FFF	UART	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI	
0x4000_5000	0x4001_9FFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C	
0x4004_9000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC/PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM	
0x4007_7000	0x4007_FFFF	Reserved	
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU/RSTCU	
0x4008_A000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIOA	
0x400B_2000	0x400B_3FFF	GPIOB	
0x400B_4000	0x400F_FFFF	Reserved	

Clock Structure

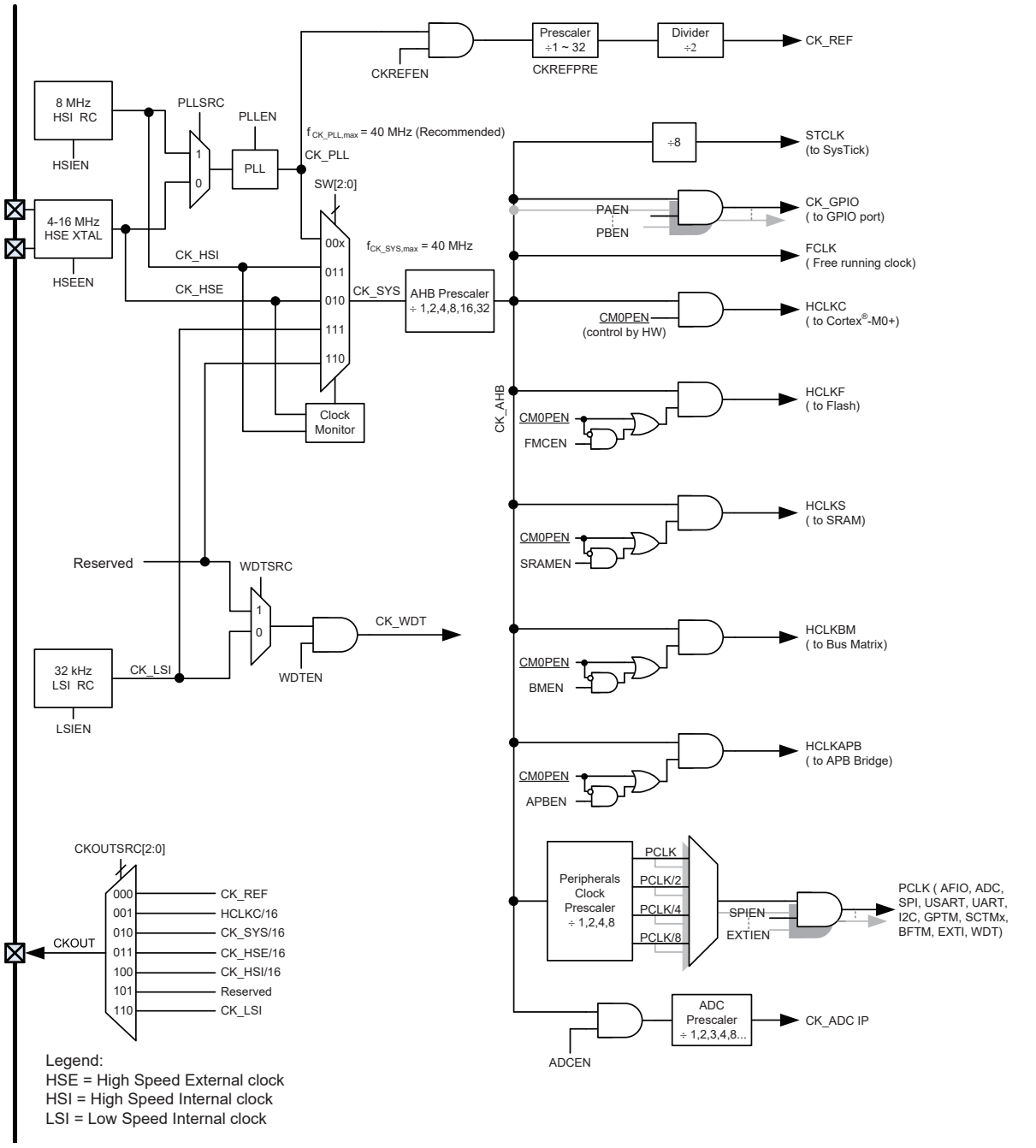


Figure 3. Clock Structure

4 Pin Assignment

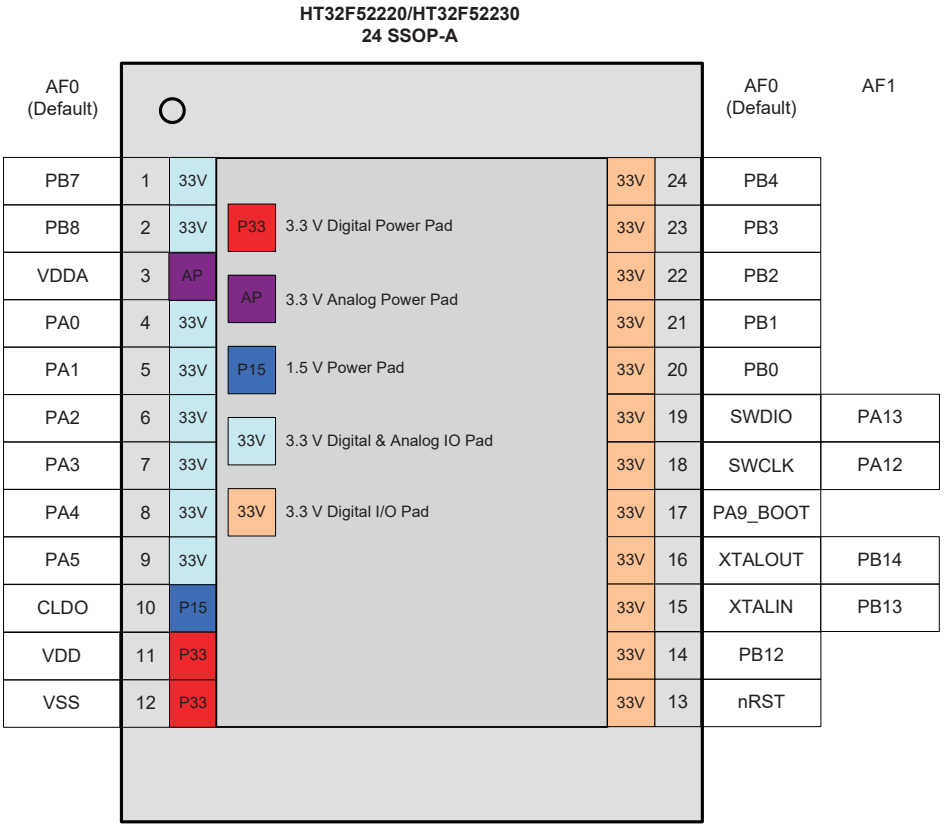


Figure 4. 24-pin SSOP Pin Assignment

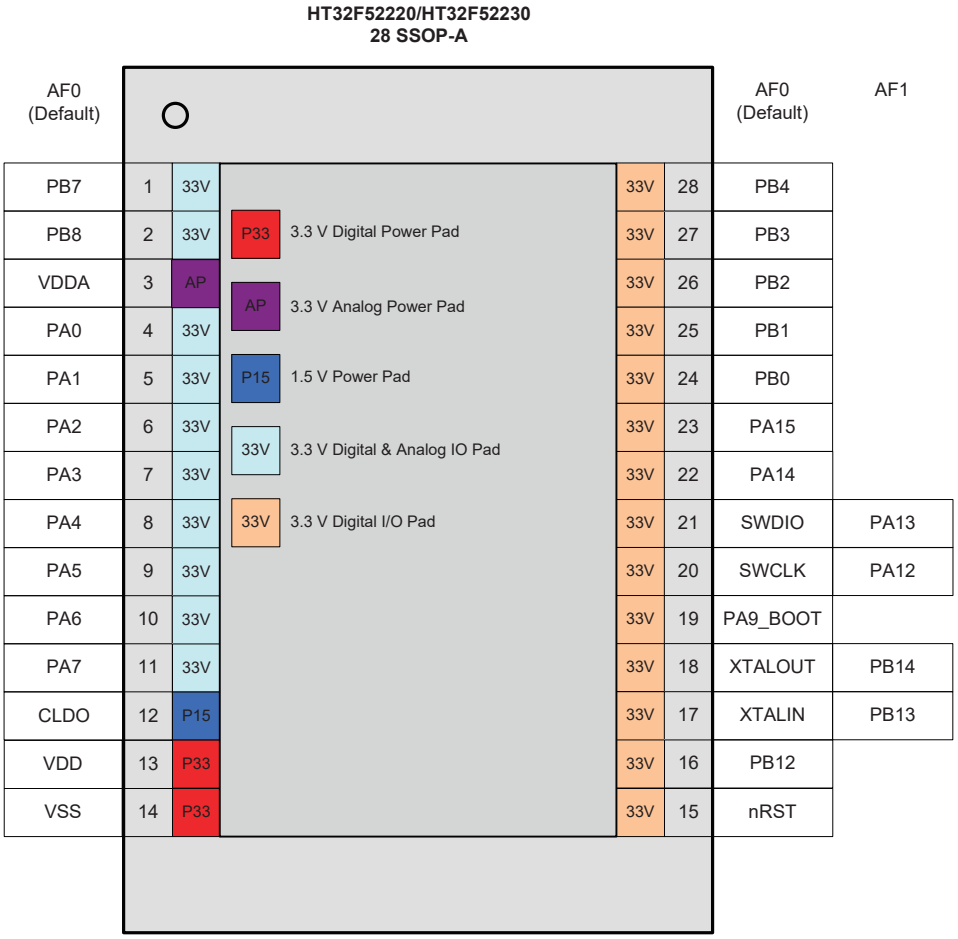


Figure 5. 28-pin SSOP Pin Assignment

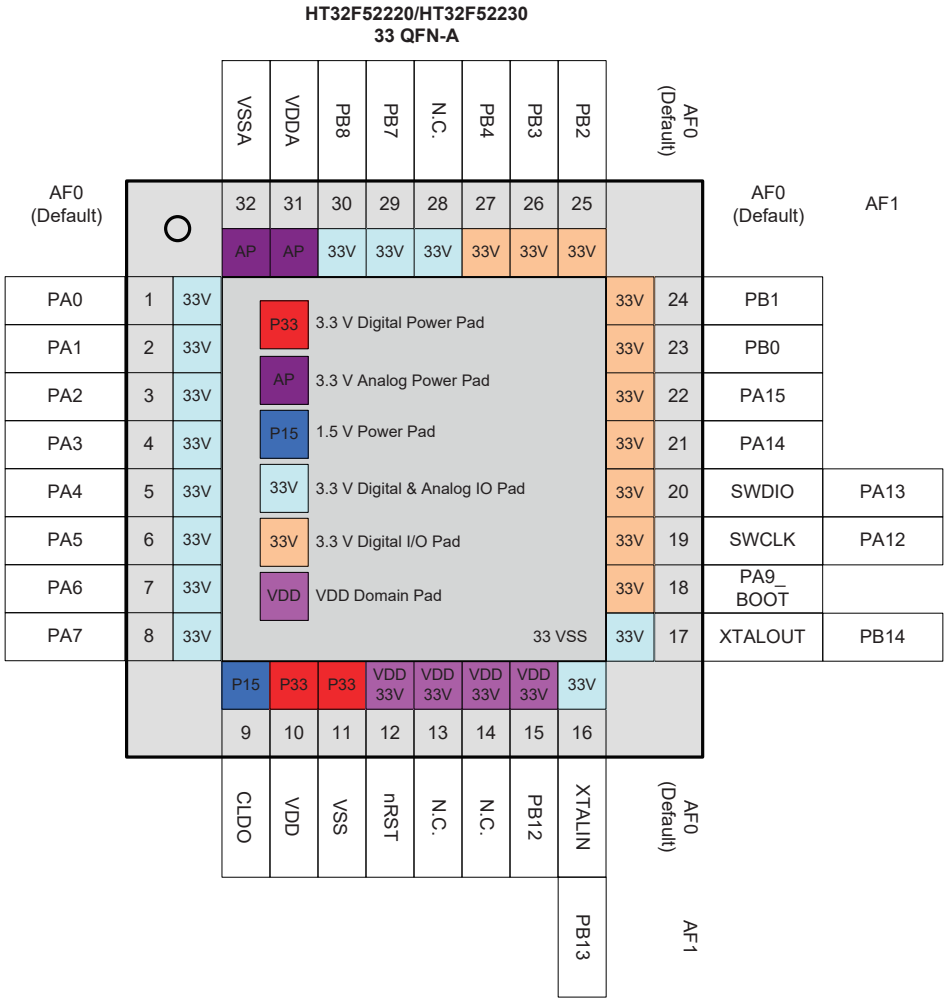


Figure 6. 33-pin QFN Pin Assignment

Table 3. Series Pin Assignment for 33-pin QFN, 24/28-pin SSOP Package

Package			Alternate Function Mapping															
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
33QFN	28SSOP	24SSOP	System Default	GPIO	ADC	N/A	GPTM	SPI	USART /UART	I2C	N/A	N/A	N/A	N/A	N/A	SCTM	N/A	System Other
1	4	4	PA0		ADC_IN0		GT_CH0	SPI_SCK	USR_ RTS	I2C_SCL								
2	5	5	PA1		ADC_IN1		GT_CH1	SPI_MOSI	USR_ CTS	I2C_SDA								
3	6	6	PA2		ADC_IN2		GT_CH2	SPI_MISO	USR_TX									
4	7	7	PA3		ADC_IN3		GT_CH3	SPI_SEL	USR_RX									
5	8	8	PA4		ADC_IN4		GT_CH0	SPI_SCK	UR_TX	I2C_SCL								
6	9	9	PA5		ADC_IN5		GT_CH1	SPI_MOSI	UR_RX	I2C_SDA								
7	10		PA6		ADC_IN6		GT_CH2	SPI_MISO										
8	11		PA7		ADC_IN7		GT_CH3	SPI_SEL										
9	12	10	CLDO															
10	13	11	VDD															
11	14	12	VSS															
12	15	13	nRST															
13			N.C.															
14			N.C.															
15	16	14	PB12					SPI_MISO	UR_RX							SCTM0		WAKEUP
16	17	15	XTALIN	PB13					UR_TX	I2C_SCL								
17	18	16	XTALOUT	PB14					UR_RX	I2C_SDA								
18	19	17	PA9_BOOT					SPI_MOSI								SCTM1		CKOUT
19	20	18	SWCLK	PA12														
20	21	19	SWDIO	PA13														
21	22		PA14				GT_CH0	SPI_SEL	USR_ RTS	I2C_SCL								
22	23		PA15				GT_CH0	SPI_SCK	USR_ CTS	I2C_SDA						SCTM1		
23	24	20	PB0				GT_CH1	SPI_MOSI	USR_TX	I2C_SCL								
24	25	21	PB1				GT_CH1	SPI_MISO	USR_RX	I2C_SDA						SCTM0		
25	26	22	PB2				GT_CH2	SPI_SEL	UR_TX									
26	27	23	PB3				GT_CH2	SPI_SCK	UR_RX							SCTM1		
27	28	24	PB4					SPI_MOSI	UR_TX							SCTM0		
28			N.C.															
29	1	1	PB7				GT_CH3	SPI_MISO	UR_TX	I2C_SCL								
30	2	2	PB8				GT_CH3	SPI_SEL	UR_RX	I2C_SDA								
31	3	3	VDDA															
32			VSSA															
33			VSS															

Table 4. Pin Description

Pin number			Pin Name	Type (Note1)	IO Structure (Note2)	Output Driving	Description
33QFN	28SSOP	24SSOP					Default function (AF0)
29	1	1	PB7	AI/O	33V	4/8/12/16 mA	PB7
30	2	2	PB8	AI/O	33V	4/8/12/16 mA	PB8
31	3	3	VDDA	P	—	—	Analog voltage for ADC
32			VSSA	P	—	—	Analog ground for ADC
33			VSS	P			Ground reference for digital I/O
1	4	4	PA0	AI/O	33V	4/8/12/16 mA	PA0
2	5	5	PA1	AI/O	33V	4/8/12/16 mA	PA1
3	6	6	PA2	AI/O	33V	4/8/12/16 mA	PA2
4	7	7	PA3	AI/O	33V	4/8/12/16 mA	PA3
5	8	8	PA4	AI/O	33V	4/8/12/16 mA	PA4
6	9	9	PA5	AI/O	33V	4/8/12/16 mA	PA5
7	10		PA6	AI/O	33V	4/8/12/16 mA	PA6
8	11		PA7	AI/O	33V	4/8/12/16 mA	PA7
9	12	10	CLDO	P	—	—	Core power LDO 1.5 V output It must be connected a 1 μF to 2.2 μF capacitor as close as possible between this pin and VSS pin.
10	13	11	VDD	P	—	—	Voltage for digital I/O
11	14	12	VSS	P	—	—	Ground reference for digital I/O
12	15	13	nRST Note 3	I (V_{DD})	33V_PU	—	External reset pin and external wakeup pin in the Power-Down mode
13			N.C.	—	—	—	—
14			N.C.	—	—	—	—
15	16	14	PB12 Note 3	I/O (V_{DD})	33V	4/8/12/16 mA	PB12
16	17	15	PB13	AI/O	33V	4/8/12/16 mA	XTALIN
17	18	16	PB14	AI/O	33V	4/8/12/16 mA	XTALOUT
18	19	17	PA9	I/O	33V_PU	4/8/12/16 mA	PA9_BOOT
19	20	18	PA12	I/O	33V_PU	4/8/12/16 mA	SWCLK
20	21	19	PA13	I/O	33V_PU	4/8/12/16 mA	SWDIO
21	22		PA14	I/O	33V	4/8/12/16 mA	PA14
22	23		PA15	I/O	33V	4/8/12/16 mA	PA15
23	24	20	PB0	I/O	33V	4/8/12/16 mA	PB0
24	25	21	PB1	I/O	33V	4/8/12/16 mA	PB1
25	26	22	PB2	I/O	33V	4/8/12/16 mA	PB2
26	27	23	PB3	I/O	33V	4/8/12/16 mA	PB3
27	28	24	PB4	I/O	33V	4/8/12/16 mA	PB4
28			N.C.	—	—	—	—

Note: 1. I = input, O = output, A = Analog port, P = power supply, PU = pull-up, V_{DD} = V_{DD} Power
2. 33V = 3.3 V tolerant.
3. These pins are located at the V_{DD} power domain.

5 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	External Main Supply Voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External Analog Supply Voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{IN}	Input Voltage On I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Ambient Operating Temperature Range	-40	+85	°C
T_{STG}	Storage Temperature Range	-55	+150	°C
T_J	Maximum Junction Temperature	—	125	°C
P_D	Total Power Dissipation	—	500	mW
V_{ESD}	Electrostatic Discharge Voltage – Human Body Mode	-4000	+4000	V

Recommended DC Operating Conditions

Table 6. Recommended DC Operating Conditions

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	I/O OPerating Voltage	—	2.0	3.3	3.6	V
V_{DDA}	Analog Operating Voltage	—	2.5	3.3	3.6	V

On-Chip LDO Voltage Regulator Characteristics

Table 7. LDO Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 2.0 V Regulator input @ I_{LDO} = 35 mA and voltage variant = ±5 %, After trimming.	1.425	1.5	1.57	V
I_{LDO}	Output Current	V_{DD} = 2.0 V Regulator input @ V_{LDO} = 1.5 V	—	30	35	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	—	1	—	µF

Power Consumption

Table 8. Power Consumption Characteristics

Symbol	Parameter	Conditions	Typ	Max		Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	
I_{DD}	Supply Current (Run Mode)	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f_{CPU} = 40 MHz, f_{BUS} = 40 MHz, All peripherals enabled	9.3	10.6	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f_{CPU} = 40 MHz, f_{BUS} = 40 MHz, All peripherals disabled	6.0	6.8	—	mA
		V_{DD} = 3.3 V, HSI off, PLL off, LSI on, f_{CPU} = 32 kHz, f_{BUS} = 32 kHz, All peripherals enabled	39	52	—	µA
		V_{DD} = 3.3 V, HSI off, PLL off, LSI on, f_{CPU} = 32 kHz, f_{BUS} = 32 kHz, All peripherals disabled	36	48	—	µA
	Supply Current (Sleep Mode)	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f_{CPU} = 0 MHz, f_{BUS} = 40 MHz, All peripherals enabled	4.9	5.6	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f_{CPU} = 0 MHz, f_{BUS} = 40 MHz, All peripherals disabled	1.0	1.15	—	mA
	Supply Current (Deep-Sleep1 Mode)	V_{DD} = 3.3 V, All clock off (HSE/HSI/PLL), LDO in low power mode, LSI on	32.0	49.0	—	µA
	Supply Current (Deep-Sleep2 Mode)	V_{DD} = 3.3 V, All clock off (HSE/HSI/PLL), LDO off DMOS on, LSI on	3.1	4.7	—	µA
	Supply Current (Power-Down Mode)	V_{DD} = 3.3 V, LDO off, DMOS off, LSI on	1.3	2.0	—	µA

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSI means 32 kHz low speed internal oscillator.
3. Code = while (1) { 208 NOP } executed in Flash.
4. f_{BUS} means f_{HCLK} and f_{PCLK}.

Reset and Supply Monitor Characteristics

Table 9. V_{DD} Power Reset Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{POR}	Power on reset threshold (Rising Voltage on V_{DD})	T_A = -40°C ~ +85°C	1.66	1.79	1.90	V
V_{PDR}	Power down reset threshold (Falling Voltage on V_{DD})		1.49	1.64	1.78	V
$V_{PORHYST}$	POR hysteresis	—	—	150	—	mV
t_{POR}	Reset delay time	V_{DD} = 3.3 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.
3. If the LDO is turned on, the VDD POR has to be in the de-assertion condition. When the VDD POR is in the assertion state then the LDO will be turned off.

Table 10. LVD/BOD Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BOD}	Voltage of Brown Out Detection	T_A = -40°C ~ 85°C After factory-trimmed (V_{DD} Falling edge)		2.02	2.1	2.18	V
V_{LVD}	Voltage of Low Voltage Detection	T_A = -40°C ~ 85°C (V_{DD} Falling edge)	LVDS = 000	2.17	2.25	2.33	V
			LVDS = 001	2.32	2.4	2.48	V
			LVDS = 010	2.47	2.55	2.63	V
			LVDS = 011	2.62	2.7	2.78	V
			LVDS = 100	2.77	2.85	2.93	V
			LVDS = 101	2.92	3.0	3.08	V
			LVDS = 110	3.07	3.15	3.23	V
			LVDS = 111	3.22	3.3	3.38	V
$V_{LVDHTST}$	Lvd Hysteresis	V_{DD} = 3.3 V	—	—	100	—	mV
t_{suLVD}	Lvd Setup Time	V_{DD} = 3.3 V	—	—	—	5	μs
t_{atLVD}	Lvd Active Delay Time	V_{DD} = 3.3 V	—	—	—	—	μs
I_{DDLVD}	Operation Current Note3	V_{DD} = 3.3 V	—	—	5	15	μA

Note: 1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.
3. Bandgap current is not included.
4. LVDS field is in the PWRCU LVDCSR register

External Clock Characteristics

Table 11. High Speed External Clock (HSE) Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operation Range	—	2.0	—	3.6	V
f_{HSE}	High Speed External Oscillator Frequency (HSE)	—	4	—	16	MHz
C_{LHSE}	Load Capacitance	V_{DD} = 3.3 V, R_{ESR} = 100 Ω @ 16 MHz	—	—	22	pF
R_{FHSE}	Internal Feedback Resistor Between XTALIN and XTALOUT pins	—	—	1	—	MΩ
R_{ESR}	Equivalent Series Resistance*	V_{DD} = 3.3 V, C_L = 12 pF @ 16 MHz, HSEDR = 0	—	—	160	Ω
		V_{DD} = 2.4 V, C_L = 12 pF @ 16 MHz, HSEDR = 1				
D_{HSE}	Hse Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	Hse Oscillator Current Consumption	V_{DD} = 3.3 V @ 16 MHz	—	TBD	—	mA
I_{PWDHSE}	Hse Oscillator Power Down Current	V_{DD} = 3.3 V	—	—	0.01	μA
t_{SUHSE}	Hse Oscillator STartup Time	V_{DD} = 3.3 V	—	—	4	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE clock in the PCB layout:

- The crystal oscillator should be located as close as possible to the MCU to keep the trace lengths as short as possible to reduce any parasitic capacitance.
- Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
- Keep any high frequency signal lines away from the crystal area to prevent any crosstalk adverse effects.

Internal Clock Characteristics

Table 12. High Speed Internal Clock (HSI) Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operation Range	—	2.0	—	3.6	V
f_{HSI}	Hsi Frequency	V_{DD} = 3.3 V @ 25°C	—	8	—	MHz
ACC_{HSI}	Factory Calibrated Hsi Oscillator FRequency Accuracy	V_{DD} = 3.3 V, T_A = 25°C	-2	—	2	%
		V_{DD} = 2.5 V ~ 3.6 V, T_A = -40°C ~ +85°C	-3	—	3	%
		V_{DD} = 2.0 V ~ 3.6 V T_A = -40°C ~ +85°C	-4	—	4	%
Duty	Duty Cycle	f_{HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	Oscillator Supply Current	f_{HSI} = 8 MHz	—	300	500	μA
	Power Down Current		—	—	0.05	μA
t_{suHSI}	Startup Time	f_{HSI} = 8 MHz	-—	—	10	μs

Table 13. Low Speed Internal Clock (LSI) Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Low Speed Internal Oscillator Frequency (LSI)	V_{DD} = 3.3 V, T_A = -40°C ~ +85°C	21	32	43	kHz
ACC_{LSI}	Lsi Frequency Accuracy	After factory-trimmed, V_{DD} = 3.3 V, T_A = 25°C	-10	—	+10	%
I_{DDLSI}	Lsi Oscillator Operating Current	V_{DD} = 3.3 V, T_A = 25°C	—	0.4	0.8	μA
t_{SULSI}	Lsi Oscillator STartup Time	V_{DD} = 3.3 V, T_A = 25°C	—	—	100	μs

PLL Characteristics

Table 14. PLL Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock	—	4	—	16	MHz
f_{CK_PLL}	PLL output clock	—	16	—	48	MHz
t_{LOCK}	PLL lock time	—	—	200	—	μs

Memory Characteristics

Table 15. Flash Memory Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{ENDU}	Number of guaranteed program/erase cycles before failure. (Endurance)	T_A = -40°C ~ +85°C	10	—	—	K cycles
t_{RET}	Data retention time	T_A = -40°C ~ +85°C	10	—	—	Years
t_{PROG}	Word programming time	T_A = -40°C ~ +85°C	20	—	—	μs
t_{ERASE}	Page erase time	T_A = -40°C ~ +85°C	2	—	—	ms
t_{MERASE}	Mass erase time	T_A = -40°C ~ +85°C	10	—	—	ms

I/O Port Characteristics

Table 16. I/O Port Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{IL}	Low Level Input Current	3.3 V IO	$V_I = V_{SS}$, On-chip pull-up resister disabled.	—	—	3	μA
		Reset pin		—	—	3	μA
I_{IH}	High Level Input Current	3.3 V IO	$V_I = V_{DD}$, On-chip pull-down resister disabled.	—	—	3	μA
		Reset pin		—	—	3	μA
V_{IL}	Low Level Input Voltage	3.3 V IO		- 0.5	—	V_{DD} × 0.35	V
		Reset pin		- 0.5	—	V_{DD} × 0.35	V
V_{IH}	High Level Input Voltage	3.3 V IO		V_{DD} × 0.65	—	V_{DD} + 0.5	V
		Reset pin		V_{DD} × 0.65	—	V_{DD} + 0.5	V
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	3.3 V IO		—	0.12 × V_{DD}	—	mV
		Reset pin		—	0.12 × V_{DD}	—	mV
I_{OL}	Low Level Output Current (GPIO Sink current)	3.3 V IO 4 mA drive, V_{OL} = 0.4 V		4	—	—	mA
		3.3 V IO 8 mA drive, V_{OL} = 0.4 V		8	—	—	mA
		3.3 V IO 12 mA drive, V_{OL} = 0.4 V		12	—	—	mA
		3.3 V IO 16 mA drive, V_{OL} = 0.4 V		16	—	—	mA
I_{OH}	High Level Output Current (GPIO Source current)	3.3 V I/O 4 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		4	—	—	mA
		3.3 V I/O 8 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		8	—	—	mA
		3.3 V I/O 12 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		12	—	—	mA
		3.3 V I/O 16 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		16	—	—	mA
V_{OL}	Low Level Output Voltage	3.3 V 4 mA drive IO, I_{OL} = 4 mA		—	—	0.4	V
		3.3 V 8 mA drive IO, I_{OL} = 8 mA		—	—	0.4	V
		3.3 V 12 mA drive IO, I_{OL} = 12 mA		—	—	0.4	V
		3.3 V 16 mA drive IO, I_{OL} = 16 mA		—	—	0.4	V
V_{OH}	High Level Output Voltage	3.3 V 4 mA drive IO, I_{OH} = 4 mA		V_{DD} - 0.4	—	—	V
		3.3 V 8 mA drive IO, I_{OH} = 8 mA		V_{DD} - 0.4	—	—	V
		3.3 V 12 mA drive IO, I_{OH} = 12 mA		V_{DD} - 0.4	—	—	V
		3.3 V 16 mA drive IO, I_{OH} = 16 mA		V_{DD} - 0.4	—	—	V
R_{PU}	Internal Pull-up Resistor	3.3 V I/O		—	46	—	kΩ
R_{PD}	Internal Pull-down Resistor	3.3 V I/O		—	46	—	kΩ

ADC Characteristics

Table 17. ADC Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating Voltage	—	2.5	3.3	3.6	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference Voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	Current Consumption	V_{DDA} = 3.3 V	—	1	TBD	mA
I_{ADC_DN}	Power Down Current Consumption	V_{DDA} = 3.3 V	—	—	0.1	μA
f_{ADC}	A/D Converter Clock	—	0.7	—	16	MHz
f_S	Sampling Rate	—	0.05	—	1	MHz
t_{DL}	Data Latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	—	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin/pad capacitance included	—	16	—	pF
t_{SU}	Startup Time	—	—	—	1	μs
N	Resolution	—	—	12	—	bits
INL	Integral Non-Linearity Error	f_S = 750 kHz, V_{DDA} = 3.3 V	—	±2	±5	LSB
DNL	Differential Non-Linearity Error	f_S = 750 kHz, V_{DDA} = 3.3 V	—	±1	—	LSB
E_O	Offset Error	—	—	—	±10	LSB
E_G	Gain Error	—	—	—	±10	LSB

Note: 1. Guaranteed by design, not tested in production.

2. Due to the A/D Converter input channel and GPIO pin-shared function design limitation, the V_{DDA} supply power of the A/D Converter has to be equal to the V_{DD} supply power of the MCU in the application circuit.

3. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

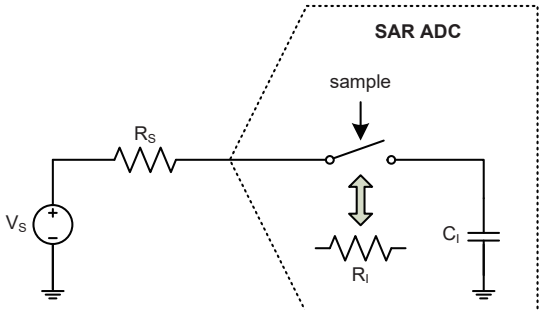


Figure 7. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0V and V_{REF}) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

SCTM/GPTM Characteristics

Table 18. SCTM/GPTM Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TM}	Timer clock source for GPTM	—	—	—	48	MHz
t_{RES}	Timer resolution time	—	—	—	—	f_{TM}
f_{EXT}	External signal frequency on channel 1 ~ 4	—	—	—	1/2	f_{TM}
RES	Timer resolution	—	—	—	16	bits

I²C Characteristics

Table 19. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Scl Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	Scl Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	Scl Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	Scl And Sda Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	Scl And Sda Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	Sda Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA data hold time (Note 5)	0	—	0	—	0	—	ns
	SDA data hold time (Note 6)	100	—	100	—	100	—	ns
$t_{VD(SDA)}$	SDA data valid time	—	1.6	—	0.475	—	0.25	μs
$t_{SU(STA)}$	Start Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	Start Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	Stop Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Guaranteed by design, not tested in production.
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast mode plus, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: COMB_FILTER_En = 0 and SEQ_FILTER = 00.
6. The above characteristic parameters of the I²C bus timing are based on: COMB_FILTER_En = 1 and SEQ_FILTER = 00.

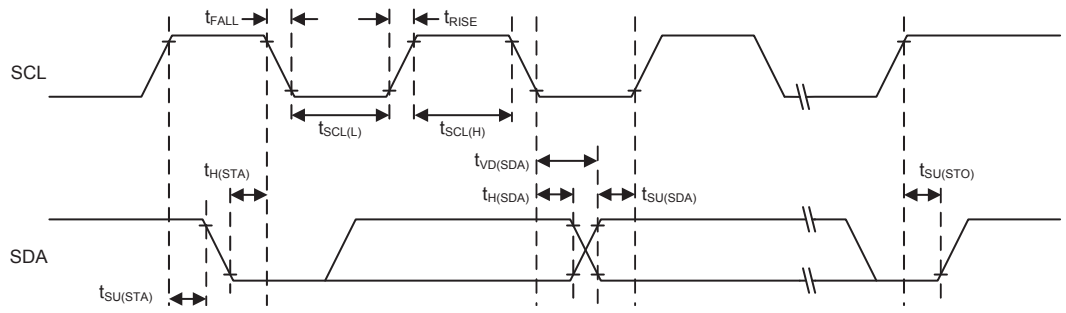


Figure 8. I²C Timing Diagrams

SPI Characteristics

Table 20. SPI Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI Master mode						
f_{SCK}	SPI master output SCK clock frequency	SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK clock high and low time	—	$t_{SCK}/2$ - 2	—	$t_{SCK}/2$ + 1	ns
$t_{V(MO)}$	Data output valid time	—	-	—	5	ns
$t_{H(MO)}$	Data output hold time	—	2	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	5	—	—	ns
$t_{H(MI)}$	Data input hold time	—	5	—	—	ns
SPI Slave mode						
f_{SCK}	SPI slave input SCK clock frequency	SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI slave input SCK clock duty cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL enable setup time	—	3 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL enable hold time	—	2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data output disable time	—	—	—	10	ns
$t_{V(SO)}$	Data output valid time	—	—	—	25	ns
$t_{H(SO)}$	Data output hold time	—	15	—	—	ns
$t_{SU(SI)}$	Data input setup time	—	5	—	—	ns
$t_{H(SI)}$	Data input hold time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

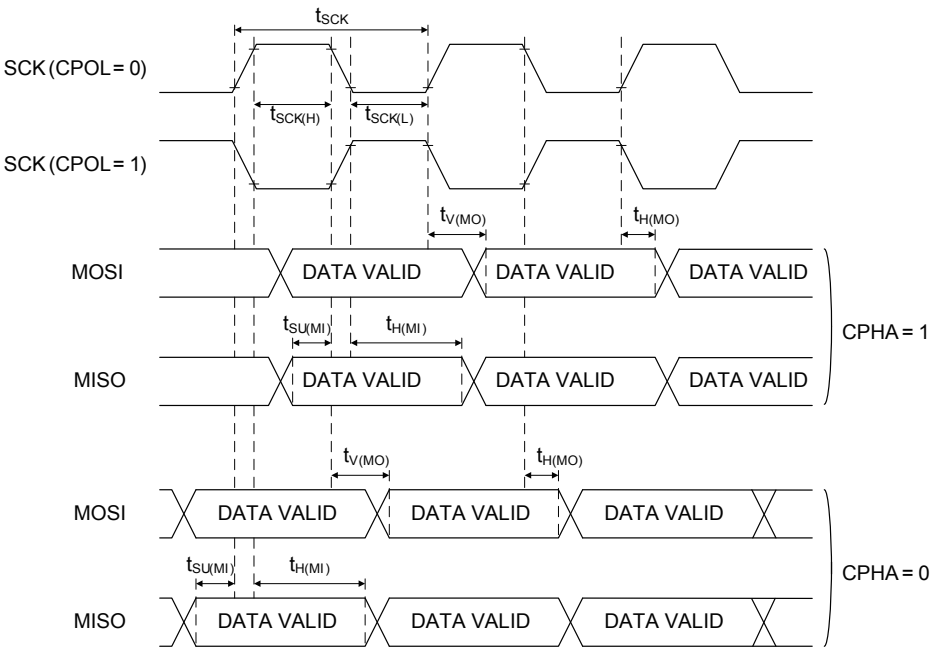


Figure 9. SPI Timing Diagrams – SPI Master Mode

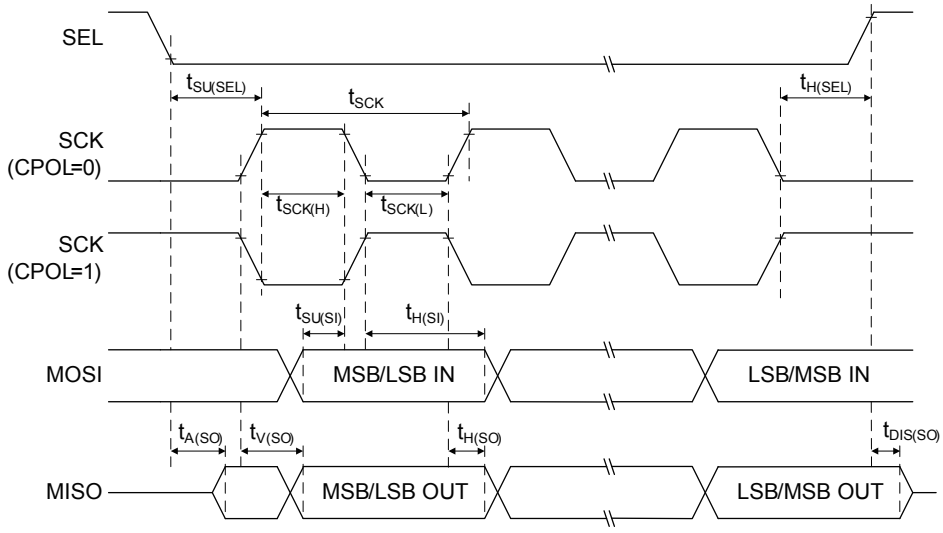


Figure 10. SPI Timing Diagrams – SPI Slave Mode with CPHA=1

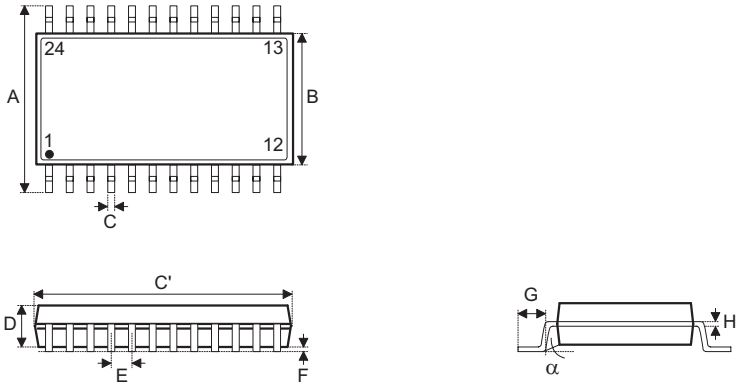
6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

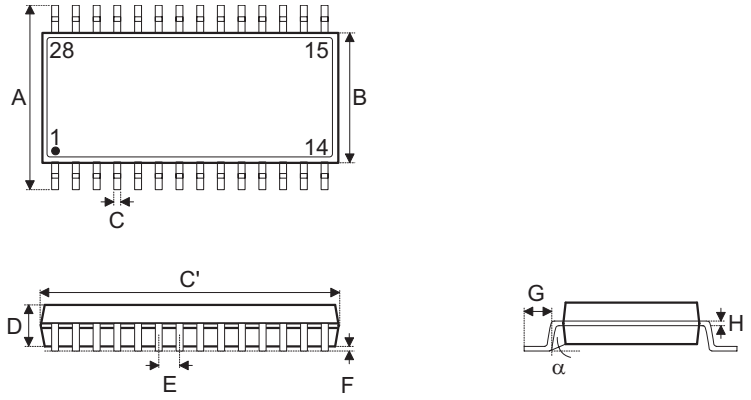
24-pin SSOP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.008	—	0.012
C’	—	0.341 BSC	—
D	—	—	0.069
E	—	0.025 BSC	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.000 BSC	—
B	—	3.900 BSC	—
C	0.200	—	0.300
C’	—	8.660 BSC	—
D	—	—	1.750
E	—	0.635 BSC	—
F	0.100	—	0.250
G	0.410	—	1.270
H	0.100	—	0.250
α	0°	—	8°

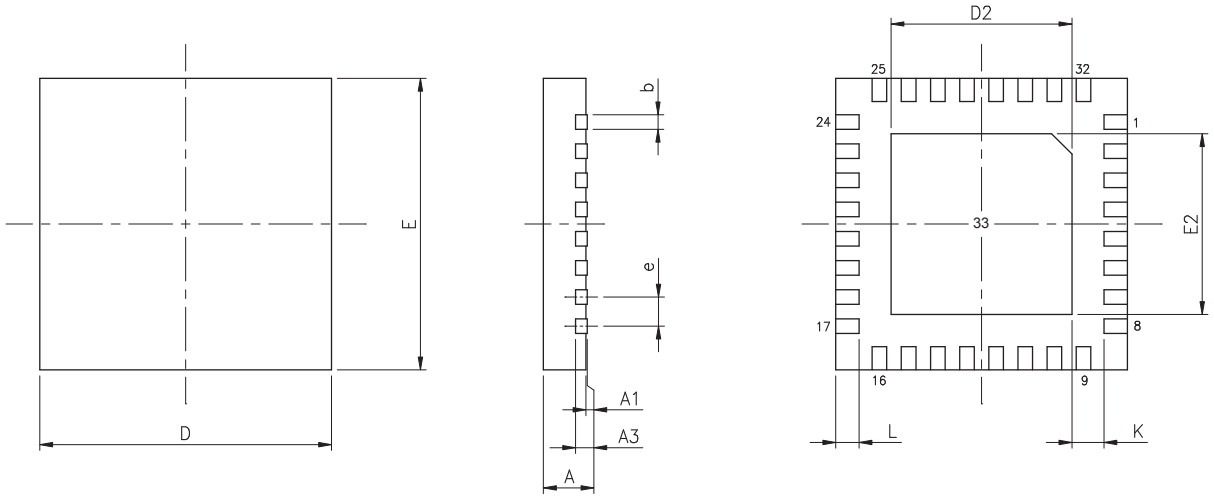
28-pin SSOP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.008	—	0.012
C’	—	0.390 BSC	—
D	—	—	0.069
E	—	0.025 BSC	—
F	0.004	—	0.0098
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.000 BSC	—
B	—	3.900 BSC	—
C	0.200	—	0.300
C’	—	9.900 BSC	—
D	—	—	1.750
E	—	0.635 BSC	—
F	0.100	—	0.250
G	0.410	—	1.270
H	0.100	—	0.250
α	0°	—	8°

SAW Type 33-pin (4mm×4mm) QFN Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.006	0.008	0.010
D	—	0.157 BSC	—
E	—	0.157 BSC	—
e	—	0.016 BSC	—
D2	0.104	0.106	0.108
E2	0.104	0.106	0.108
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A3	—	0.203 BSC	—
b	0.150	0.200	0.250
D	—	4.000 BSC	—
E	—	4.000 BSC	—
e	—	0.400 BSC	—
D2	2.650	2.700	2.750
E2	2.650	2.700	2.750
L	0.350	0.400	0.450
K	0.200	—	—