Feature

- Logic Operating Voltage: 2.4V~5.5V
- Integrated oscillator circuitry
- Bias: 1/2 or 1/3; Duty: 1/4
- Internal LCD bias generation with voltage-follower buffers
- External V_{LCD} pin to supply LCD operating voltage
- Support I^2C-bus serial interface
- Selectable LCD Frame Frequencies
- Up to 36×4 bits RAM for display data storage
- Maximum Display patterns:
  36×4 patterns - 36 segments and 4 commons
- Versatile blinking modes: off, 0.5Hz, 1Hz, 2Hz
- Write address auto-increment
- Support Power Save Mode for low power consumption
- Manufactured in silicon gate CMOS process
- Package Types: 48-pin TSSOP/LQFP and Chip

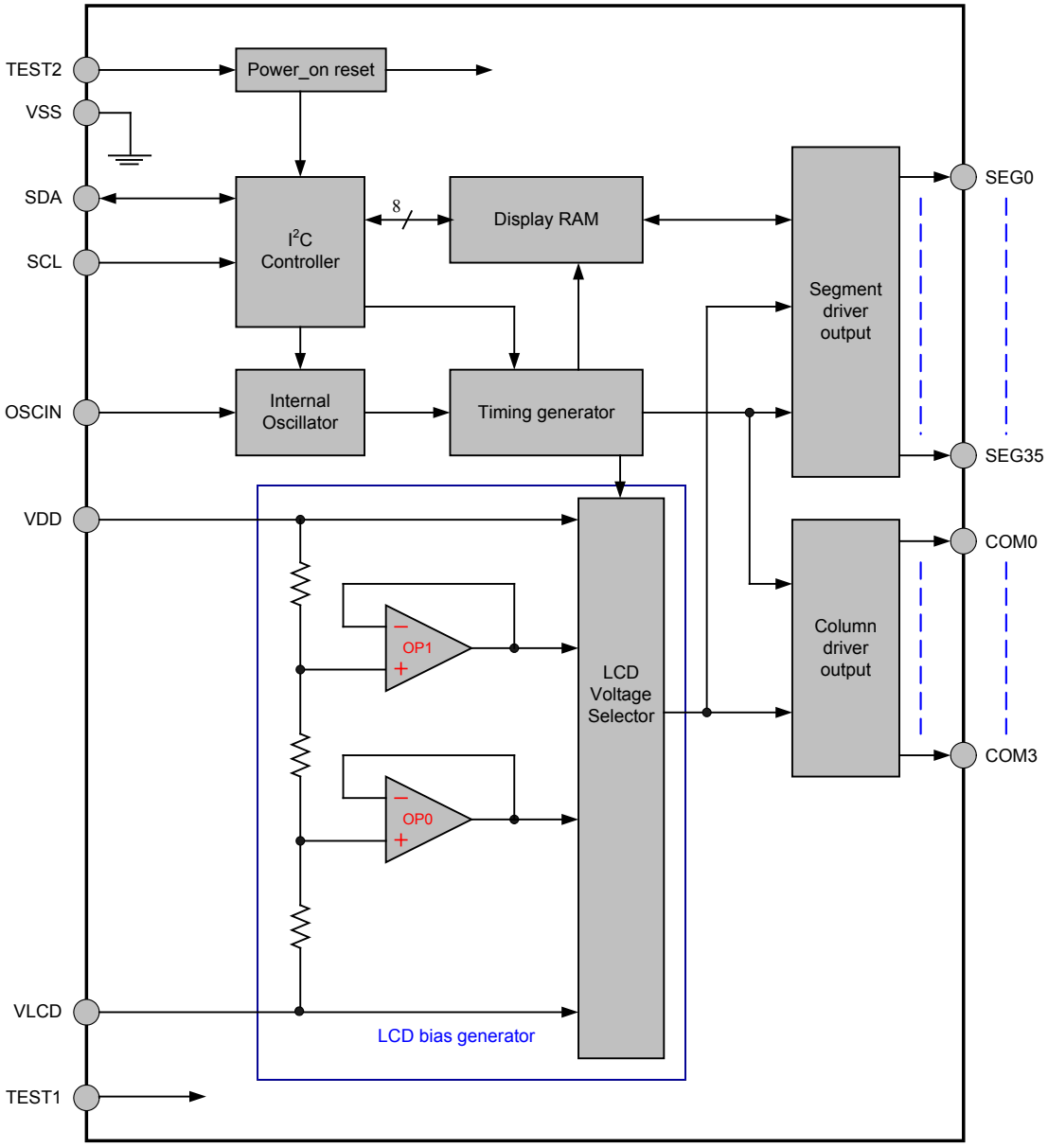
Applications

- Leisure products
- Games
- Telephone display
- Audio Combo display
- Video Player display
- Kitchen Appliance display
- Measurement equipment display
- Household appliance
- Consumer electronics

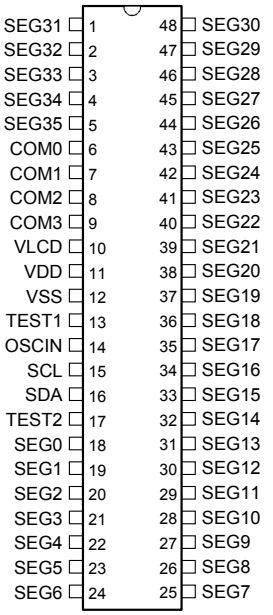
General Description

The HT9B92 device is a memory mapping and multi-function LCD controller driver. The maximum display segments of the device are 144 patterns (36 segments and 4 commons) display. The software configuration feature of the HT9B92 device makes it suitable for multiple LCD applications including LCD modules and display subsystems. The HT9B92 device communicates with most microprocessors/ microcontrollers via a two-wire bidirectional I^2C-bus interface.

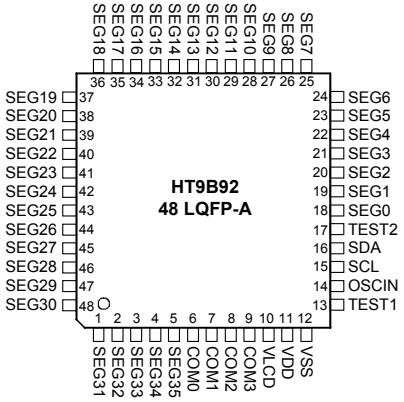
Block Diagram



Pin Assignment

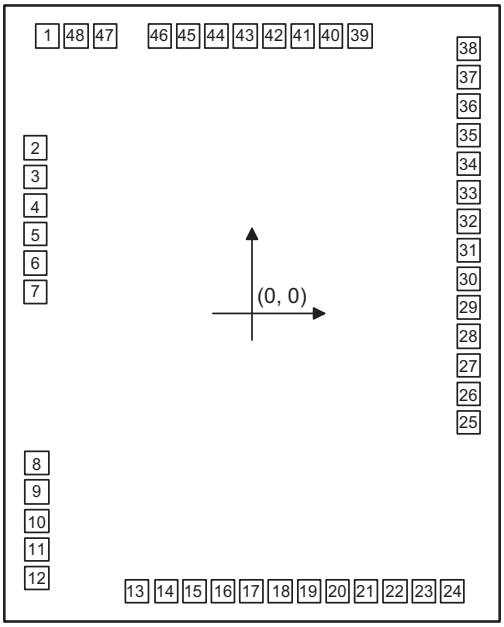


HT9B92
48 TSSOP-A



HT9B92
48 LQFP-A

Pad Assignment for COB



Chip size: 1484 × 1836um^2

Note : The IC substrate should be connected to VSS in the PCB layout artwork

Pad Coordinates for COB

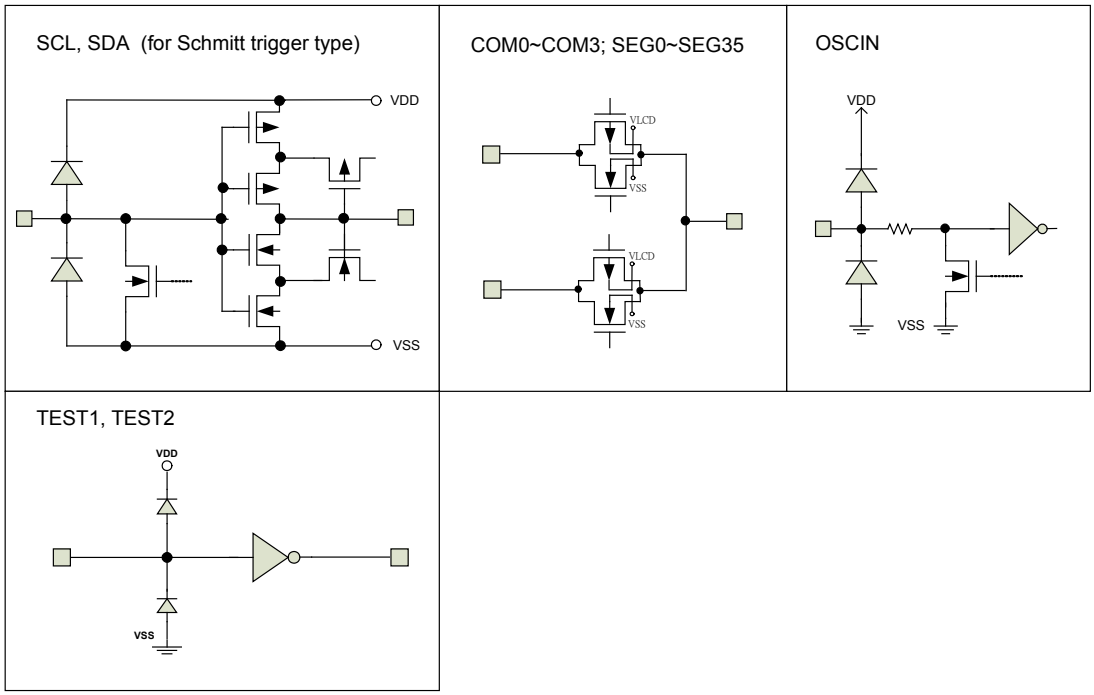
unit: μm

No	Pad Name	X	Y	No	Pad Name	X	Y
1	COM0	-606.600	819.900	25	SEG12	643.900	-322.400
2	COM1	-643.900	489.399	26	SEG13	643.900	-237.400
3	COM2	-643.900	404.399	27	SEG14	643.900	-152.400
4	COM3	-643.900	319.399	28	SEG15	643.900	-67.400
5	VLCD	-643.900	234.399	29	SEG16	643.900	17.600
6	VDD	-643.900	149.399	30	SEG17	643.900	102.600
7	VSS	-643.900	64.399	31	SEG18	643.900	187.600
8	TEST1	-638.400	-442.600	32	SEG19	643.900	272.600
9	OSCIN	-638.400	-527.600	33	SEG20	643.900	357.600
10	SCL	-638.400	-612.600	34	SEG21	643.900	442.600
11	SDA	-638.400	-697.600	35	SEG22	643.900	527.600
12	TEST2	-638.400	-782.600	36	SEG23	643.900	612.600
13	SEG0	-340.350	-819.900	37	SEG24	643.900	697.600
14	SEG1	-255.350	-819.900	38	SEG25	643.900	782.600
15	SEG2	-170.350	-819.900	39	SEG26	320.799	819.900
16	SEG3	-85.350	-819.900	40	SEG27	235.799	819.900
17	SEG4	-0.350	-819.900	41	SEG28	150.799	819.900
18	SEG5	84.650	-819.900	42	SEG29	65.799	819.900
19	SEG6	169.650	-819.900	43	SEG30	-19.201	819.900
20	SEG7	254.650	-819.900	44	SEG31	-104.201	819.900
21	SEG8	339.650	-819.900	45	SEG32	-189.201	819.900
22	SEG9	424.650	-819.900	46	SEG33	-274.201	819.900
23	SEG10	509.650	-819.900	47	SEG34	-436.600	819.900
24	SEG11	594.650	-819.900	48	SEG35	-521.600	819.900

Pad Description

Pin Name	Type	Description
SDA	I/O	Serial Data Input/Output pin Serial Data (SDA) Input/Output for 2-wire I^2C interface is an NMOS open drain structure
SCL	I	Serial Clock Input pin Serial Data (SCL) is a clock input for 2-wire I^2C interface
OSCIN	I	External Clock Input pin The external and internal clock mode can be selected by the command. When the internal oscillator circuitry is used, this pin must be connected to V_{SS}
TEST1	I	Test mode input pin When this pin is connected to V_{DD}, the device will enter the test mode
TEST2	I	Power on reset control pin The internal power on reset circuitry will be enabled if this pin is connected to V_{SS}. If this pin is connected to V_{DD}, the internal power on reset circuitry will be disabled and the reset function will be performed by executing the software reset command
COM0~COM3	O	LCD Common outputs
SEG0~SEG35	O	LCD Segment outputs
VDD	—	Positive power supply
VSS	—	Negative power supply, ground
VLCD	—	LCD power supply pin

Approximate Internal Connections



Absolute Maximum Ratings

SupplyVoltage ..... V_{SS}-0.3V to V_{DD}+6.5V

Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V

Storage Temperature ..... -55°C to 150°C

Operating Temperature ..... -40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

V_{SS}=0V; V_{DD}=2.4V~5.5V; Ta=-40 to +85°C

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	2.4	—	5.5	V
V_{LCD}	LCD operating voltage	—	—	0	—	V_{DD}-2.4	V
V_{IH}	Input high Voltage	—	SCL, SDA, TEST1, TEST2	0.7V_{DD}	—	V_{DD}	V
V_{IL}	Input low Voltage	—	SCL, SDA, TEST1, TEST2	0	—	0.3V_{DD}	V
I_{IL}	Input leakage current	—	V_{IN}=V_{SS} or V_{DD}	-1	—	1	μA
I_{OL}	Low level output current	3.3V	V_{OL}=0.4V for SDA pin	6	—	—	mA
		5.0V		9	—	—	mA
I_{DD}	Operating Current	3.3V	No load, 1/3bias, B type inversion, Ta=25°C, LCD display on, f_{LCD}=80Hz, VLCD pin is connected to V_{SS}, Power save mode=Low Current2 mode	—	7.5	15	μA
		5.0V		—	12	20	μA
I_{STB1}	Standby Current	3.3V	No load, 1/3bias, B type inversion, Ta=25°C, LCD display off, f_{LCD}=80Hz, VLCD pin is connected to V_{SS}, Power save mode=Low Current2 mode	—	—	1	μA
		5.0V		—	—	2	μA
R_{PL}	Pull-Low Resistance	3.3V	For OSCIN pin	2.0	4.0	6.5	kΩ
		5.0V		1.5	3.0	4.5	kΩ
I_{OL1}	LCD Common Sink Current	—	V_{DD}-V_{LCD}=3.3V, V_{OL}=0.33V	250	400	—	μA
			V_{DD}-V_{LCD}=5V, V_{OL}=0.5V	500	800	—	μA
I_{OH1}	LCD Common Source Current	—	V_{DD}-V_{LCD}=3.3V, V_{OH}=2.97V	-140	-230	—	μA
			V_{DD}-V_{LCD}=5V, V_{OH}=4.5V	-300	-500	—	μA
I_{OL2}	LCD Segment Sink Current	—	V_{DD}-V_{LCD}=3.3V, V_{OL}=0.33V	250	400	—	μA
			V_{DD}-V_{LCD}=5V, V_{OL}=0.5V	500	800	—	μA
I_{OH2}	LCD Segment Source Current	—	V_{DD}-V_{LCD}=3.3V, V_{OH}=2.97V	-140	-230	—	μA
			V_{DD}-V_{LCD}=5V, V_{OH}=4.5V	-300	-500	—	μA

A.C. Characteristics

V_{SS}=0V,V_{DD}=2.4V~5.5V, Ta=-40 to +85°C

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
f_{LCD1}	LCD Frame Frequency	3.3V	Ta=25°C, internal oscillator is used, Display control command: P[4:3]="00"	72.0	80.0	88.0	Hz
			Ta=25°C, internal oscillator is used, Display control command: P[4:3]="01"	63.9	71	78.1	
			Ta=25°C, internal oscillator is used, Display control command: P[4:3]="10"	57.6	64.0	70.4	
			Ta=25°C, internal oscillator is used, Display control command: P[4:3]="11"	47.7	53.0	58.3	
f_{LCD2}	LCD Frame Frequency	2.4~5.5V	Ta=-40 to 85°C, internal oscillator is used, Display control command: P[4:3]="00"	56.0	80.0	104.0	Hz
			Ta=-40 to 85°C, internal oscillator is used, Display control command: P[4:3]="01"	49.7	71.0	92.3	
			Ta=-40 to 85°C, internal oscillator is used, Display control command: P[4:3]="10"	44.8	64.0	83.2	
			Ta=-40 to 85°C, internal oscillator is used, Display control command: P[4:3]="11"	37.1	53.0	68.9	
V_{POR}	V_{DD} Start Voltage to ensure Poewr-on Reset	—	—	—	—	100	mV
RR_{VDD}	V_{DD} Rise Rate to ensure Power-on Reset	—	—	0.05	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} to remain at V_{POR} to ensure Power-on Reset	—	—	10	—	—	ms

Note: $f_{LCD}=1/t_{LCD}$

I²C Interface Characteristics

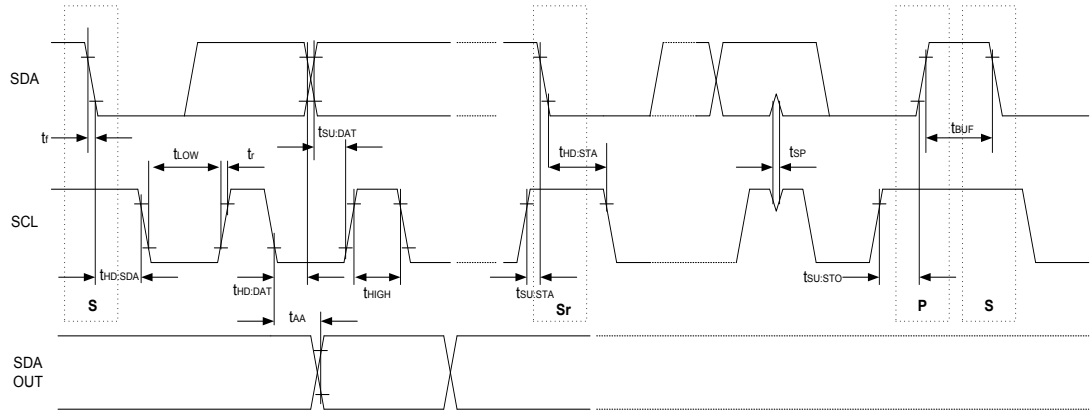
Unless otherwise specified, V_{SS}=0V; V_{DD}=2.4V~5.5V; Ta=-40 to +85°C

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{SCL}	Clock frequency	—	—	400	kHz
t_{BUF}	bus free time	Time in which the bus must be free before a new transmission can start	1.3	—	μs
$t_{HD:STA}$	Start condition hold time	After this period, the first clock pulse is generated	0.6	—	μs
t_{LOW}	SCL Low time	—	1.3	—	μs
t_{HIGH}	SCL High time	—	0.6	—	μs
$t_{SU:STA}$	Start condition setup time	Only relevant for repeated START condition	0.6	—	μs
$t_{HD:DAT}$	Data hold time	—	0	—	ns
$t_{SU:DAT}$	Data setup time	—	100	—	ns
t_R	SDA and SCL rise time	Note	—	0.3	μs
t_F	SDA and SCL fall time	Note	—	0.3	μs
$t_{SU:STO}$	Stop condition set-up time	—	0.6	—	μs
t_{AA}	Output Valid from Clock	—	—	0.9	μs
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	50	ns

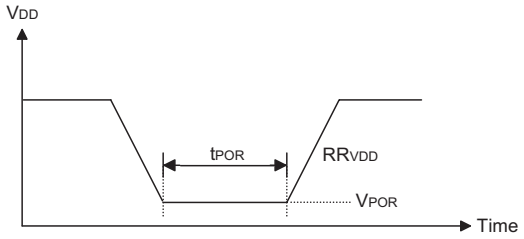
Note: These parameters are periodically sampled but not 100% tested.

Timing Diagrams

I²C Timing



Power On Reset Timing



Note: 1. If the conditions of Reset timing are not satisfied in power ON/OFF sequence, the internal Power on Reset (POR) circuit will not operate normally.

2. If it is difficult to meet power on reset timing conditions, please execute software reset command after Power on.

Functional Description

Power-On Reset

When the power is applied, the device is initialized by an internal power-on reset circuit. The status of the internal circuits after initialization is as follows:

- All common outputs are set to V_{SS}.
- All segment outputs are set to V_{SS}.
- LCD Driver Output Waveform: A-type inversion.
- Internal oscillator is selected.
- The 1/3 bias drive mode is selected.
- LCD bias generator is in an off state.
- LCD Display and internal oscillator are in off states.
- Power save mode is set to normal current.
- Frame Frequency is set to 80Hz.
- Blinking function is switched off.

Data transfers on the I²C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

System Oscillator

The timing for the internal logic and the LCD drive signals are generated by the internal oscillator or external clock source input. The System Clock frequency (f_{SYS}) determines the LCD frame frequency. During initial system power on the System Oscillator will be in the stop state.

Segment Driver Outputs

The LCD drive section includes up to 36 segment outputs SEG0~SEG35 which should be connected directly to the LCD panel. The segment output signals are generated in accordance with the multiplexed common signals and with the data resident in the display latch. The unused segment outputs should be left open-circuit.

Column Driver Outputs

The LCD drive section includes 4 column outputs COM0~COM3 which should be connected directly to the LCD panel. The column output signals are generated in accordance with the selected LCD drive mode. The unused column outputs should be left open-circuit if less than 4 column outputs are required.

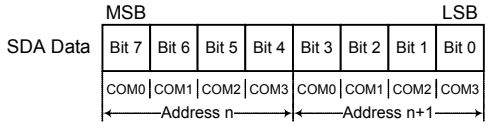
Address Pointer

The addressing mechanism for the display RAM is implemented using the address pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the address pointer by the Display Data Input command.

Display Memory – RAM Structure

The display RAM is static 36×4 bits RAM which stores the LCD data. Logic "1" in the RAM bit-map indicates the "on" state of the corresponding LCD segment; similarly, logic 0 indicates the "off" state.

The contents of the RAM data are directly mapped to the LCD data. The first RAM column corresponds to the segments operated with respect to COM0. In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with COM1, COM2 and COM3 respectively. The following diagram is a data transfer format for I²C interface.



LCD Display Output Data Transfer Format for I²C bus

Address	COM0	COM1	COM2	COM3	Output
00H					SEG0
01H					SEG1
02H					SEG2
03H					SEG3
04H					SEG4
05H					SEG5
06H					SEG6
07H					SEG7
08H					SEG8
09H					SEG9
0AH					SEG10
0BH					SEG11
0CH					SEG12
0DH					SEG13
0EH					SEG14
0FH					SEG15
10H					SEG16
11H					SEG17
12H					SEG18
13H					SEG19
14H					SEG20
15H					SEG21
16H					SEG22
17H					SEG23
18H					SEG24
19H					SEG25
1AH					SEG26
1BH					SEG27
1CH					SEG28
1DH					SEG29
1EH					SEG30
1FH					SEG31
20H					SEG32
21H					SEG33
22H					SEG34
23H					SEG35
RAM Data	Bit 3	Bit 2	Bit 1	Bit 0	

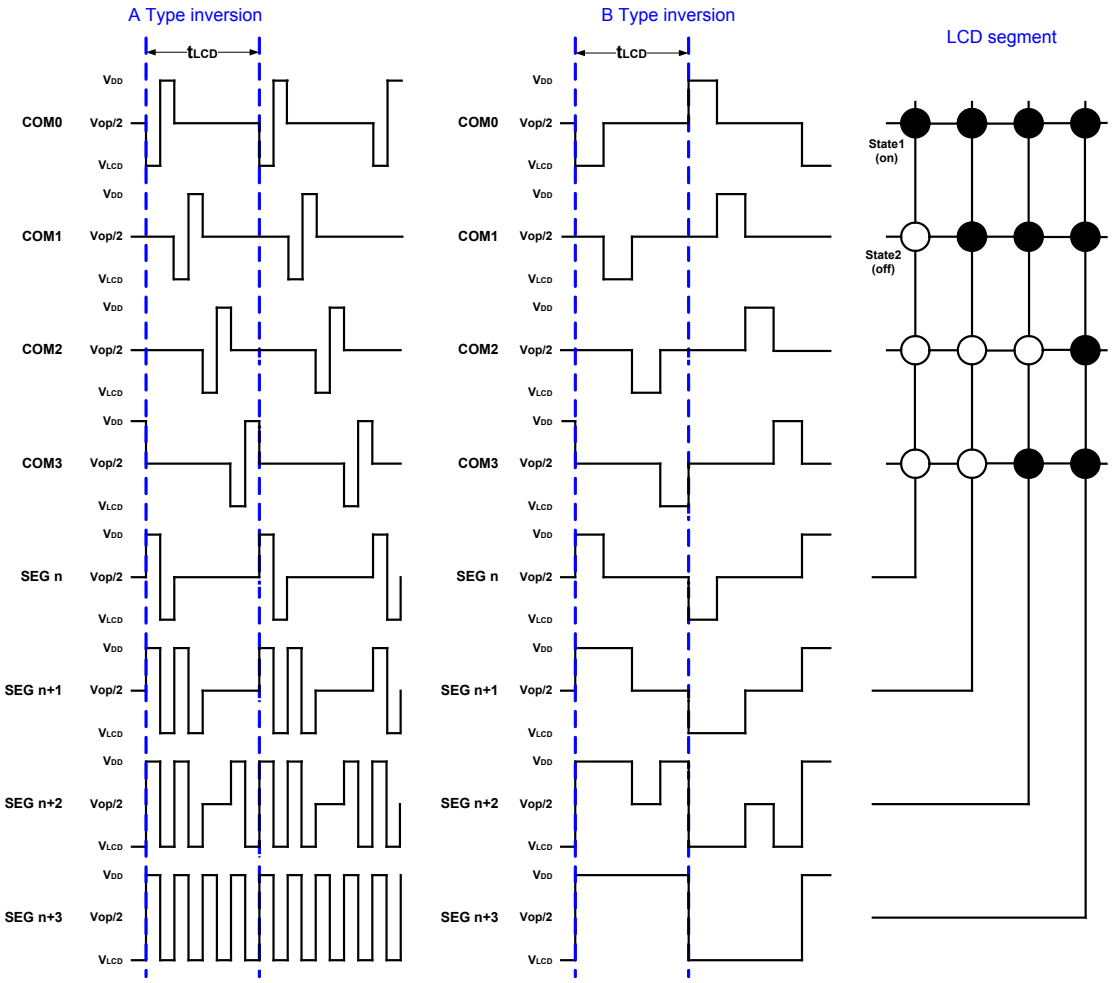
Note: The LCD display RAM address is specified by the Address Set command and the address will be automatically incremented by one after a 4-bit data is shifted in.

LCD Bias Generator

Fractional LCD biasing voltages, known as 1/2 or 1/3 bias voltage, are obtained from an internal voltage divider of three series resistors connected between V_{LCD} and V_{DD}. The centre resistor can be switched out of circuits to provide a 1/2 bias voltage level configuration.

LCD Drive Mode Waveforms

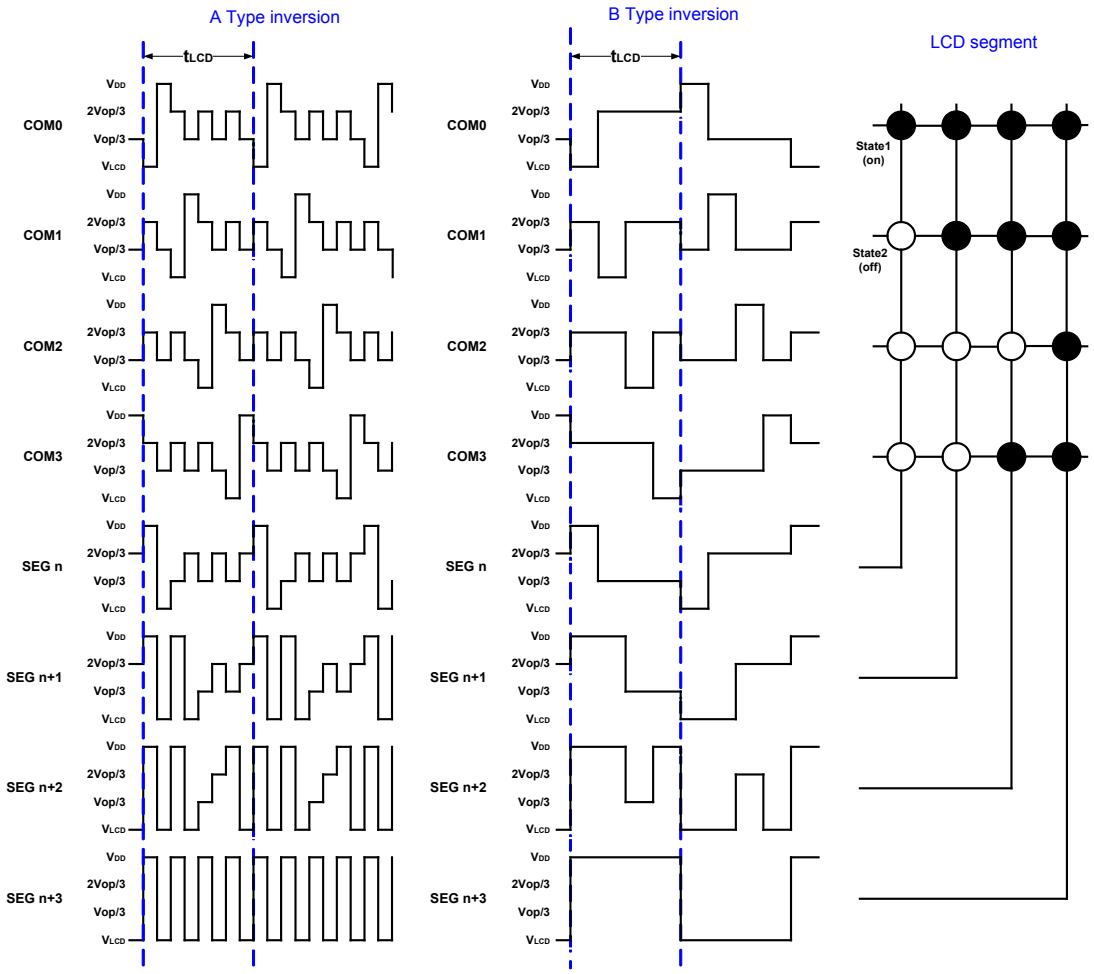
- When the LCD drive mode is selected as 1/4 duty and 1/2 bias, the waveform and LCD display is shown as follows:



Waveforms for 1/4 duty drive mode with 1/2 bias ($V_{OP}=V_{DD}-V_{LCD}$)

Note: $t_{LCD}=1/f_{LCD}$

- When the LCD drive mode is selected as 1/4 duty and 1/3bias, the waveform and LCD display is shown as follows:



Waveforms for 1/4 duty drive mode with 1/2 bias (V_{OP}=V_{DD}-V_{LCD})

Note: t_{LCD}=1/f_{LCD}

Blinking Function

The device contains versatile blinking capabilities. The whole display can be blinked at frequencies selected by the Blinking Frequency command. The blinking frequency is a subdivided ratio of the system frequency. The ratio between the system oscillator and blinking frequencies depends on the blinking mode in which the device is operating, as shown in the following table:

Blinking Mode	Blinking frequency (Hz)
0	Blink off
1	0.5
2	1
3	2

Frame Frequency

The device provides four frame frequencies selected with the Frame Frequency command known as 80Hz, 71Hz, 64Hz and 53Hz respectively.

Mode	Frame frequency (Hz) @ V_{DD}=3.3V
0	80
1	71
2	64
3	53

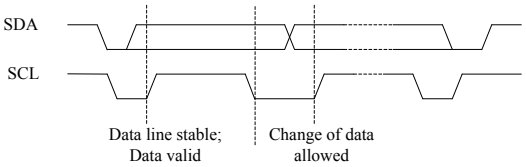
I²C Serial Interface

I²C Operation

The device supports I²C serial interface. The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via pull-up resistors. When the bus is free, both lines are high. Devices connected to the bus must have open-drain or open-collector outputs to implement a wired-or function. Data transfer is initiated only when the bus is not busy.

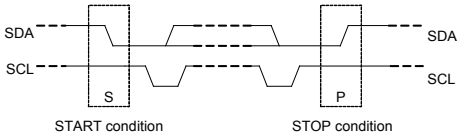
Data Validity

The data on the SDA line must be stable during the high period of the serial clock. The high or low state of the data line can only change when the clock signal on the SCL line is Low as shown in the diagram.



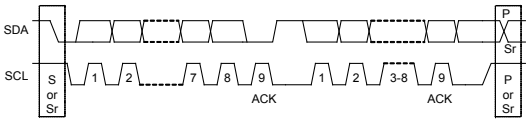
START and STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In some respects, the START(S) and repeated START (Sr) conditions are functionally identical.



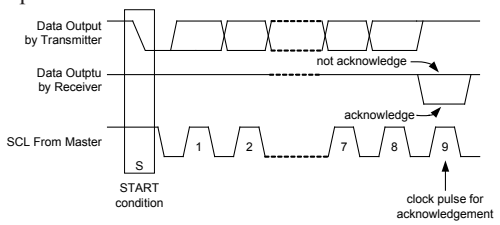
Byte Format

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit, MSB, first.



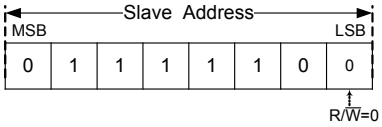
Acknowledge

- Each bytes of eight bits is followed by one acknowledge bit. This Acknowledge bit is a low level placed on the bus by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an Acknowledge, ACK, after the reception of each byte.
- The device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.
- A master receiver must signal an end of data to the slave by generating a not-acknowledge, NACK, bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse to not acknowledge. The master will generate a STOP or repeated START condition.



Slave Addressing

- The slave address byte is the first byte received following the START condition form the master device. The first seven bits of the first byte make up the slave address. This device only supports the write operation and therefore, the eighth data bit, R/$\overline{W}$, which is used to define a read or write operation will be fixed at a "0" state. If the R/$\overline{W}$ bit is set to 1 to execute a read operation, it will result in no operation.
- The HT9B92 device address bits are "0111110". When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an Acknowledge on the SDA line.

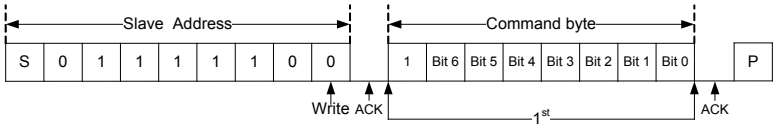


I²C Interface Write Operation

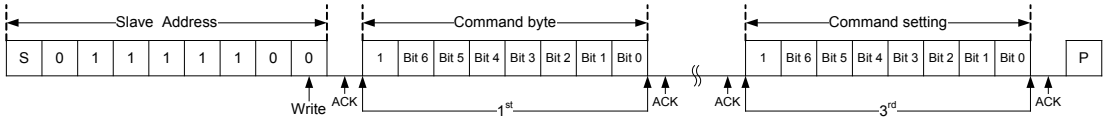
Byte Write Operation

- Single Command Type
  A Single Command write operation requires a START condition, a slave address with a write control bit, a command byte and a STOP condition for a single command write operation.
- Compound Command Type
  A Compound Command write operation requires a START condition, a slave address with a write control bit, a command byte, up to two command setting bytes and a STOP condition for a compound command write operation.
- Display RAM Single Data Byte
  A display RAM data byte write operation requires a START condition, a slave address with a write control bit, a valid Register Address byte, a Data byte and a STOP condition.

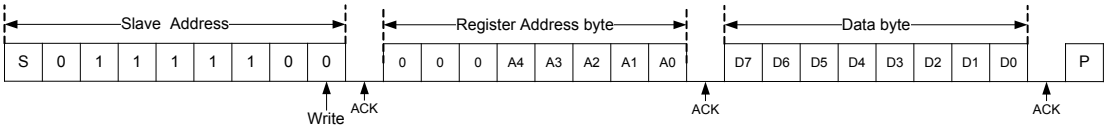
  The start address can only be set from 00H to 1FH. The start address which is greater than 1FH will be regarded as a command. Therefore, it is recommended that the start address should be set from 00H to 1FH.



I²C Single Command Type Write Operation



I²C Compound Command Type Write Operation



I²C Display RAM Single Data Byte Write Operation

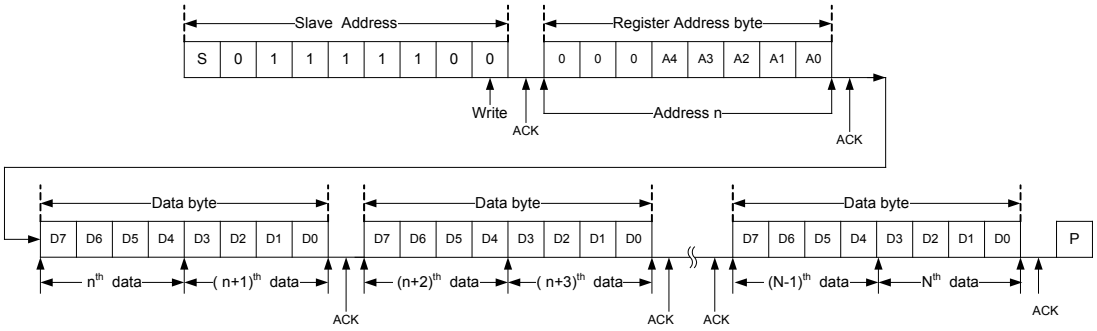
Display RAM Page Write Operation

After a START condition the slave address with a write control bit is placed on the bus followed with the specified display RAM Register Address of which the contents are written into the internal address pointer. The data to be written into the memory will be transmitted next. The internal address pointer will be incremented by 1 after a 4-bit data is shifted in. Then the acknowledge clock pulse will be received after an 8-bit data is shifted. After the internal address point reaches the maximum memory address, 23H, the address pointer will be reset to 00H. It is strongly recommended to write the display RAM data from address 00H to 23H using the Display RAM Page Write Operation.

Command Summary

The bit 7 denoted as "C" here is the control bit which is used to determine that the next byte is the display RAM data or command byte.

C bit	Remark
0	Next byte is Display RAM data.
1	Next byte is command.



I²C Interface N Bytes Display RAM Data Write Operation

Display RAM Address Setting Command

This command is used to define the start address of the display RAM.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note
Address Pointer	C	0	0	A4	A3	A2	A1	A0	Display RAM memory start address

Note: 1. The address ranges from 00H to 1FH.
2. It is strongly recommended to write the display RAM data from address 00H to 23H at one time.
3. Power on status: the address will be set to 00H.
4. If the programmed command is not defined, the function will not be affected.

Drive Mode Setting Command

This command is used to control the LCD bias and display on/off.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note
Bias and Display on/off setting	C	1	0	X	P3	P2	X	X	—

Note:

P2	Bias
0	1/3 bias (default)
1	1/2 bias

P3	LCD Display On/Off
0	Off (default)
1	On

- Power on status: The 1/3 bias drive mode is selected and the LCD display is switched off.
- If the programmed command is not defined, the function will not be affected.

Display Control Command

This command is used to select the Current mode according to the characteristics of the LCD panel for achieving high display quality and LCD driver output waveform set and frame frequency select.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note
Display Control Setting	C	0	1	P4	P3	P2	P1	P0	—

Note:

P [1:0]	Power Save Mode	Current Consumption	Remark
00	Low Current2 Mode	x 0.5	● The data listed here is for reference only. The actual data depends upon the panel load. ● Please meet the condition: $V_{DD}-V_{LCD}\geq 3V$ when used in High current mode.
01	Low Current1 Mode	x 0.67	
10	Normal Current Mode	x 1 (default)	
11	High Current Mode	x 1.8	

P2	LCD Driver Output Waveform	Remark
0	A Type inversion (default)	
1	B Type inversion	

P [4:3]	Frame Frequency @V_{DD}=3.3V (Hz)	Remark
00	80 (default)	● The data listed here is for reference only. The actual data depends upon the panel load. ● Please meet the condition: $V_{DD}-V_{LCD}\geq 3V$ when used in High current mode.
01	71	
10	64	
11	53	

● The setting of the frame frequency, LCD output waveform and current mode will influence the display image qualities. Please select a proper display setting suitable for the current consumption and display image quality with LCD panel.

Mode	Flicker	Image Quality/Contrast
Frame Frequency	O	
LCD Driver Output Waveform	O	O
Power Save Mode		O

● If the programmed command is not defined, the function will not be affected.

Software Reset and Oscillator Mode Setting Command

This command is used to select the system oscillator source and to initiate a software reset.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note
System Oscillator Setting and Software Reset	C	1	1	0	1	X	P1	P0	—

P1	Software Reset	Remark
0	No Operation (default)	When a "Software Reset" is executed, the device will be reset to an initial condition. Other settings can be configured after Software reset is completed.
1	Initiate a Software Reset	

P0	Oscillator Mode	Remark
0	Internal Oscillator (default)	• When the internal oscillator is used, the OSCIN pin must be connected to VSS or open-circuit.
1	External Clock Input Mode	• When the external clock mode is selected, the external clock is supplied on the OSCIN pin.

When the software reset is executed, the device is initialized by an internal power-on reset circuit. The status of the internal circuits after initialization is as follows:

- All common outputs are set to V_{SS}.
- All segment outputs are set to V_{SS}.
- LCD Driver Output Waveform: A-type inversion.
- Internal oscillator source is selected.
- 1/3 bias is selected.
- LCD bias generator is off state.
- LCD Display and system oscillation are off state.
- Power save mode is set to normal current.
- Frame Frequency is set to 80Hz.
- Blinking function is switched off.

Note that if the programmed command is not defined, the function will not be affected.

Blinking Frequency Setting Command

This command defines the blinking frequency of the display modes.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note
Blinking Frequency setting	C	1	1	1	0	X	P1	P0	—

Note:

P [1:0]	Blinking Frequency	Remark
00	Blinking off (default)	—
01	0.5 Hz	
10	1 Hz	
11	2 Hz	

- Power on status: Blinking function is switched off.
- If the programmed command is not defined, the function will not be affected.

All Pixels On/Off Setting Command

This command controls that all pixels are switched on or off when the LCD normally displays.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note
All Pixels On/Off setting	C	1	1	1	1	1	P1	P0	—

Note:

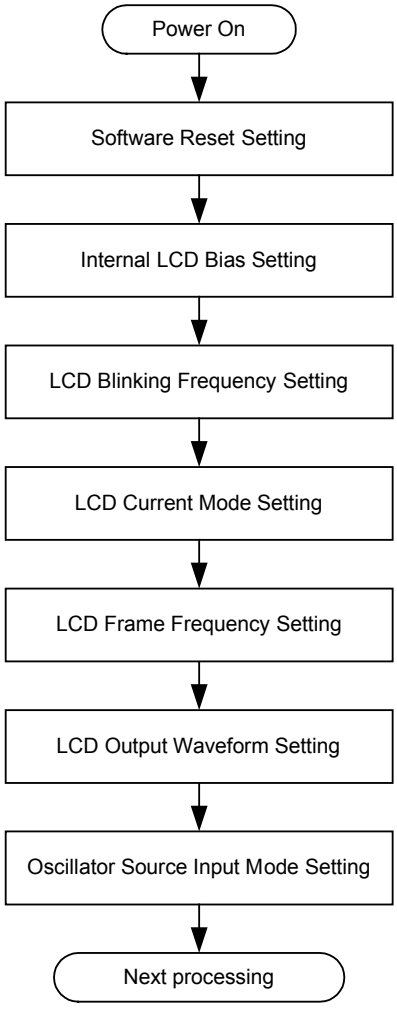
P [1:0]	Blinking Frequency	Remark
00	Normal Display (default)	● This command is only available when the LCD is normally displayed. The display RAM contents will not be changed when this command is executed. ● All pixels are switched on or off regardless of the display RAM data when the relevant setting is selected.
01	All Pixels Off	
10	All Pixels On	
11	All Pixels Off	

● Power on status: Normal display.
● If the programmed command is not defined, the function will not be affected.

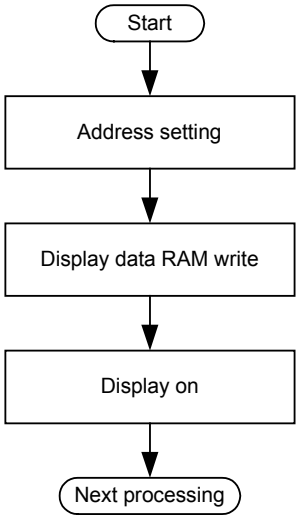
Operation Flow Chart

Access procedures are illustrated below using flowcharts.

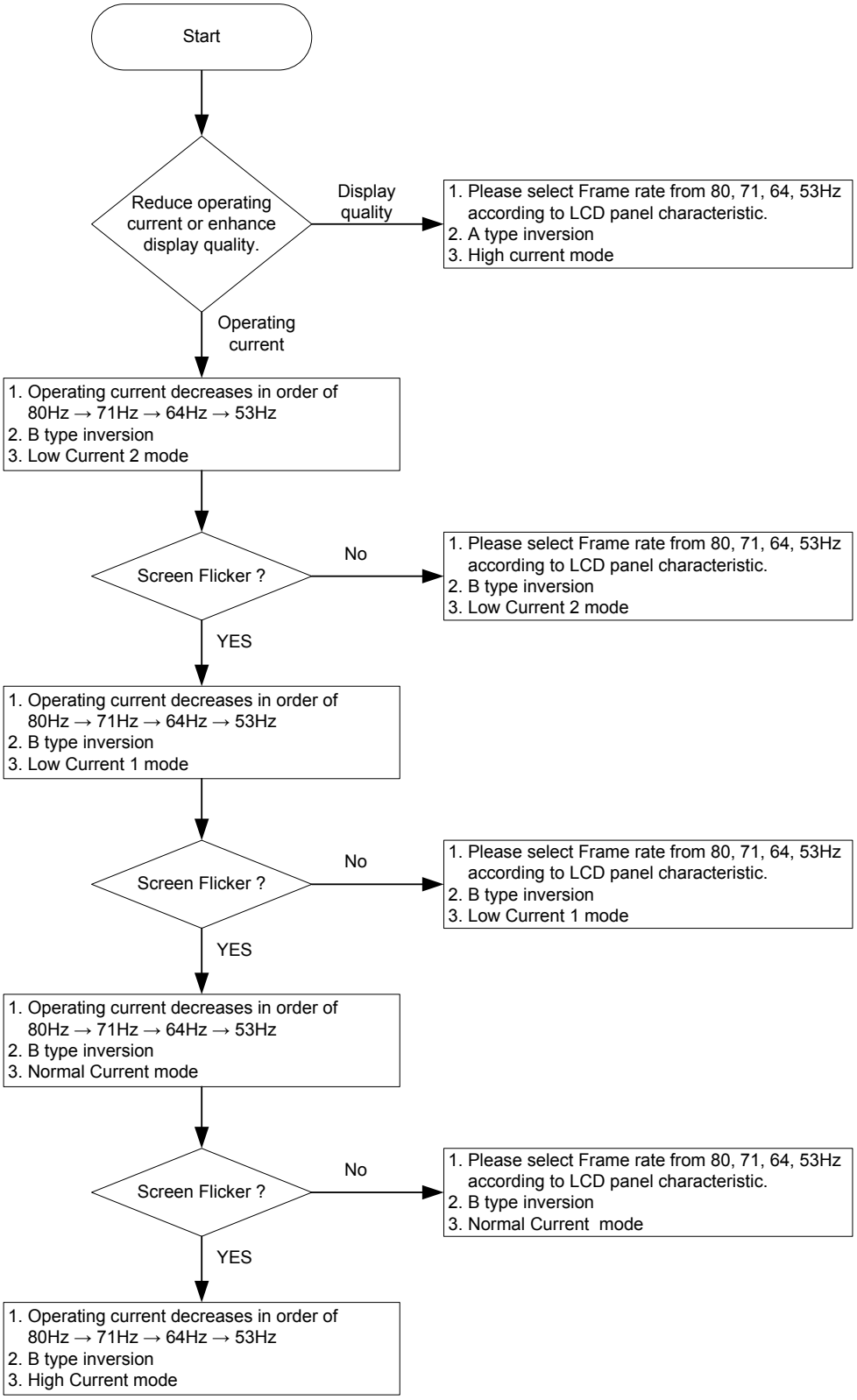
Initialization



Display Data Write (Address Setting)



Display Quality or Operating Current (Power Save Mode) Setting



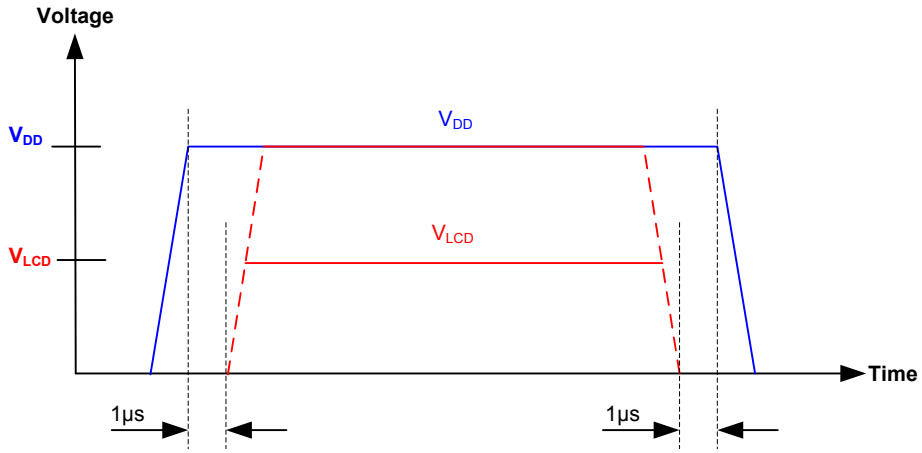
Power Supply Sequence

- If the power is individually supplied on the LCD and VDD pins, it is strongly recommended to follow the Holtek power supply sequence requirement.
- If the power supply sequence requirement is not followed, it may result in malfunction.

Holtek Power Supply Sequence Requirement:

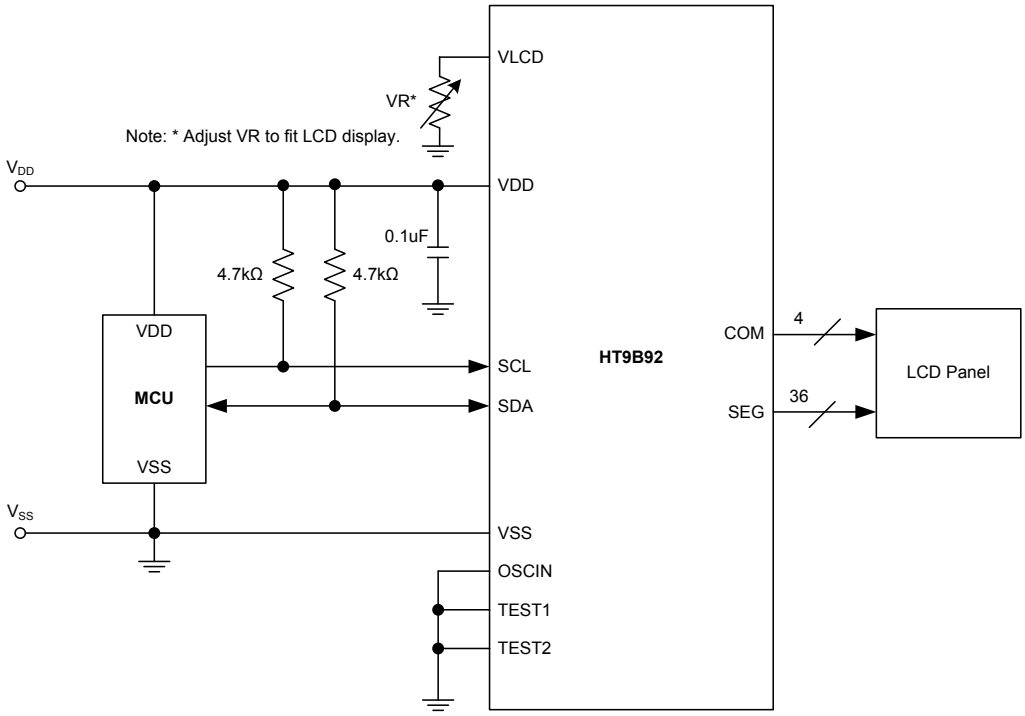
1. Power-on sequence:
   Turn on the logic power supply V_{DD} first and then turn on the LCD driver power supply V_{LCD}.
2. Power-off sequence:
   Turn off the LCD driver power supply V_{LCD}. First and then turn off the logic power supply V_{DD}.
3. The Holtek Power Supply Sequence Requirement must be followed no matter whether the V_{LCD} voltage is higher than the V_{DD} voltage.

- When the V_{LCD} voltage is smaller than or is equal to V_{DD} voltage application

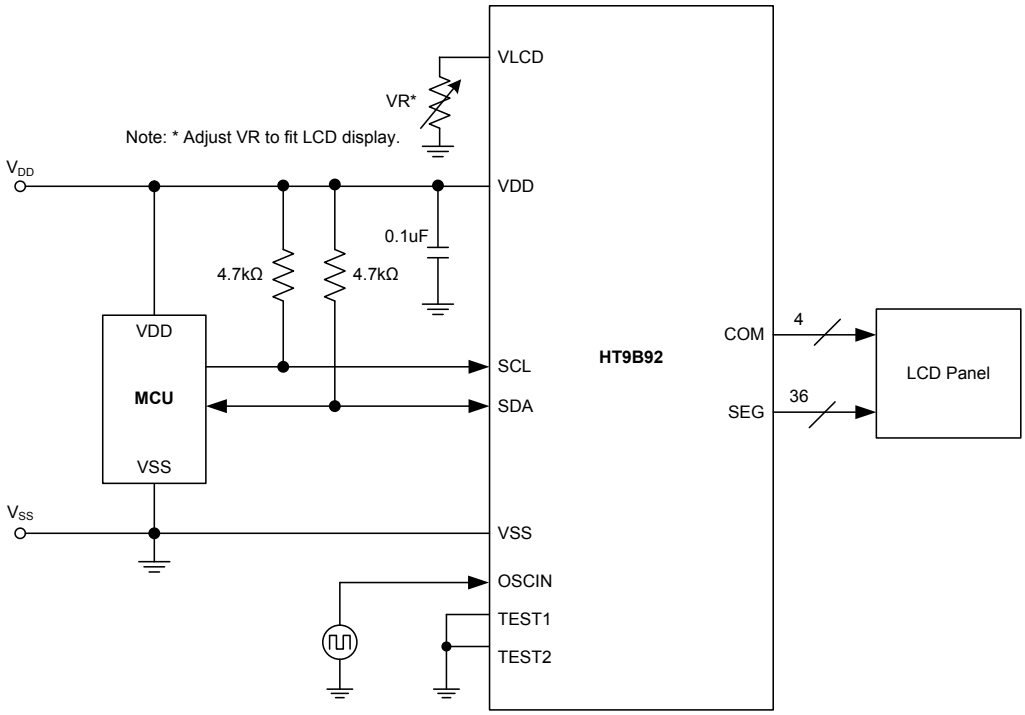


Application Circuit

Internal Oscillator Circuit Mode



External Clock Input Mode



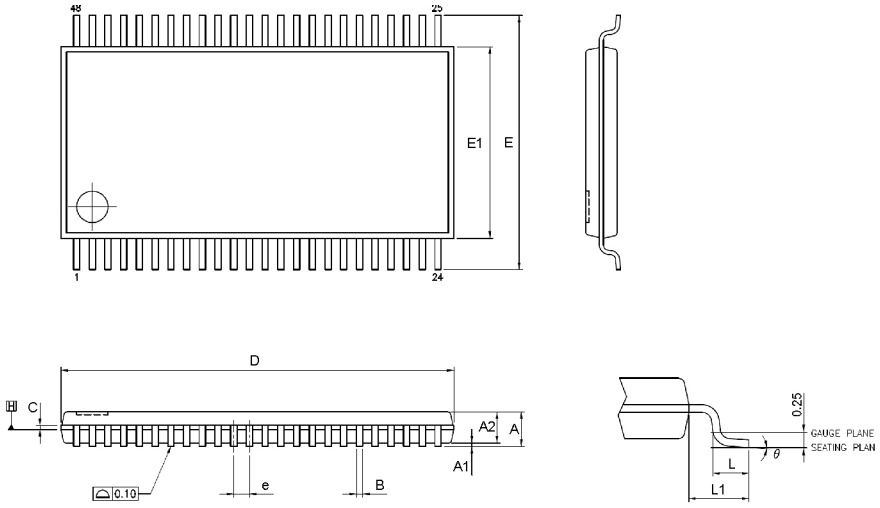
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

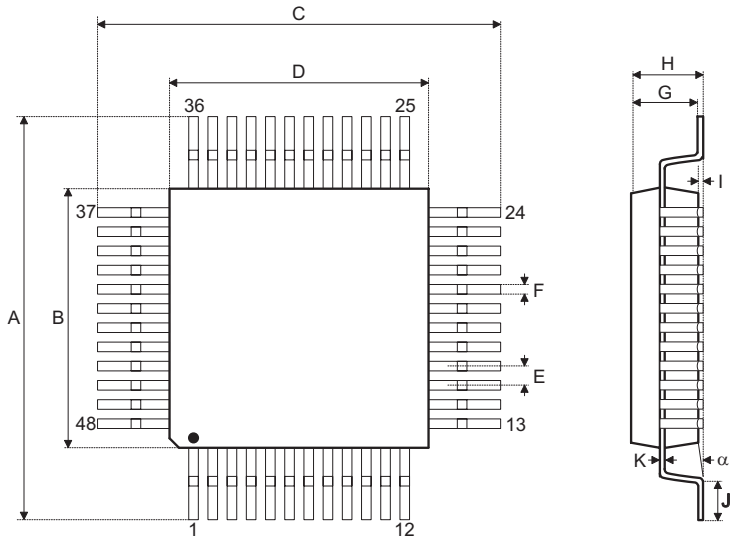
48-pin TSSOP Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	—	0.047
A1	0.002	—	0.006
A2	0.031	0.039	0.041
B	0.007	—	0.011
C	0.004	—	0.008
D	0.488	0.492	0.496
E	—	0.319 BSC	—
E1	0.236	0.240	0.244
e	—	0.020 BSC	—
L	0.018	0.024	0.030
L1	—	0.039 BSC	—
y	—	0.004	—
θ	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1	1.05
B	0.17	—	0.27
C	0.09	—	0.20
D	12.40	12.50	12.60
E	—	8.10 BSC	—
E1	6.00	6.10	6.20
e	—	0.50 BSC	—
L	0.45	0.60	0.75
L1	—	1.0 BSC	—
y	—	0.10	—
θ	0°	—	8°

48-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.50 BSC	—
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°