

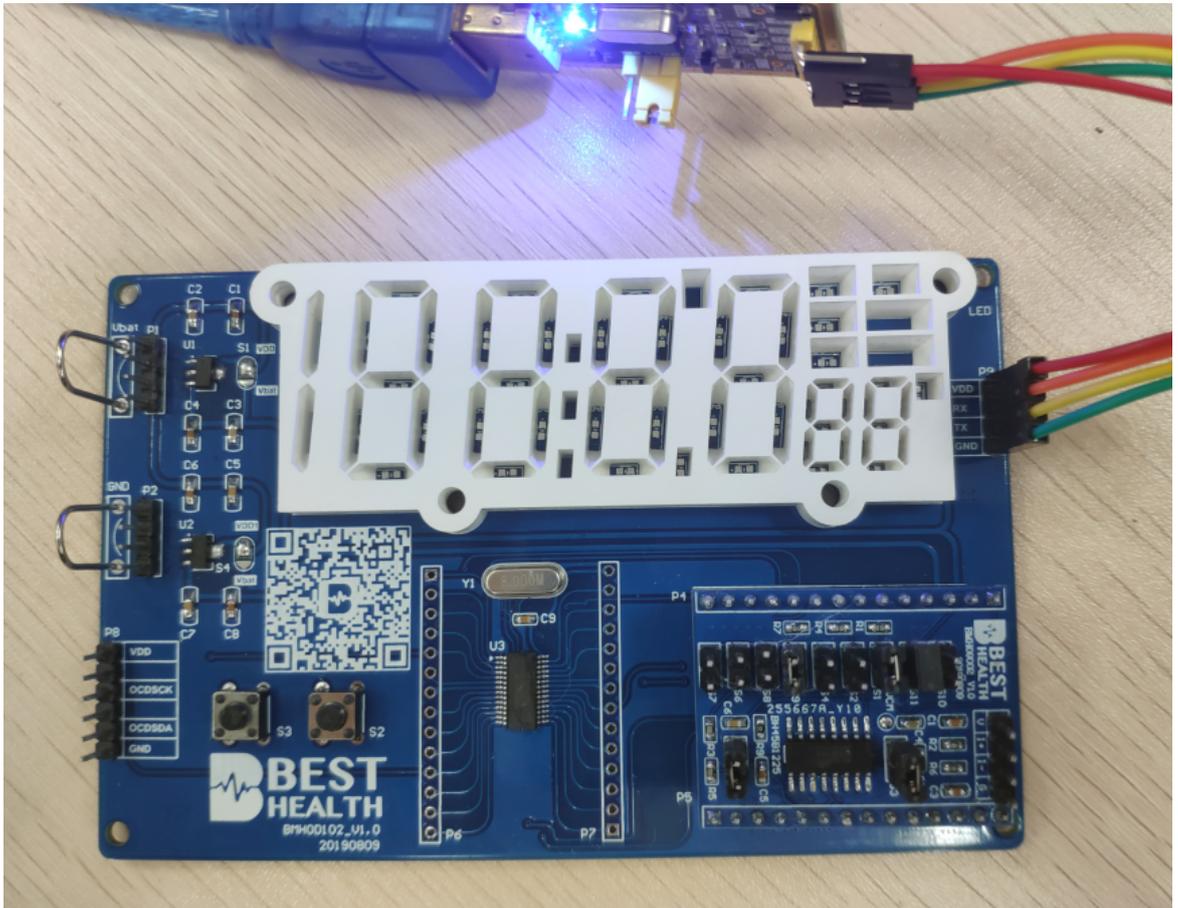
BH45B1225_24bit-ADC 開發套件操作說明

一、 套件介紹

此套件採用 IIC 通訊 (HT66F0185 為主機, BH45B1225 為從機) 和 UART 通訊。過程如下：

1. 用戶通過界面設置上位機, 設置的內容通過 UART 通訊發送給主機
2. 主機將接收到的內容通過 IIC 通訊發送給從機, 進行 ADC 配置, 並使能從機採集 ADC 數據
3. 從機將 ADC 數據傳回到主機
4. 主機通過 UART 通訊將 ADC 數據傳輸到上位機觀察

接線如下圖所示：



二、 上位機使用方法

打開上位機，按照下圖進行配置（此接法為測試 BH45B1225 的 ENOB）：

The screenshot displays the '24Bit ADC Testing Platform' software interface. On the left, there are three main configuration panels: 'Device Setting', 'COM Setting', and 'Raw Data Analysis'. The 'Device Setting' panel shows 'Device' set to 'BH45B1225' and 'Sys Clock' set to '4.9MHz'. The 'COM Setting' panel shows 'COM' set to 'COM3', 'Baud Rate' set to '38400', 'Stop Bits' set to '1', 'Data Bits' set to '8', and 'Parity' set to 'None'. The 'Raw Data Analysis' panel shows 'MAX: 9', 'MIN: -5', 'AVG: 2', and 'VOL: 0.000250339508056641mV'. Below these panels are 'Sliding Average Analysis' and 'IIR Filter Analysis' sections. The main configuration area on the right is titled 'AFE Power Setting: VCM_OFF' and contains a block diagram of the ADC system. The diagram shows two channels, 'CHSP' and 'CHSN', connected to 'EMI' inputs. The 'CHSP' channel is connected to the 'DI+' input of the 'PGA' (Programmable Gain Amplifier), and the 'CHSN' channel is connected to the 'DI-' input. The 'PGA' output is connected to the 'PGAOP' and 'PGAON' inputs of the 'AD Converter'. The 'AD Converter' has 'ADC Gain = x1', 'VREFGN = x1', and 'DCSET = +0V'. The 'AD Converter' output is connected to the 'REFP' and 'REFN' inputs of the 'VREFP&VRE' block. The 'VREFP&VRE' block has 'Vrefp = 1.05 V' and 'Vrefn = 0.00 V'. The 'AD Converter' is connected to the 'DataRate = 5Hz', 'ADCK = 31', 'OSR = 32768', and 'FLMS: fM/30' settings. The 'AD Converter' is also connected to the 'fsys 4.9MHz' and 'VCM: 1.25' settings. The 'AD Converter' output is connected to the 'AD Result' block. The bottom panel shows a waveform graph with 'RAW Data' (blue), 'Sliding Average' (red), and 'IIR Filter' (green) traces. The graph has a y-axis from 1 to 9 and an x-axis from 1024 to 50. The 'AD Sample Buff: 1024' is displayed at the top of the graph.

操作步驟：

1. 依次配置 Device Setting、COM Setting，按下 OPEN 鍵即配置完成。
2. 配置 AFE Power Setting，按下 OK 鍵即配置完成。
3. 按下播放按鈕  開始獲取 ADC 數據。