WK2124

SPI Interface
Four-channel Universal Asynchronous Receiver Transmitter
Lead-free Package

1. Product Description

WK2124 is 4-channel UART device with SPI™ interface. It realizes SPI bridging/extending to four enhancements UART.

UART extended slave channels has the following features:

- Each slave channel UART baud rate, word length, parity format can be set independently. We can provide the highest communication rate at 2Mbps.
- Each slave channel can be set independently in the IrDA infrared communications.
- Each slave channel has send / receive an independent 256 FIFO. According to user needs, FIFO programmed trigger.

WK2124 adopts SSOP20L green lead-free package and can operate in a wide operating voltage range of 2.5 ~ 5.0V. It can be configured with automatic sleep / wake function.

[Note]: SPI™ is registered trademark of MOTOROLA Company.

2. Basic Characteristics

2.1 General Features

- Send and receive large hardware cache, support 256 FIFO
- Low-power design, you can configure the automatic sleep, automatic wake-up mode(uS grade wake)
- Wide operating voltage design, operating voltage of 2.5V ~ 5.0V
- Streamlined configuration registers and control words, simple and reliable operation
- Provide industrial products
- High-speed CMOS technology, the slave UART data rate of up to 2Mbps@5V, 1.5Mbps@3.3V, 1Mbps@2.5V
- Used in line with environmental protection policies SSOP20 lead-free package

2.2 Extended Slave Channel UART Features

- Independent slave channel UART port configuration, speed, flexibility:

  Each child window to full-duplex, each child window via software on / off

  The baud rate can be set independently, the highest child window can reach 2M bps

  Each slave character UART format can be set independently including data length, stop bits, parity mode

  Perfect child window status query function

  It can be achieved on a single slave UART port software reset
- FIFO function:

  Each child window has a separate 256 transmit FIFO, transmit FIFO trigger point can be programmed according to user needs

  Each child window has a separate 256 receiving FIFO, receive FIFO trigger point can be

programmed according to user needs

FIFO software enabled and emptying

FIFO status and counter output

- Error detection:

  Support parity error, framing error, overrun error, and Line-Break error detection

  Support start bit error detection

- Built in SIR line with standard IrDA infrared transceiver codecs, transmission speeds of up to 115.2K bit/s
- Interrupt features:

  With slave UART receive FIFO timeout interrupt

  Support Line-Break error interrupt

2.3 SPI Interface Features

- 10Mbit/s maximum speed
- Support slave mode only
- SPI mode 0
- Support the longest continuous transceiver 256 bytes

3. Applications

- Multi-UART server / UART boards
- Industrial / automation field RS485 control
- Wireless data transmission by 2G/3G/4G
- Telematics Platform / Car GPS positioning system
- Remote automatic meter reading (AMR) systems
- POS / tax control POS / financial machinery
- DSP / Embedded Systems

4. Ordering Information

Table 4.1 WK2124 Ordering Information

Product Type	Package	Explanation
WK2124-ISSG	SSOP20 Lead-free package	General industrial grade; operating temperature -45℃～+85℃

5. Block Diagram

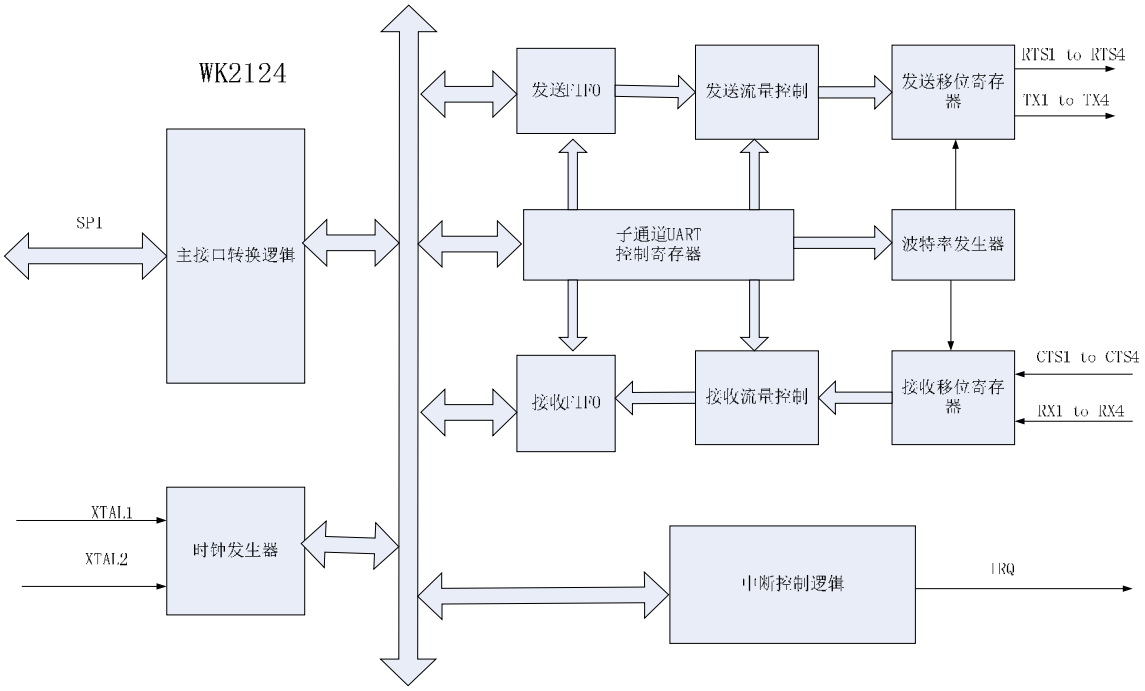
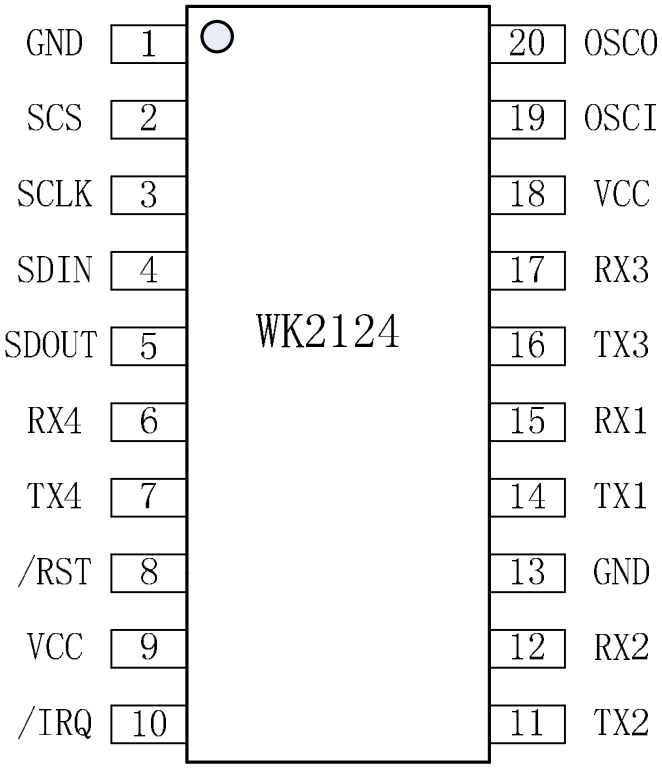


Figure 5.1 WK2124 Block Diagram

6. Package Pins

6.1 Figure Package



6.2 Pin Description

Table 6.2 WK2124 Pin Description

Symbol	Pin	Type	Function Description
GND	1,13	-	Ground
SCS	2	I/O	SPI chip select
SCLK	3	I/O	SPI clock
SDIN	4	I/O	SPI data input
SDOUT	5	I/O	SPI data output
RX1 RX2 RX3 RX4	15 12 17 6	I	UART receiver input
TX1 TX2 TX3 TX4	14 11 16 7	O	UART transmitter output
RST	8	I	Hardware reset, active low reset effective
VCC	9,18	-	Power supply
IRQ	10	O	Interrupt output, active high
OSCI	19	I	Oscillator input
OSCO	20	O	Oscillator output

7. Register Description

7.1 Register List

WK2124 internal registers address is a 6bit decoder, the address 000000~111111. It divides into the global register and slave UART register.

Global registers have 4, the specific arrangement of global register address is shown in Table 7.1.

Table 7.1 Global Register Lists

Addr[5:0]	Naming	Type	Function Description
000000	GENA	R/W	Global Control Register
000001	GRST	R/W	Global slave UART Reset Register
010000	GIER	R/W	Global Interrupt Register
010001	GIFR	R	Global Interrupt Flag Register

Slave UART registers have 18, which are arranged in C1C0 REG[3:0]. The higher 2bit is the slave UART channel number, and the lower 4bit is the register address. The following table shows the address of lower 4bit allocation.

Table 7.2 Slave UART Control Register

Addr[3:0]	Naming	Type	Function Description	
(C1,C0) 0011	SPAGE	R/W	Slave UART Page Control Register	
(C1,C0) 0100	SCR	R/W	Slave UART Enable Register	SPAGE0
(C1,C0) 0101	LCR	R/W	Slave UART Configuration Register	SPAGE0
(C1,C0) 0110	FCR	R/W	Slave UART FIFO Control Register	SPAGE0

(C1,C0) 0111	SIER	R/W	Slave UART Interrupt Enable Register	SPAGE0
(C1,C0) 1000	SIFR	R/W	Slave UART Interrupt Flag Register	SPAGE0
(C1,C0) 1001	TFCNT	R	Slave UART Transmit FIFO Count Register	SPAGE0
(C1,C0) 1010	RFCNT	R	Slave UART Receive FIFO Count Register	SPAGE0
(C1,C0) 1011	FSR	R	Slave UART FIFO Status Register	SPAGE0
(C1,C0) 1100	LSR	R	Slave UART Receive Status Register	SPAGE0
(C1,C0) 1101	FDAT	R/W	Slave UART FIFO Data Register	SPAGE0
(C1,C0) 0100	BAUD1	R/W	Slave UART Baud Rate Configuration Register High Byte	SPAGE1
(C1,C0) 0101	BAUD0	R/W	Slave UART Baud Rate Configuration Register Low Byte	SPAGE1
(C1,C0) 0110	PRES	R/W	Slave UART Baud Rate Configuration Register Decimal Part	SPAGE1
(C1,C0) 0111	RFTL	R/W	Slave UART Receive FIFO Interrupt Trigger Point Configuration Register	SPAGE1
(C1,C0) 1000	TFTL	R/W	Slave UART Transmit FIFO Interrupt Trigger Point Configuration Register	SPAGE1

C1,C0: slave channel number, 00~11, corresponding to the slave UART port 1 to 4.

7.2 Register Description

7.2.1 GENA Global Control Register: (000000)

Bit	Rst	Function Description	Type
Bit7	0	RSV (reserved)	R
Bit6	0	RSV (reserved)	R
Bit5	1	RSV (reserved)	R
Bit4	1	RSV (reserved)	R
Bit3	0	UT4EN: slave UART 4 clock enable (slave UART clock off can achieve lower power consumption) 0: Disabled 1: Enabled	W/R
Bit2	0	UT3EN: slave UART 3 clock enable (slave UART clock off can achieve lower power consumption) 0: Disabled 1: Enabled	W/R
Bit1	0	UT2EN: slave UART 2 clock enable (slave UART clock off can achieve lower power consumption) 0: Disabled 1: Enabled	W/R
Bit0	0	UT1EN: slave UART 1 clock enable (slave UART clock off can achieve lower power consumption) 0: Disabled 1: Enabled	W/R

7.2.2 GRST Global Slave UART Reset Register: (000001)

Bit	Rst	Function Description	Type
Bit7	0	UT4SLEEP: slave UART 4 sleep status (reduce power consumption, wake up automatically) 0: Not sleep 1: Sleep	R
Bit6	0	UT3SLEEP: slave UART 3 sleep status (reduce power	R

		consumption, wake up automatically) 0: Not sleep 1: Sleep	
Bit5	0	UT2SLEEP: slave UART 2 sleep status (reduce power consumption, wake up automatically) 0: Not sleep 1: Sleep	R
Bit4	0	UT1SLEEP: slave UART 1 sleep status (reduce power consumption, wake up automatically) 0: Not sleep 1: Sleep	R
Bit3	0	UT4RST: slave UART 4 soft reset control 0: Not reset slave UART 4 1: Reset slave UART 4	W1/R0
Bit2	0	UT3RST: slave UART 3 soft reset control 0: Not reset slave UART 3 1: Reset slave UART 3	W1/R0
Bit1	0	UT2RST: slave UART 2 soft reset control 0: Not reset slave UART 2 1: Reset slave UART 2	W1/R0
Bit0	0	UT1RST: slave UART 1 soft reset control 0: Not reset slave UART 1 1: Reset slave UART 1	W1/R0

7.2.3 GIER Global Interrupt Register: (010000)

Bit	Rst	Function Description	Type
Bit7--5	000	RSV (reserved)	R
Bit4	0	RSV (reserved)	W/R
Bit3	0	UT4IE: slave UART 4 interrupt enable control 0: Disabled 1: Enabled	W/R
Bit2	0	UT3IE: slave UART 3 interrupt enable control 0: Disabled 1: Enabled	W/R
Bit1	0	UT2IE: slave UART 2 interrupt enable control 0: Disabled 1: Enabled	W/R
Bit0	0	UT1IE: slave UART 1 interrupt enable control 0: Disabled 1: Enabled	W/R

7.2.4 GIFR Global Interrupt Flag Register: (010001)

Bit	Rst	Function Description	Type
Bit7--4	000	RSV (reserved)	R
Bit3	0	UT4INT: slave UART 4 interrupt flag 0: Not interrupt 1: Interrupt	R
Bit2	0	UT3INT: slave UART 3 interrupt flag 0: Not interrupt 1: Interrupt	R
Bit1	0	UT2INT: slave UART 2 interrupt flag 0: Not interrupt 1: Interrupt	R
Bit0	0	UT1INT: slave UART 1 interrupt flag 0: Not interrupt 1: Interrupt	R

7.2.5 SPAGE Slave UART Page Control Register: (0011)

Bit	Rst	Function Description	Type

Bit7--1	000000	RSV (reserved)	R
Bit0	0	PAGE: slave UART page control (slave UART register distributes on PAGE0 and PAGE1 and switches different pages by the register) 0: PAGE0 1: PAGE1	W/R

7.2.6 SCR Slave UART Control Register: (PAGE0: 0100)

Bit	Rst	Function Description	Type
Bit7--3	000	RSV (reserved)	W/R
Bit2	0	SLEEPEN: slave UART sleep enable 0: Disabled 1: Enabled	W/R
Bit1	0	TXEN: slave UART transmitter enable 0: Disabled 1: Enabled	W/R
Bit0	0	RXEN: slave receiver sleep enable 0: Disabled 1: Enabled	W/R

7.2.7 LCR Slave UART Configuration Register: (PAGE0: 0101)

Bit	Rst	Function Description	Type
Bit7--6	00	RSV (reserved)	W/R
Bit5	0	BREAK: slave UART Line-Break output control 0: Normal output 1: Line-Break output (TX forced output 0)	W/R
Bit4	0	IREN: slave UART infrared enable 0: Normal mode 1: Infrared mode	W/R
Bit3	0	PAEN: slave UART parity enable 0: Not parity bit(8-bit data) 1: Parity bit(9-bit data)	W/R
Bit2--1	0	PAM1--0: slave UART parity mode selection PAEN=1, slave UART parity enable: 00: force 0 parity 01: odd parity 10: even parity 11: force 1 parity	W/R
Bit0	0	STPL: slave UART stop bit length control 0: 1 bit 1: 2 bits	W/R

7.2.8 FCR Slave UART FIFO Control Register: (PAGE0: 0110)

Bit	Rst	Function Description	Type
Bit7--6	00	TFTRIG[1:0]: slave UART transmit FIFO trigger level setting TFTL[7:0]=0: 00: 8 byte 01: 16 byte 10: 24 byte 11: 30 byte	W/R
Bit5--4	00	RFTRIG[1:0]: slave UART receive FIFO trigger level setting RFTL[7:0]=0: 00: 8 byte 01: 16 byte 10: 24 byte 11: 28 byte	W/R
Bit3	0	TFEN: slave UART transmit FIFO enable 0: Disabled 1: Enabled	W/R

Bit2	0	RFEN: slave UART receive FIFO enable 0: Disabled 1: Enabled	W/R
Bit1	0	TFRST: slave UART transmit FIFO reset (write 1 resetting,set to 0 automatically after completion) 0: Disabled reset 1: Reset FIFO	W1/R0
Bit0	0	RFRST: slave UART receive FIFO reset (write 1 resetting,set to 0 automatically after completion) 0: Disabled reset 1: Reset FIFO	W1/R0

7.2.9 SIER Slave UART Interrupt Enable Register: (PAGE0: 0111)

Bit	Rst	Function Description	Type
Bit7	0	FERR_IEN: receive FIFO error interrupt enable 0: Forbidden to receive FIFO error interrupt 1: Enabled to receive FIFO error interrupt	W/R
Bit6	0	RSV (reserved)	W/R
Bit5	0	RSV (reserved)	W/R
Bit4	0	RSV (reserved)	W/R
Bit3	0	TFEMPTY_IEN: transmit FIFO empty interrupt enable 0: Forbid transmit FIFO empty interrupt 1: Enable transmit FIFO empty interrupt	W/R
Bit2	0	TFTRIG_IEN: transmit FIFO trigger interrupt enable 0: Forbid transmit FIFO trigger interrupt 1: Enable transmit FIFO trigger interrupt	W/R
Bit1	0	RXOVT_IEN: receive FIFO overtime interrupt enable 0: Forbid receive FIFO overtime interrupt 1: Enable receive FIFO overtime interrupt	W/R
Bit0	0	RFTRIG_IEN: receive FIFO trigger interrupt enable 0: Forbid receiver FIFO trigger interrupt 1: Enable receive FIFO trigger interrupt	W/R

7.2.10 SIFR Slave UART Interrupt Flag Register: (PAGE0: 1000)

Bit	Rst	Function Description	Type
Bit7	0	FERR_INT: receive FIFO data error interrupt flag 0: Not receive FIFO data error interrupt 1: Receive FIFO data error interrupt	W/R
Bit6	0	RSV (reserved)	W/R
Bit5	0	RSV (reserved)	W/R
Bit4	0	RSV (reserved)	W/R
Bit3	0	TFEMPTY_INT: transmit FIFO empty interrupt flag 0: Not transmit FIFO empty interrupt 1: Transmit FIFO empty interrupt	W/R
Bit2		TFTRIG_INT: transmit FIFO trigger interrupt flag 0: Not transmit FIFO trigger interrupt 1: Transmit FIFO trigger interrupt	W/R

Bit1		RXOVT_INT: receive FIFO overtime interrupt flag 0: Not transmit FIFO overtime interrupt 1: Transmit FIFO overtime interrupt	W/R
Bit0	0	RFTRIG_INT: receive FIFO trigger interrupt flag 0: Not transmit FIFO trigger interrupt 1: Transmit FIFO trigger interrupt	W/R

7.2.11 TFCNT Slave UART Transmit FIFO Counter Register: (PAGE0: 1001)

Bit	Rst	Function Description	Type
Bit7--0	00000000	slave UART transmit FIFO counter	R

7.2.12 RFCNT Slave UART Receive FIFO Counter Register: (PAGE0: 1010)

Bit	Rst	Function Description	Type
Bit7--0	00000000	slave UART receive FIFO counter	R

7.2.13 FSR Slave UART FIFO Status Register: (PAGE0: 1011)

Bit	Rst	Function Description	Type
Bit7	0	RFOE: there is overflow error byte in receive FIFO 0: Not OE error 1: OE error	R
Bit6	0	RFBI: there is break error byte in receive FIFO 0: Not Line-Break error 1: Line-Break error (Rx signal has zero state, including parity and stop bit)	W/R
Bit5	0	RFFE: there is frame error byte in receive FIFO 0: Not FE error 1: FE error	W/R
Bit4	0	RFPE: there is parity error byte in receive FIFO 0: Not PE error 1: PE error	W/R
Bit3	0	RDAT: slave UART receive FIFO empty flag 0: Receive FIFO empty 1: Receive FIFO not empty	W/R
Bit2	0	TDAT: slave UART transmit FIFO empty flag 0: Transmit FIFO empty 1: Transmit FIFO not empty	W/R
Bit1	0	TFULL: slave UART transmit FIFO full flag 0: Transmit FIFO not full 1: Transmit FIFO full	W/R
Bit0	0	TBUSY: slave UART transmit TX busy flag 0: Transmit TX not busy 1: Transmit TX busy	W/R

7.2.14 LSR Slave UART Receive Status Register: (PAGE0: 1100)

Bit	Rst	Function Description	Type
Bit7--4	0	RSV (reserved)	R
Bit3	0	OE: the reading data is overflow error 0: Not OE error 1: OE error	R
Bit2	0	BI: the reading data is break error 0: Not Line-Break error 1: Line-Break error(Rx signal has zero state, including parity and stop bit)	R
Bit1	0	FE: the reading data is frame error	R

		0: Not FE error 1: FE error	
Bit0	0	PE: the reading data is parity error 0: Not PE error 1: PE error	R

7.2.15 FDAT Slave UART FIFO Data Register: (PAGE0: 1101)

Bit	Rst	Function Description	Type
Bit7--0	00000000	Writer transmit FIFO data or read receive FIFO data	W/R

7.2.16 BAUD1 Slave UART Baud Rate Configuration Register High Byte: (PAGE1: 0100)

Bit	Rst	Function Description	Type
Bit7--0	00000000	BAUD[15:8]: slave UART baud rate configuration register high byte	W/R

7.2.17 BAUD0 Slave UART Baud Rate Configuration Register Low Byte: (PAGE1: 0101)

Bit	Rst	Function Description	Type
Bit7--0	00000000	BAUD[7:0]: slave UART baud rate configuration register low byte	W/R

7.2.18 PRES Slave UART Baud Rate Configuration Register Fractional Part: (PAGE1: 0110)

Bit	Rst	Function Description	Type
Bit7--4	0000	RSV	R
Bit3--0	0000	PRES[3:0]	W/R

7.2.19 RFTL Slave UART Receive FIFO Trigger Interrupt Register: (PAGE1: 0111)

Bit	Rst	Function Description	Type
Bit7--0	00000000	Receive FIFO trigger level	W/R

7.2.20 TFTL Slave UART Transmit FIFO Trigger Interrupt Register: (PAGE1: 1000)

Bit	Rst	Function Description	Type
Bit7--0	00000000	Transmit FIFO trigger level	W/R

8. Global Function Description

8.1 Reset

WK2124 is low reset.

The reset value of each register see Table 7.2 listed in the register.

During reset and after reset, each slave UART is disabled receiving and transmitting states. When the slave UART is in networking mode, this feature makes that the slave UART located on the nodes will not interfere other nodes in the network during the power-up and reset.

Each slave UART can be implemented independently software reset.

8.2 Clock Selection

WK2124 can choose to use chip oscillator clock as the clock source. Note: you need to shunt crystal and start resistance of 1M. Follow as figure 8.2.

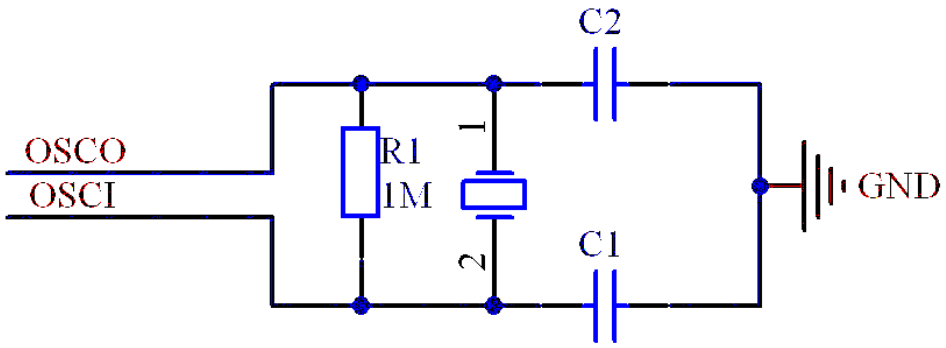


Figure 8.2 WK2124 Clock Circuit

8.3 Interrupt Control

WK2124 has two interrupt: slave UART interrupt and global interrupt. When the IRQ pin indicates an interruption, we can read GIFR global interrupt register to determine the current interrupt type, and then read the interrupt status register to determine the current interrupt source.

WK2124 interrupt structure is shown as below:

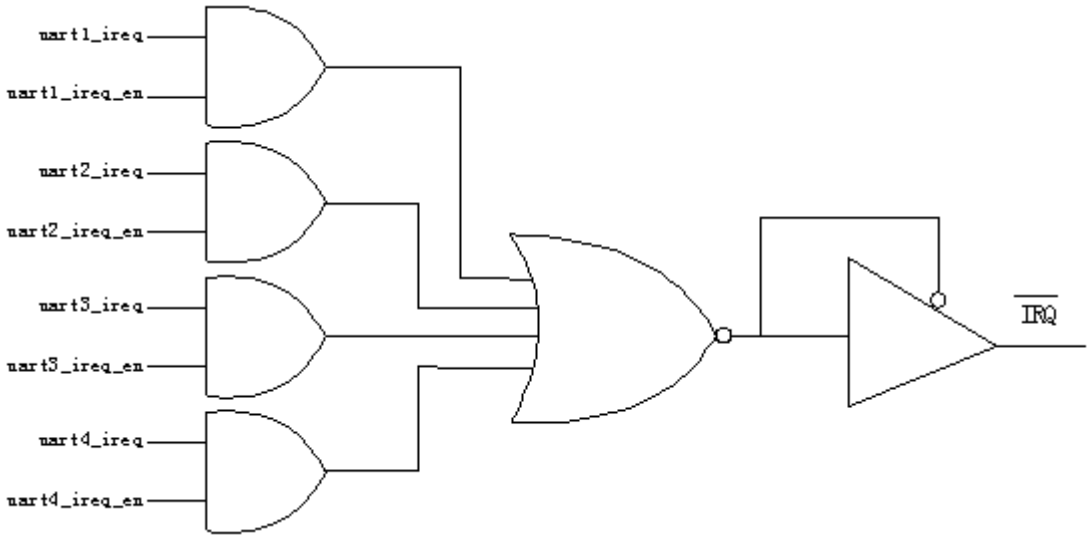


Figure 8.3 WK2124 Interrupt Structure Diagram

WK2124 each slave UART has an independent interrupt system, including FIFO data error interrupt, transmit FIFO empty interrupt, transmit FIFO trigger interrupt, receive FIFO timeout interrupt, receive FIFO trigger interrupt.

When any one of the interrupt is enabled and meets the interrupt condition, the corresponding interrupt is generated.

8.3.1 FIFO Data Error Interrupt

FIFO data error interrupt indicates that the current receiving FIFO has one or more data errors. Error conditions include OE(overflow error), FE(framing error), PE(parity error), BE(Line-Break error).

Once the receiver FIFO has data error, the interrupt will disappear when reading FSR

register. We can clear the interrupt by clearing the error data.

8.3.2 Transmitting FIFO Empty Interrupt

When there is no data in the transmitting FIFO, the interrupt is generated. When the number of data in the transmitting FIFO is larger than the setting transmit FIFO trigger, the interrupt is cleared.

8.3.3 Transmitting FIFO Trigger Interrupt

When the number of data in the transmitting FIFO is less than the setting transmit FIFO trigger, the interrupt is generated. When the number of data in the transmitting FIFO is larger than the setting transmit FIFO trigger, the interrupt is cleared.

8.3.4 Receiving FIFO Overtime Interrupt

When the number of data in the receiving FIFO is less than the setting receiving FIFO trigger and there is no data in the 4 bytes of RX pin, the interrupt is generated. When the data in the receiving FIFO is read away or RX continue to receive data, the interrupt disappears.

8.3.5 Receiving FIFO Trigger Interrupt

When the number of data in the receiving FIFO is lager than the setting transmit FIFO trigger, the interrupt is generated. When the number of data in the receiving FIFO is less than the setting transmit FIFO trigger, the interrupt is cleared.

8.4 Infrared Mode Operation

WK2124 main UART and slave UART can be set to the infrared communication mode. When the WK2124 UART is set to the IrDA mode, it can communicate with devices in line with the SIR infrared communication protocol standards or applied directly to the optical isolation communications.

In IrDA mode, a data cycle is shorted to an ordinary UART data 3/16, pulse less than 1/16 potter cycle will be look as interference and ignored.

8.4.1 Infrared Receiver Operation

The corresponding figure of infrared data reception timing and ordinary UART data reception is shown in figure 8.4.1: IRX is the received infrared data signal, RX is the decoded data via infrared data. Decoded data and data on the IRX has a BIT (16xCLOCK) delay. In receive mode, RX is different from ordinary UART. It has one sample in the middle of pulse (the difference between the ordinary UART of 3 times sample). IrDA decoder decodes 3/16 potter cycle pulse on IRX to the data 0 and continued low level to data 1.

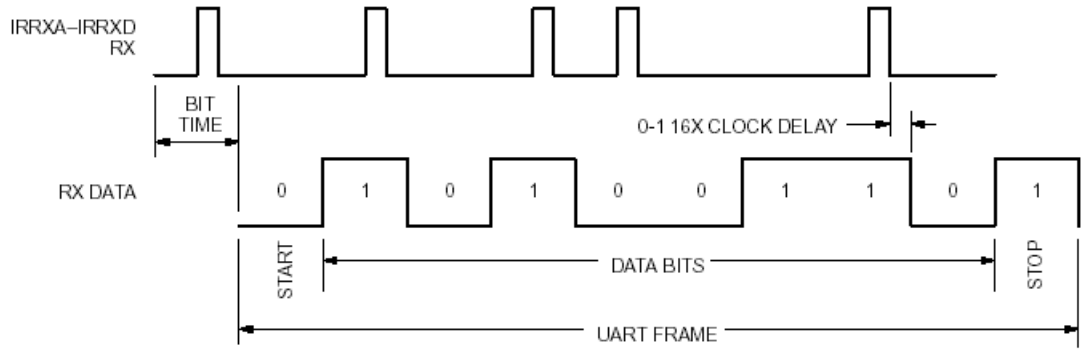


Figure 8.4.1 Infrared Receiver Timing

8.4.2 Infrared Transmission Operation

The corresponding figure of infrared data transmission and ordinary UART data transmission is shown in figure 8.4.2: TX is the ordinary UART data transmission timing, IRTX is the infrared transmission timing.When transmitting data 0, the infrared encoder will produce a 3/16 bit-wide pulse sent through the TX.When transmitting data 0, it remains low unchanged.

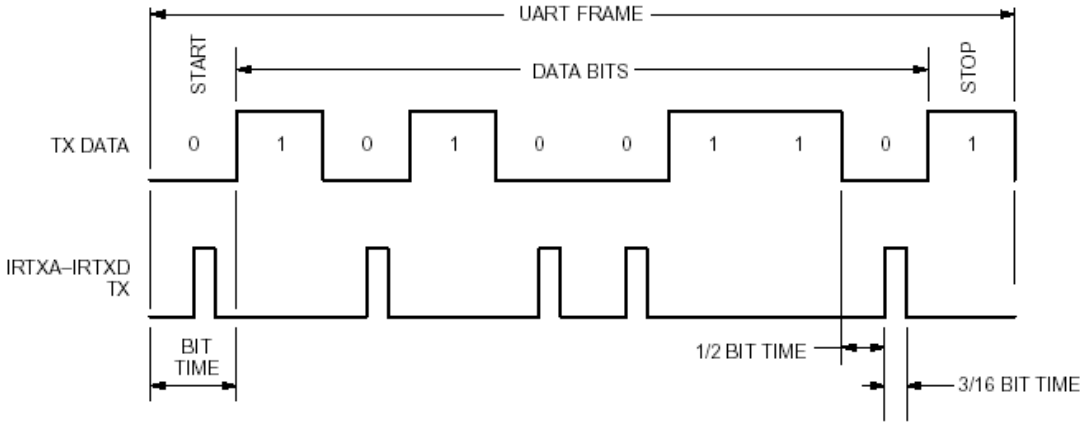


Figure 8.4.2 Infrared Transmission Timing

8.5 Programmable Baud Rate Generator

WK2124 main UART and slave UART use the same independent programmable baud rate generator. The baud rate generator produce division factor of 16X system clock. The division factor can be set by software.

8.5.1 Common Baud Rate and Crystal Table

The following table gives a different system clock frequency of the serial port baud rate setting table:

Table 8.5.1

BAUD BAUD[15-0]	PRES	BAUD RATE Fosc= 1.8432MHz	BAUD RATE Fosc= 3.6864MHz	BAUD RATE Fosc= 7.3728MHz	BAUD RATE Fosc= 11.0592MHz	BAUD RATE Fosc= 14.7456MHz
0X0002	0X00	38400	76800	153600	230400	307200
0X0005	0X00	19200	38400	78600	115200	153600
0X000b	0X00	9600	19200	38400	57600	76800
0X0017	0X00	4800	9600	19200	28800	38400
0X002f	0X00	2400	4800	9600	14400	19200
0X005f	0X00	1200	2400	4800	7200	9600
0X00bf	0X00	600	1200	2400	3600	4800
0X017f	0X00	300	600	1200	1800	2400
0X0000	0X00	115200	230400	460800	691200	912600
0X0001	0X00	57600	115200	230400	345600	460800
0X0003	0X00	28800	57600	115200	172800	230400
0X0007	0X00	14400	28800	57600	86400	115200

0X000f	0X00	7200	14400	28800	43200	57600
0X001f	0X00	3600	7200	14400	21600	28800
0X003f	0X00	1800	3600	7200	10800	14400
0X007f	0X00	900	1800	3600	5400	7200

8.5.2 Any Crystal Baud Rate Calculation

The formula: f_s / (baud*16) = Reg

Note: f_s is the system clock, baud is baud rate to be set, Reg is calculation result(usually accurate to two decimal places)

Reg integer part minus one and converter into 16 hex written {BAUD1, BAUA0}, if there are fractional part, the fractional part is taking the first written PRES.

Example 1: f_s = 11.0592MHz, baud = 115200. According to the formula can get Reg=6. Then the filling registers of data: BAUD1 = 0X00; BAUD0 = 0X05; PRES = 0X00.

Example 2: f_s = 12MHz, baud = 115200. According to the formula can get Reg=6.51(accurate to two decimal places). Then the filling registers of data: BAUD1 = 0X00; BAUD0 = 0X05; PRES = 0X05.

Example 3: high baud rate calculation

BAUD BAUD[15-0]	PRES	BAUD RATE Fosc= 8MHz	BAUD RATE Fosc= 16MHz	BAUD RATE Fosc= 24MHz	BAUD RATE Fosc= 32MHz
0X0000	0X00	500K	1M	1.5M	2M
0X0001	0X00	250K	500K	750K	1M
0X0003	0X00	125K	250K	375K	500K

8.6 Data Formatting

8.6.1 Parity Mode

WK2124 UART can provide forcing parity, calculating parity and no parity data format. It sets by LCR(slave UART configuration register):

Forcing parity mode

WK2124 supports forcing 1 parity, forcing 0 parity and user-specified parity mode. In this mode, the parity setting affects only data transmission, data reception will ignore the parity check.

WK2124 supports always 1 parity, 0 parity, odd parity, even parity. In this mode, the parity setting affects both the transmitting and the receiving, the receiving data will be checked the parity bit according to the parity setting.

8.6.2 Data length

WK2124 support 1 bit or 2 bits stop mode, main UART set by GMUT.GSTPL, slave UART set by LCR.STPL.

8.7 Sleep and Auto Wake-up

WK2124 supports sleep and automatic wake-up mode and each slave UART can be set to sleep individually.

Sleep conditions: 1、SCR SLEEPEN=1

2、receiving and transmitting FIFO is empty.

3、there is no data receiving on the RX and transmitting on the TX.

4、slave UART has no any interrupt.

When the above conditions are satisfied and remain above state 4 bytes time, slave UART goes to sleep automatically. The clock of slave UART is stopped and the lowest power will be consumed. At this time, whether the slave UART into sleep state determined by reading GRST.

When the slave UART goes to sleep and satisfy one of the following conditions, sleeping slave UART can wake up automatically. At this time, whether the slave UART wake-up determined by reading GRST.

Wake-up conditions: 1、RX begains to receive data.

2、transmitting FIFO write data to slave UART.

3、CTS pin level change

8.8 FIFO Trigger Setting

WK2124 support that each slave UART is set to the different trigger point. The receiving and transmitting FIFO can be independently set different trigger points. There are two methods of setting trigger point: 1、Configuring fixed point: by FCR register TFTRIG[1:0] and RFTRIG[1:0] bits fixed programming to configure the trigger position. 2、Configuring any trigger: by setting TFTL and RFTL of the two registers to set any trigger position. Specific configuration shown in Table 8.8.1:

TFTL [7:0]	TFTRIG [1:0]		TX Trigger Level	RFTL [7:0]	RFTRIG [1:0]		RX Trigger Level
= =0	0	0	8	= =0	0	0	8
= =0	0	1	16	= =0	0	1	16
= =0	1	0	24	= =0	1	0	24
= =0	1	1	30	= =0	1	1	28
! =0	X	X	TFTL	! =0	X	X	RFTL

Table 8.8.2:

RFTL[7:0]	FCR[5:4] RFTRIG[1:0]		接收中断触点值
= =0	0	0	8
= =0	0	1	16
= =0	1	0	24
= =0	1	1	28
! =0	X	X	RFTL

9. SPI Interface Mode Operation

9.1 SPI Connect With Host

As shown in Figure 9.1, SPI interface consists the following four signals:

SDIN: SPI slave device data input(MOSI).

SDOUT: SPI slave device data output(MISO).

SCLK: SPI serial clock.

SCS: SPI chip selection (slave select SSEL).

WK2124 connection with the host is shown in Figure 9.1.

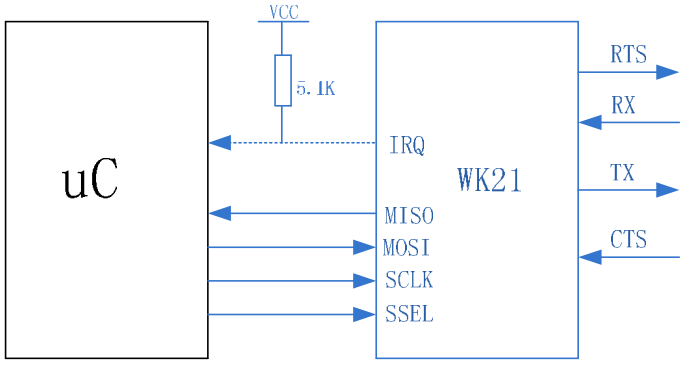


Figure 9.1 The Connection Diagram of SPI and Host

9.2 SPI Interface Operation Timing

WK2124 work in slave mode of the SPI synchronous serial communication, supports SPI mode 0 standard. In order to achieve the communication of host and WK2124, it needs to set CPOL=0(SPI clock polarity selection bit) and CPHA=0(SPI clock phase selection bit) on the host side.

The operation timing of WK2124 SPI interface shows as follow:

The operation timing of write register shows as Figure 9.2: at first, write a command byte, and then write the corresponding data byte. The register address of data byte is automatically incremented.

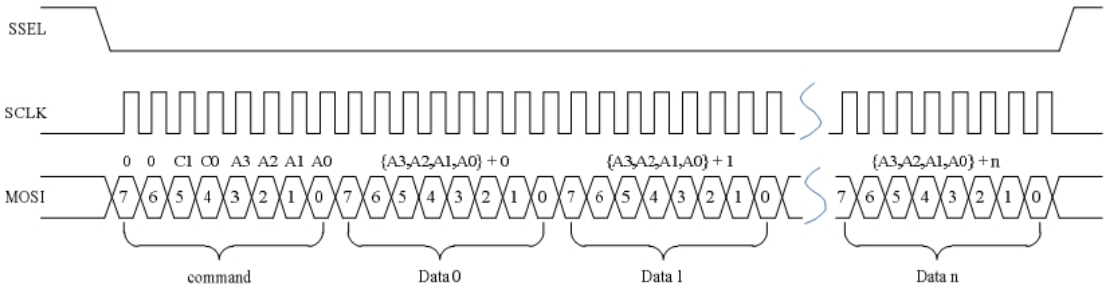


Figure 9.2 SPI Write Register Timing Diagram

Read register operation timing is shown as 9.3: at first, write a command byte, and then chip MISO line will return the corresponding data bytes. The register address of returning data type is automatically incremented.

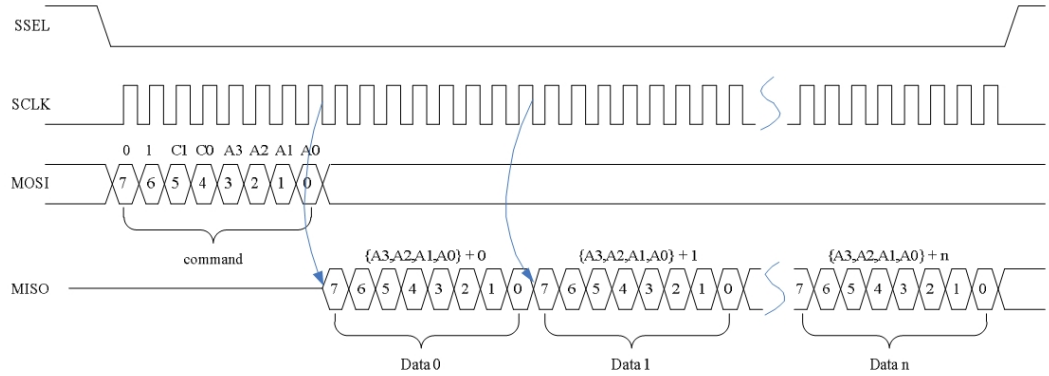


Figure 9.3 SPI Read Register Timing Diagram

Write FIFO operation timing is shown as 9.4: at first write a command byte, and then write the corresponding data byte. FIFO address is automatically incremented.

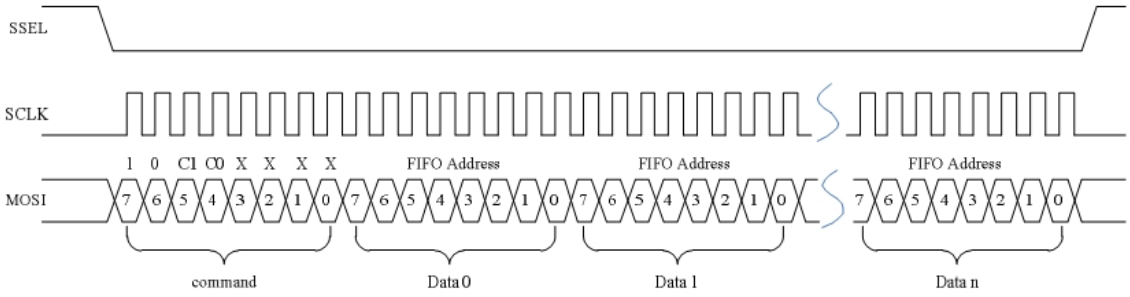


Figure 9.4 SPI Write FIFO Timing Diagram

Read FIFO operation timing is shown as 9.5: at first, write a command type, and then chip MISO line will return the corresponding data bytes. The FIFO address is automatically incremented.

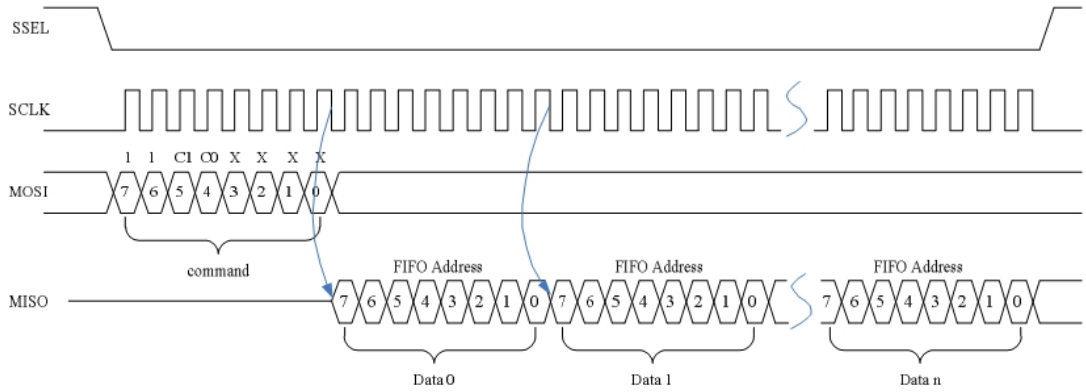


Figure 9.5 SPI Read FIFO Timing Diagram

9.3 SPI Bus Communication Protocol Description

9.3.1 SPI Write Register

SPI	Command Byte								Write N Bytes Data Address increment Automatically							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MOSI	0	0	C1	C0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
MISO	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz

9.3.2 SPI Read Register

SPI	Command Byte								Read N Bytes Data Address increment Automatically							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MOSI	0	1	C1	C0	A3	A2	A1	A0	X	X	X	X	X	X	X	X
MISO	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz	D7	D6	D5	D4	D3	D2	D1	D0

9.3.3 SPI Write FIFO

SPI	Command Byte								Write N Bytes Data to {C1,C0} FIFO							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MOSI	1	0	C1	C0	X	X	X	X	D7	D6	D5	D4	D3	D2	D1	D0
MISO	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz

9.3.4 SPI Read FIFO

SPI	Command Byte								Read N Bytes Data from {C1,C0} FIFO							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MOSI	1	1	C1	C0	A3	A2	A1	A0	X	X	X	X	X	X	X	X
MISO	Hz	Hz	Hz	Hz	Hz	Hz	Hz	Hz	D7	D6	D5	D4	D3	D2	D1	D0

Explanation:

C1 C0: slave UART channel number 00~11: slave UART 1 to 4

A3-A0: slave UART register address

D7…D0: 8 bits data type

10. Slave UART Operation Description

10.1 Slave UART Enable/Disable

WK2124 allow to independent enable/disable every slave UART channel.

It can disable the no using of slave UART during using.

Slave UART channel can receive and transmit data only in enabled state.

10.2 Receive and Transmit FIFO Control

WK2124 provide independent 256 FIFO receive and transmit FIFO.

10.2.1 Transmit FIFO Trigger Operation

WK2124 provide independent programmable transmit FIFO trigger setting for each channel to generate a corresponding transmit FIFO trigger interruption. When the transmit FIFO trigger interrupt is enabled and the data number in the transmit FIFO is less than the trigger point, it generates the corresponding interrupt.

10.2.2 Receive FIFO Trigger Operation

WK2124 provide independent programmable receive FIFO trigger setting for each channel to generate a corresponding receive FIFO trigger interruption. When the receive FIFO trigger interrupt is enabled and the data number in the transmit FIFO is larger than the trigger point, it generates the corresponding interrupt.

10.2.3 Transmit FIFO Enable/Disable

After the rest, the transmit FIFO is stationary. If you want to write data to transmit FIFO, you need to enable transmit FIFO.

Whether transmit FIFO data transmit or not, it depends on the corresponding sub-channel UART enabled. Once the corresponding sub-channel UART is enabled, the data in the transmit FIFO will be sent immediately. Otherwise, the data in the transmit FIFO will not be sent to the corresponding sub-channel enabled.

10.2.4 Receive FIFO Enable/Disable

After the rest, the receive FIFO is stationary. If you want to receive slave UART data, you need to enable the corresponding sub-channel and receive FIFO. Only the corresponding UART and receive FIFO is enabled, the received data can be written to the receive FIFO memory.

If sub-channel enable and receive FIFO disabled, the slave UART can receive data, but the data is not written to receive FIFO and is ignored.

10.2.5 Transmit FIFO Empty

When the FCR in the transmit FIFO empty (TFRST) is set to 1, the data of the sub-channel transmit FIFO will be cleared. Transmit FIFO counters and pointers will be cleared.

TFRST bit is set to 1 and it will be automatically cleared by hardware after one clock.

10.2.6 Receive FIFO Empty

When the FCR in the receive FIFO empty (RFRST) is set to 1, the data of the sub-channel receive FIFO will be cleared. Receive FIFO counters and pointers will be cleared.

RFRST bit is set to 1 and it will be automatically cleared by hardware after one clock.

10.2.7 Transmit FIFO Counter

WK2124 uses an 8-bit register to reflect the number data of currently transmit FIFO. When one byte of data writes to transmit FIFO, the transmit FIFO counter is automatically incremented by 1. When a transmit FIFO data is transmitted, the transmit FIFO counter is automatically decremented by 1.

Note: When transmit FIFO counter is 255(11111111) and if we write a data, the counter changes to 0(00000000). When transmit FIFO counter is 1(00000001), the counter changes to 0(00000000) after transmitting a data. Therefore, when transmit FIFO counter is 0, it indicates that transmit FIFO is full or empty. In this case, it need to combine the associated status bit of slave UART status register (FSR) to judge.

10.2.8 Receive FIFO Counter

WK2124 uses an 8-bit register to reflect the number data of currently receive FIFO. When one byte of data writes to receive FIFO, the receive FIFO counter is automatically incremented by 1. When a receive FIFO data is received, the receive FIFO counter is automatically decremented by 1.

Note: When receive FIFO counter is 255(11111111) and if we receive a data, the counter changes to 0(00000000). When receive FIFO counter is 1(00000001), the counter changes to 0(00000000) after reading a data. Therefore, when receive FIFO counter is 0, it indicates that receive FIFO is full or empty. In this case, it need to combine the associated status bit of slave UART status register (FSR) to judge.

11. Parameter Index

11.1 WK2124 Static Parameter

Unless otherwise specified, meet: VCC=(2.5V±0.2V) or (3.3V±0.3V) or (5V); -40℃ ~ +85℃.

Symbol	Description	Condition	VCC=2.5V		VCC=3.0V		VCC=5.0V		Unit
			Min	Max	Min	Max	Min	Max	

Power supply									
VCC	voltage		2.3	2.7	3.0	3.6	4.5	5.0	V
ICC	working current	3.6864MHz crystal no load	0.8	2	1	2	2	3	mA
ICCSL	sleep current		150	-	200	-	460	-	uA
Input logic signal									
VIH	input high		1.8	5.0	2.0	5.0	3.6	5.0	V
VIL	input low		-	0.6	-	0.9	-	1.1	V
IIL	input leakage current	VI=5.0 or 0V	-	±10	-	±10	-	±10	uA
CI	input capacity		-	5	-	5	-	5	pF
Output logic signal									
VOH	output high	IOH=3mA	1.9	-	2.4	-	4.5	-	V
VOL	output low	IOL=3mA	-	0.4	-	0.4	0	0.4	V
IOL	output leakage current		-	±10	-	±10	-	±10	uA
CO	output capacity		-	5	-	5	-	5	pF

11.2 WK2124 Dynamic Parameter

Symbol	Description	Condition	VCC=2.5V		VCC=3.0V		VCC=5.0V		Unit
			Min	Max	Min	Max	Min	Max	
FOSI	Crystal frequency		-	16	-	24	-	32	MHz

11.3 WK2124 Limit Parameter

Symbol	Description	Condition	Min	Max	Unit
VCC	voltage		-0.5	5	V
VI	input voltage		-0.5	+5.5	V
VO	output voltage		-0.5	+5.5	V
PTOL	total power consumption		-	300	mW
TO	operating temperature		-40	+85	℃
TSTG	storage temperature		-65	+150	℃

12. Package Information

尺寸 / 标注	最小（mm）	最大（mm）	尺寸 / 标注	最小（mm）	最大（mm）
A	7.15	7.25	C3	0.152	
A1	0.30TYP		C4	0.172	
A2	0.65TYP		H	0.05	0.25
A3	0.525TYP		θ	12° TYP4	
B	5.25	5.35	θ1	12° TYP4	
B1	7.65	7.95	θ2	10° TYP	
B2	0.60	0.80	θ3	0° ～ 8°	
C	1.45	1.55	R	0.20TYP	
C1	1.65	1.85	R1	0.15TYP	

C2	0.674		

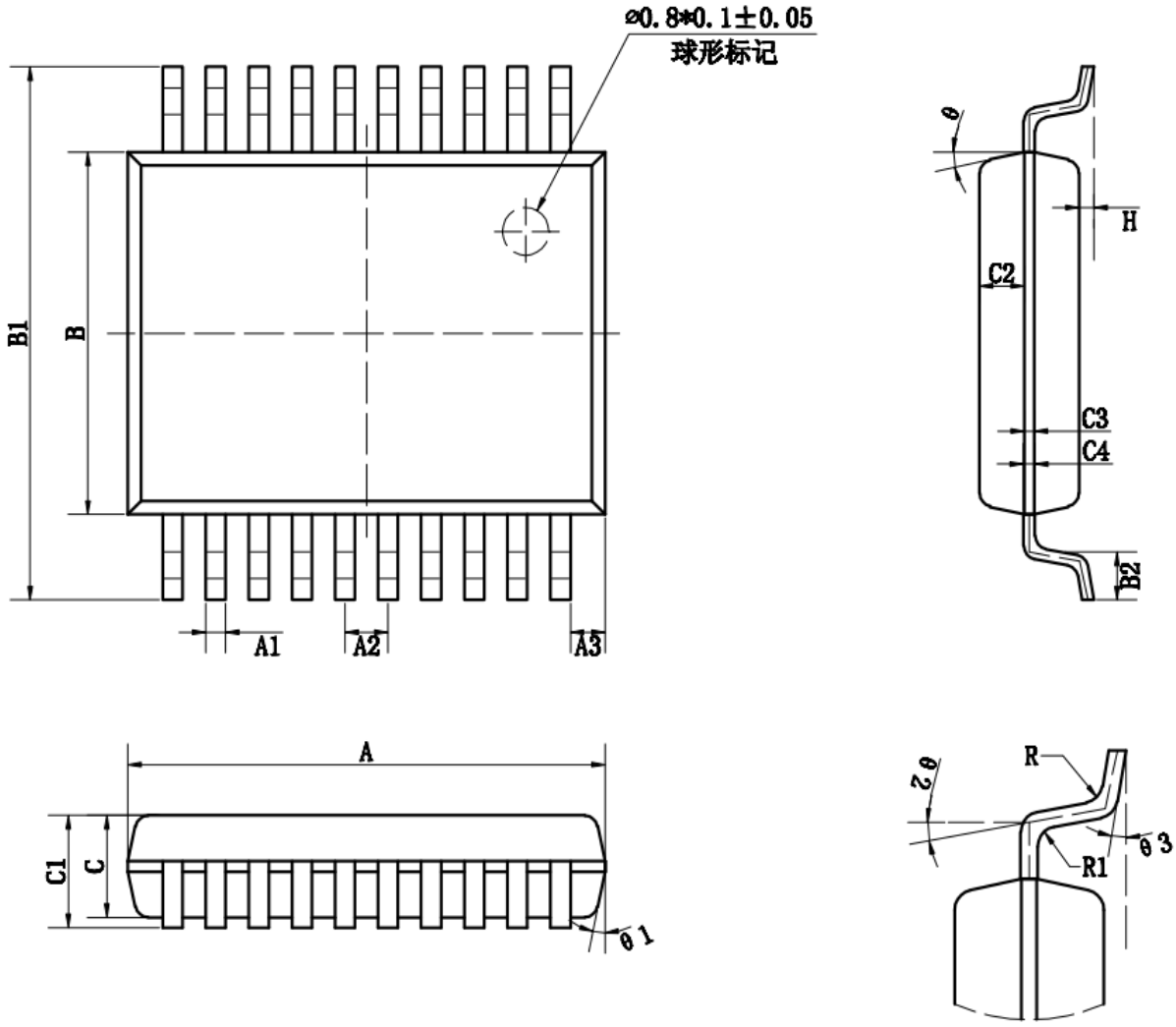


Figure 12.1 SSOP20 Package Information

13. Welding Process

This product uses green materials, the pin using pure tin plating. The recommended peak temperature is less than 260℃, in line with lead-free reflow process welding.

SMD devices, welding processes are sensitive to temperature, it is recommended to be dried before welding.

O`clock by hand welding is adopted, should be first of all welding the pin of the two diagonal to carried out the fixed and then welding other pins, welding temperature is 300℃, soldering iron and pin contact time control within 10 seconds.

14. Special Statement

This product is not for the life support system. Aerospace systems design, this product is applied to the field of all the consequences arising from Weikai Microelectronic will not accept

any responsibility. Weikai Microelectronic to retain the performance of the product, modify, parameters modify the right to the Weikai Microelectronic make changes for the mass production of products, will be the announcement notice user.

15. Version History

The version before V1.1 was internal version that was informally public.

16. Contact Information

Please visit Weikai Microelectronic website to get the latest contact information: www.wkmic.com.