

Bluetooth Low Energy (BLE) Transparent Transmission Controller Programming User Guide

BC7601/BC7602/BC32F7611

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Introduction

Overview

The series of BLE devices discussed in this guide are Holtek's fully integrated single chip Bluetooth Low Energy transparent transmission controllers. The devices require a patch code to activate the BLE function for full BLE optimization. This patch code can be downloaded from an EEPROM or MCU for which the patch source can be selected by the IIC_SDA line status during the reset period. The patch interface can also be selected to be the UART or SPI interface determined by the SPI-UR_N line status during the reset period. The IIC_SDA and SPI-UR_N line level will be detected after the reset has completed. Therefore these two lines should be fixed at a certain level before the RST_N line goes high.

As these two lines selections are independent, there will be four patch modes as shown in the following table.

Patch Mode	Patch Code Description
Mode_A	Patch from the MCU using the SPI interface – 8K patch code memory capacity
Mode_B	Patch from the EEPROM using the SPI interface
Mode_C	Patch from the MCU using the UART interface – 8K patch code memory capacity
Mode_D	Patch from the EEPROM using the UART interface

Device Summary

The supported mode types is dependent upon which device is selected as shown in the following table.

Patch Mode Device	Mode_A	Mode_B	Mode_C	Mode_D
BC7601	\checkmark	—	√	—
BC7602		\checkmark		\checkmark
BC32F7611		_	_	—

Pin Description

Name	Direction	Level	Description
RST_N	Input	0: Reset 1: Not reset	
PDN	Input	0: Power down 1: Not power down	If the PDN pin state is changed from low to high, it is necessary to reset the device and patch again.
IIC_CLK	Input/ Output	1: Baud rate=115200 0: Baud rate=9600	In Mode_C, IIC_CLK pin is used to select the default baud rate. The IIC_CLK pin level should be fixed during a reset as it will be checked after the reset.
EE_WP	Output	0: EEPROM Write Protect Disable 1: EEPROM Write Protect Enable	Used for an EEPROM write protect. The MCU should not change the EE_WP pin level.
IIC_SDA	Input/ Output	0: Patch from MCU Pull-high resistor contained in EEPROM: Patch from EEPROM	The device will check the EEPROM after a reset.
STATE	Output	0: Device sleep 1: Device active	Device state indicator
INT_EXT	Output	0: Valid data ready 1: No data ready	SPI interrupt – software
SPI_INT	Output	0: Data valid 1: No data valid	SPI interrupt – hardware

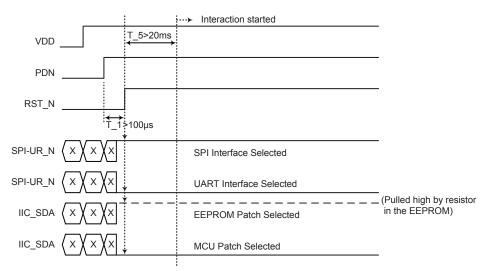


Name	Direction	Level	Description
WAKEUP	Input	0: Enter Sleep mode 1: Wake up the device (delay<3ms)	MCU controls the WAKEUP pin WAKEUP=1 \rightarrow STATE=1 when active
SPI-UR_N	Input	0: UART interface 1: SPI interface	Pin level should be fixed during a reset and checked after the reset
SPI_MOSI /UART_RXD	SPI/UART	SPI/UART	
SPI_MISO /UART_TXD	SPI/UART	SPI/UART	Patch interface selected by SPI-UR_N If the SPI-UR_N pin is pulled high the SPI interface
SPI_CS /UART_CTS	SPI/UART	SPI/UART	pins are selected. If the SPI-UR_N pin is pulled low the UART interface pins are selected.
SPI_CLK /UART_RTS	SPI/UART	SPI/UART	······································

Pin Functional Description

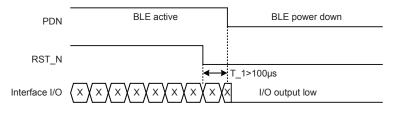
Reset Pin – RST_N

The RST_N pin must be kept low for a time period greater than 100µs after the PDN pin is set high when a power-on reset occurs. Then the device can boot from the EEPROM or MCU by reading a patch code using the SPI or UART interface. After a boot time period, denoted as T_5 in the following diagram and greater than 20 ms, then interaction can be initiated between the MCU and BLE device.



Power Down Control Pin – PDN

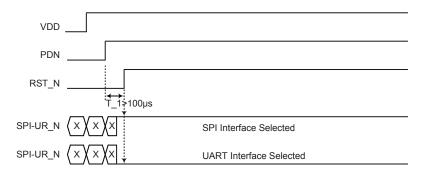
If the PDN pin is cleared to low the device will enter the power down mode. The RST_N and all interface I/O pins must be cleared to low. The Interface I/O includes the SPI_CS/UR_CTS, SPI_CLK/UR_RTS, SPI_MOSI/UR_RXD and SPI_MISO/UR_TXD lines.





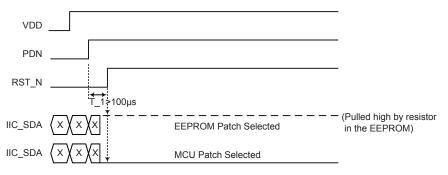
Interface Select Pin – SPI-UR_N

The SPI-UR_N pin is used to select which interface is used for data transfer. The SPI-UR_N pin status will be checked after a reset after which the interface selected can be determined. If the SPI-UR_N pin status is high the SPI interface will be selected while the UART interface will be selected if the SPI-UR_N pin status is low.



IIC_SDA Pin

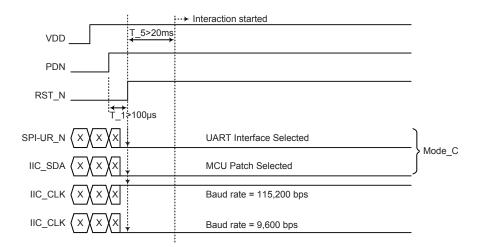
A patch code can be sourced from either the EEPROM or MCU, which is selected by the IIC_SDA line status during the reset period. If the IIC_SDA line is externally fixed to low during the reset period, the patch code will be derived from the MCU after the reset completes. However the patch code will be sourced from the EEPROM after the reset completes if the IIC_SDA line is connected to the EEPROM SDA pin and pulled high by a resistor contained within the EEPROM.



IIC_CLK Pin

The IIC_CLK pin is used to select the default baud rate when the device operates in Mode_C, which means the patch code is derived from the MCU using the UART interface. The UART default baud rate is equal to 115,200 bps when the IIC_CLK pin status is set high. Otherwise, the UART default baud rate is equal to 9,600 bps as the IIC_CLK pin status is set low.





EEPROM Write Protect Control Pin – EE_WP

The EE_WP pin is the EEPROM write protect control pin which is use to control the EEPROM write protect function and only available for the device which is patched from the EEPROM memory. This pin should be kept in a floating status and also the host MCU should not change the pin status for devices patched from the MCU.

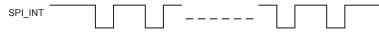
IC State Indicator Pin – STATE

The STATE pin is used to indicate that the device is in the operating or sleep mode. The external host MCU can read this pin status to know the BLE device condition. When the STATE pin status is high this indicates that the device is active while if the STATE pin status is low this indicates that the device is in the sleep mode.



SPI Interrupt Pin – SPI_INT

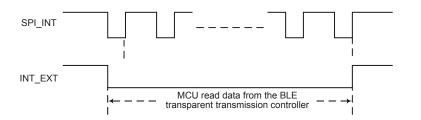
The SPI_INT line signal is used to inform the MCU that data in the SPI buffer is available. The corresponding interrupt enable control bit in the control register, CR2, should first be set high before the SPI_INT signal is used. The MCU can obtain data from the BLE transparent transmission controller when the MCU receives an SPI_INT active signal. The BLE transparent transmission controller will generate a valid trigger signal on the SPI_INT line once data in the buffer is available.



External Interrupt Pin – INT_EXT

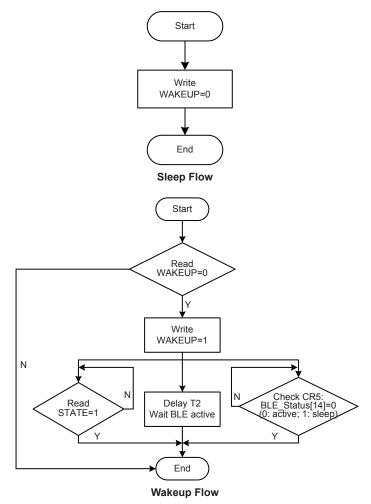
The INT_EXT line signal is used to inform the MCU that data is available. The MCU can obtain data from the BLE transparent transmission controller when the MCU receives an INT_EXT active signal. The INT_EXT active level can be determined by configuring the accessible physical address 0x0020_0494[1]. The BLE transparent transmission controller will keep the INT_EXT line at an active level until there is no more available data in the buffer.





Wake-up Pin – WAKEUP

The WAKEUP pin is used to select the device operation mode while the STATE pin is used to indicate the device operation status. The external host MCU can check the device operation mode by monitoring the STATE pin. When the WAKEUP pin is pulled low, the device will enter the Sleep mode and the STATE pin will go low. If the device is in the Sleep Mode, it can be woken up using the WAKEUP pin. When the WAKEUP pin is pulled high, the device will be woken up and the STATE pin will go high.

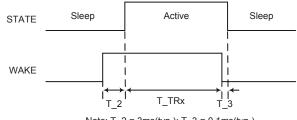




Host Start Interaction

When the host MCU sets the WAKEUP pin high, the device will set the STATE pin high after a delay time, T_2, as shown in the following diagram. After this the BLE device will be in the active mode. The host MCU can read the BLE status register, CR5, bit 14 to check that the BLE device is in the sleep or active mode when using the SPI interface. It is recommended that the host MCU should wait for a delay time, T_2, greater than 3 ms when using the UART interface. When the device is in the active mode, the host MCU can transmit or receive packets.

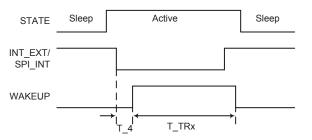
The packet will be ignored if the host MCU send a packet when the BLE device is in the sleep mode. If the host MCU sends packets during the T_2 delay time period, the BLE device will respond with a value of 26FF1C to the host to indicate that the packet type is not supported or with other error messages. After the interaction has completed the host MCU should clear the WAKEUP pin low to inform the BLE device to enter the sleep mode again.



Note: $T_2 = 3ms(typ.); T_3 = 0.1ms(typ.)$

BLE Start Interaction

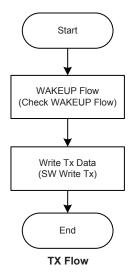
If the BLE device wishes to send packet to the external host, the BLE device should first wait until the STATE pin goes high which means that the BLE device is in the active mode. The BLE device should send an INT_EXT or SPI_INT signal to inform the host MCU after the STATE pin goes high. The host MCU should first set the WAKEUP pin high to ensure that the packet can be transferred completely. After this the host MCU can transmit or receive packets when the BLE device is in the active mode. If the packet is transferred by the host MCU before setting the WAKEUP pin high, i.e. during the T_4 period, the BLE device will respond with an error message to the host MCU. After the interaction has completed the host MCU should set the WAKEUP pin low to inform the BLE device to enter the sleep mode again. Note that the INT_EXT signal active level can be determined by configuring the accessible physical address 0x0020_0494[1] while the SPI_INT signal is always active low.





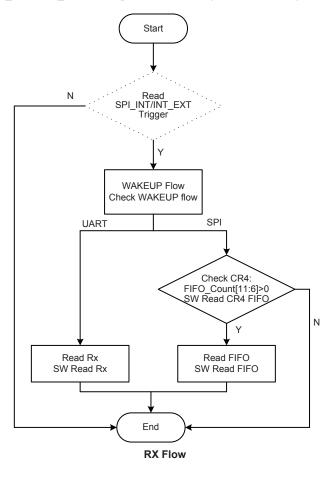
Transmission Flow – TX Flow

The MCU can transmit the Command or Payload to the BLE device using the corresponding format.



Reception Flow – RX Flow

The MCU can receive an Event or Payload from the BLE device using the corresponding format. Note that the SPI_INT/ INT_EXT check procedure can be ignored when using the UART interface.





BLE Device Command / Event

The BLE device supports several commands and events for communication with the host MCU. Some GATT services are also supported to communicate with cell phones. To more conveniently describe the command/event format several abbreviations are used which are listed in the following table.

Abbreviation	Explanation
BD	Bluetooth Device
BD_Addr	Bluetooth Device Address
BD_Name	Bluetooth Device Name

Abbreviation Summary

GATT Service Description

The BLE device supports two types of service for the communication with cell phones. The cell phone can access these services using the BLE protocol.

Service	Characteristics	Property	Data Type	Data Length	Description
Battery (UUID 0x180F)	Battery Level (UUID 0x2A19)	Read / Notify	8 bits	1 byte	Device Battery Level The cell phone sends a read command to the device after which the device battery level value will be sent to the cell phone.
Manufacture Define (UUID 0xFFF0)	Read (UUID 0xFFF1)	Notify	8 bits	20 bytes	Payload sent from the BLE device to the cell phone. If the cell phone enables the device "Notify" function, the BLE device will send the payload to the cell phone whenever the data is ready.
	Write (UUID 0xFFF2)	Write without Response	8 bits	20 bytes	Payload is sent from the cell phone to the BLE device without waiting for a device acknowledge.

Command (Cmd) / Event (Evt) Format

Both commands and events are supported by the BLE device to communicate with the host MCU. The write commands are used to configure the BLE device by the host MCU while the read commands are used to retrieve the information from the BLE device. The corresponding events are the responses which are returned from the device to the host MCU.

Turno	Dir.	Header				Р	ayloa	d					
Туре		1 st	2 nd	3 rd	4 th	5 th	6 th	7 th	8 th	9 th	10 th		N th
Read Command	M→S	0x20	Opcode (byte*1)										
Read Event	M←S	0x21	Opcode (byte*1)	LengthData(byte*1)(byte*Length, MSB)									
Payload Packet Command	M⇔S	0x22	Length (byte*1 max=200)	RF Payload (byte*Length, MSB)									
Write Command	M→S	0x25	Opcode (byte*1, unit=byte*1)	Length Data (byte*1) (byte*Length, MSB)									
Write Event/ Payload Packet Event	M←S	0x26	Opcode (byte*1, unit=byte*1)	Result (byte*1)									



Turne	Dir.	Header	Payload											
Туре		1 st	2 nd	3 rd	4 th	5 th	6 th	7 th	8 th	9 th	10 th		N th	
Write Physical Address	M→S	0x55	Length (byte*1, unit=byte*4, max=60)	Reserv (byte*	(Add byte*4		8)	Data (byte*Length*4, LSB)					
Read Physical Address	M→S	0x56	Length (byte*1, unit=byte*4, max=60)	Address (byte*4)										
Read Physical Address Return	M←S	0x57	Length (byte*1, unit=byte*4, max=60)	Reserved (byte*2)						8)	Da (byte*Leng			LSB)

Note: 1. The "Dir." word means the transfer direction.

2. " $M \rightarrow S$ ": from Master to Slave;

"M←S": from Slave to Master;

"M \leftrightarrow S": both from Master to Slave and from Slave to Master;

where "M" is the MCU and "S" is the BLE device.

3. "Reserved" means 0x00.

Read Command (Cmd) / Event (Evt) Format

These commands are used to retrieve information from the device. The corresponding events are the information which is returned from the device to the host MCU.

	Header	Opcode	Length				Dat	a	-			
Read Cmd/Evt	1 st	2 nd	3 rd	4 th	5 th	6 th	7 th	8 th	9 th		N th	
IntvRead Cmd	0x20	0x30										
IntvRead Evt	0x21	0x30	0x04	Connection Interval (4 bytes, Unit: 1ms, Valid Range=8~4000, LSB)								
Description: Rea	ad connec	tion interva	al setting betwo	een the dev	vice and	cell ph	one. On	y availa	ble whe	en conne	ected.	
BDNameRead Cmd	0x20	0x31										
BDNameRead Evt	0x21	0x31	Length (up to 16 bytes)	BD_Name (up to 16 bytes, MSB)								
Description: Rea	ad Bluetoo	oth Device	Name									
BaudRateRead Cmd	0x20	0x32										
BaudRateRead Evt	0x21	0x32	0x04	0: 2 2: 1 4: 3	BaudR 4 bytes, 400 4400 8400 15200	LSB) 1: 9600 3: 1920 5: 5760	0 0					
Description: Rea	ad the UA	RT baudra	te. Only valid v	when using	the UA	RT inter	face.					
BDAddrRead Cmd	0x20	0x33										
BDAddrRead Evt	0x21	0x33	0x06	BD_Addr (6 bytes, public, LSB)								
Description: Rea	ad Bluetoo	oth Device	public Address	s								
AdvIntvRead Cmd	0x20	0x35										



	Header	Opcode	Length				Data	a				
Read Cmd/Evt	1 st	2 nd	3 rd	4 th	5 th	6 th	7 th	8 th	9 th		N th	
AdvIntvRead Evt	0x21	0x35	0x04	Adv Interval (4 bytes, Unit: 1 ms, Valid Range=20~10000, LSB)								
Description: Rea	ad Bluetoo	oth Device	Advertising Int	erval								
AdvDataRead Cmd	0x20	0x36										
AdvDataRead E∨t	0x21	0x36	Length (up to 25 bytes)	Adv Data (up to 25 bytes, manufacturer specific data field value, MSB)								
Description: Read manufacturer specific data field value of the advertising packet Ex: Advertising packet=020106_06FF04095E5F60 020106: 02: length=2 01: type=Flags 06: value=LE General Discoverable Mode/BR/EDR not supported 06FF04095E5F60: 06: length=6 FF: type=Manufacturer Specific Data 04095E5F60: value=(Adv Data)												
WhiteListRead Cmd	0x20	0x37										
WhiteListRead Evt	0x21	0x37	0x06	Conne		device a 6 bytes,		(white li	st)			
		the BLE d	alue. If the exte evice. If the W									
TxPowerRead Cmd	0x20	0x38										
TxPowerRead Evt	0x21	0x38	0x01	Pwr (1 byte) 0: 3dBm 1: 0dBm Others: Reserved								
Description: Rea	ad the BLE	E device R	F TX power se	tup value.								

Payload Format

The BLE device receives the payload stream from the host MCU with a length of up to 200 bytes. However, the whole payload stream received from the host MCU will be divided into several payload packets with each packet having a length of 27 bytes. These packets with a length of up to 27 bytes will be sent to the cell phone.



Payload Packet Cmd	Header	Length /Result				RF Pa	yload		<u>.</u>	
Cina	1 st	2 nd	3 rd	4 th	5 th	6 th	7 th	8 th		N th
Payload Packet Command	0x22	Length (up to 200 bytes)				RF Pa (MS				
Payload Packet Evt	Header	Opcode	Length /Result							
Evi	1 st	2 nd	3 rd							
Payload Packet Evt	0x26	0x22	Result 0: ok others: fail							
The BLE device air p packet with a length several packets with phone. Finally the de received. Example: The MCU phone.	greater that each air pa evice will se	in 27 bytes, t ayload packe and an event	he device wil et having a ler packet mess	l automa ngth of 2 age to th	atically p 7 bytes ne host l	artition t and the MCU aft	he whol n send t er all pa	e pay hese yload	load stream ir packets to the packets have	e cell been
MCU		UART/SPI (wired)		В	LE Devi	ce	-		BLE packet (air)	Cell Phone
22_32_6162636465 6A6B6C6D6E6F707 75767778797A7B70 7F80818283848586 898A8B8C8D8E8F9	71727374 C7D7E 8788	→								
			(Header: 7bytes) + 6162636465666768696A6B6C6D6E → 6F7071727374							
			75767778797A7B7C7D7E 7F808182838485868788 898A8B8C8D8E8F							
			909192						\rightarrow	
		←	262200							



Write Command (Cmd) / Event (Evt) Format

These commands are used to configure the device parameters. The corresponding events are the results after the configuration has taken place.

Write Cmd/Evt	Header	Opcode	Length /Result					Data			
	1 st	2 nd	3 rd	4 th 5 th 6 th 7 th 8 th 9 th						Nth	
BDNameWrite Cmd	0x25	0x31	Length (up to 16 bytes)	BD_Name (up to 16 bytes, MSB)							
BDNameWrite Evt	0x26	0x31	Result 0: ok others: fail								
Description: Setup tl	he device	friendly na	ame.								
BaudRateWrite Cmd	0x25	0x32	0x04	0: 2 2: 1 4: 3		LSB) : 9600 : 19200 : 57600					
BaudRateWrite Evt	0x26	0x32	Result 0: ok others: fail								
Description: Setup t reboot			,	able when u mand has b	0		erface. T	he baud	rate will I	be updated at the	next
BDAddrWrite Cmd	0x25	0x33	0x06		(6 k	BD_A oytes, pul	ddr blic, LSB)				
BDAddrWrite Evt	0x26	0x33	Result 0: ok others: fail								
Description: Setup tl	he Blueto	oth device	public addre	ess.							
AdvIntvWrite Cmd	0x25	0x35	0x04	(Unit: 1 ms	Adv Int , Valid R LSE	ange=20	~10000,				
AdvIntvWrite Evt	0x26	0x35	Result 0: ok others: fail								
Description: Setup t	he adverti	sing interv	al.								
AdvDataWrite Cmd	0x25	0x36	Length (up to 25 bytes)	((up to 25 I	oytes, Ma		lv Data er specif	ic data fi	eld value, MSB)	
AdvDataWrite Evt	0x26	0x36	Result 0: ok others: fail								
Ex: Advertising data 020106: 02: length= 01: type=F	d before til packet=0 2 lags LE Gener 60: 6 1anufactu	he Patch_I 20106 06f al Discove rer Specifi	3 execution. F04095E5f rable Mode/		ta=0409	5E5F60.	" field val	ue of the	advertis	sing packet and sl	hould
WhiteListWrite Cmd	0x25	0x37	0x06	Con		device a (6 bytes,	address – LSB)	white lis	st		
WhiteListWrite Evt	0x26	0x37	Result 0: ok others: fail								



Write Cmd/Evt	Header	Opcode	Length /Result					Data			
	1 st	2 nd	3 rd	4 th	5 th	6 th	7 th	8 th	9 th		Nth
TxPowerWrite Cmd	0x25	0x38	0x01	TxPwr (1 byte) 0: 3dBm 1: 0dBm Others: Reserved		1	1	1			
TxPowerWrite Evt	0x26	0x38	Result 0: ok others: fail								
Description: Configu	ire the dev	vice RF TX	power sett	ing value.							
BatteryLevelWrite Cmd	0x25	0x3B	0x01	Battery Level (1 byte)							
BatteryLevelWrite Evt	0x26	0x3B	Result 0: ok others: fail								
Description: The hos battery			device batte	ry level and ttery" service					nd. The o	cell phone can ob	otain the
BaudRateUpdate Cmd	0x25	0x3F	0x00	*Old baudr							
BaudRateUpdate Evt	0x26	0x3F	0x00	*New baud	rate						
should	use other	read com	mands to sy	nchronize t curs if this co MinInte (2 byt unit=1.2	he UAR ommand erval es, 5ms,	F interfac is not us MaxIr (2 b unit=1	e again. ed. nterval ytes, .25ms,			Timeout (2 bytes, unit=10ms,	
IntvLatencyWrite2 Evt	0x26	0x30	0x00	LSE	5)		SB)			LSB)	
	le after cc s has com this comm use the m al settings 1000_00_ 5000_00_ 7800_00_ C800_00_ F000_00_ B004_00_	nnection. pleted, the hand is exe aximum in are the cc 00_5802, 00_580	There will be correspond ceuted with a terval setting onfigurations //10~20 //80~10 //100~1 //100~2 //20~2 //20~2 //250~3 //1000-	e an error ev ding event p a total config g of 0x10 wh c for users to 0ms 50ms 50ms 00ms 250ms	vent if the acket wil guration on hile the a	e device i I be retur of "0x25_ ndroid sy	is discon ned. 40_08_0 rstem wil	nected w 1800_100 I prefer to	ith the co 0_00_00 0 use the	ell phone. After th	ne setup
AdvDataWrite2 Cmd	0x25	0x50	Length (up to 31 bytes)		(up to 3 ⁻	1 bytes, v		dv Data vertising	Data fiel	d value, MSB)	
AdvDataWrite2 Evt	0x26	0x50	Result 0: ok others: fail								
Description: This co	mmand is	upod to o	atun the who	le advertisi							
	on. Note t	hat the "A	dvDataWrite		is used	to modify	only the	"Manufa	cturer Sp	after a Patch_B pecific Data" field	value



Write Cmd/Evt	Header	Opcode	Length /Result	Data							
	1 st	2 nd	3 rd	4 th 5 th 6 th 7 th 8 th					9 th		N th
ScanResDataWrite Evt	0x26	0x51	Result 0: ok others: fail	k							
	Description: The ScanResDataWrite command is used to setup the whole scan response data field value and can only be used after a Patch B execution. The ScanResDataWrite event is used to response the Scan Request in the BLE protocol.										
DisconnectWrite Cmd	0x25	0x5F	0x00								
DisconnectWrite Evt 0x26 0x5F 0: ok others: fail											
Description: This con device										this command, the connection status.	

Event Packet

Packet Type	Opcode	Payload	Description
		0x00	Tx finish – Tx buffer empty
		0x01	Connection not established – ignore this Payload Packet
	0x22	0x02	Indication or Notification not enabled – ignore this Payload Packet
		0x03	Unknown error – ignore all Payload Packets
		0x04	Send data error – ignore this Payload Packet
		0x05	Tx buffer full – ignore this Payload Packet
		0x00	Changing the Connection Interval is successful
		0x01	Master rejected the Connection Interval setup
0x26		0x02	Command send fail
	0x30	0x12	
		0x13	Interval or length out of valid range
		0x14	
		0x15	No Connection
	0x40	0x12	Interval or length out of valid range
		0x10	Disconnected
	0xFF	0x11	Connected
	UXFF	0x19	Packet Type is not supported
		0x1C	Packet Type is not supported



Accessible Physical Address

Address	Description		Note		
0x0000_5FFC	ROM Version	0x99000000	A5		
0x0020_0134	Disable EEPROM Check	[0]	0: Reserved 1: Disable EEPROM check		
		0x0000~0x00B4	Buffer size		
0x0020_0480	Tx Buffer Valid Size	0xFFFF	Buffer error		
		0xFFB4 Not in connection mode			
0x0020_0484	Patch_B Version				
0x0020_0488	RF parameter Address				
0x0020_048C	RF parameter Size		Unit: byte		
0x0020_0490	Patch_A Version				
0x0020_0494	Function	[0]	0: Enable "262200" event 1: Disable "262200" event When the host MCU writes a payload into the BLE device to transmit air packets to a cell phone, the BLE device will send a "262200" event packet when the Tx operation has finished. If this bit is set high, the "262200" event packet will be disabled.		
		[1]	0: INT_EXT low active 1: INT_EXT high active		
0x0020_0500	Patch Start Address				
0x0020_1F80	Patch Execute Trigger		0 to execute Patch_A 0 to execute Patch_B		
		[6]	0: Device Patch_A successful 1: Device wait for Patch_A		
0x0060_2020	Patch State (map to CR5)	[10]	0: Device wait for Patch_B 1: Device Patch_B successful		
		[15]	0: Device ROM boot fail 1: Device ROM boot ok		

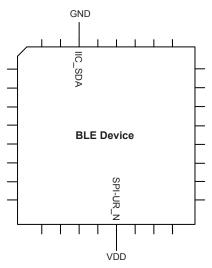


SPI Interface

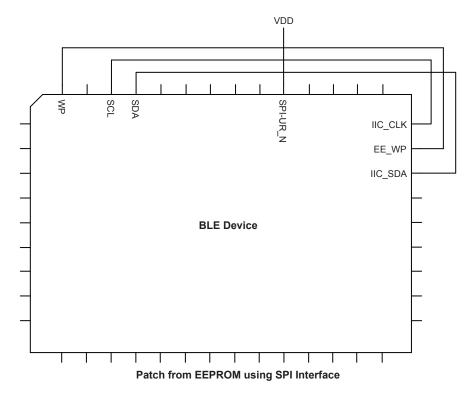
Hardware setup

The hardware environment should be established before using the SPI interface.

- Keep the SPI-UR_N pin=1 before the RST_N pin=1
- If patched from the MCU, keep the IIC_SDA pin=0
- If patched from an EEPROM, connect the IIC_CLK/IIC_SDA/EE_WP pins to the EEPROM corresponding pins.



Patch from MCU using SPI Interface



Rev. 0.00

July 19, 2017



SPI interface default setting

 5-Wire
 : SPI_MISO, SPI_MOSI, SPI_CS, SPI_CLK, SPI_INT/INT_EXT

 Data length
 : 8 bits (MSB first)

 Format
 : CPOL=0, CPHA=0

Operating mode : Duplex

Max. Frequency : 10MHz

SPI Command Format

Туре		Header			SPI Interface Action						
	Bit[7:5]	Bit[4:1]	Bit[0]	SPI MOSI	Read Registe	er					
Read Register	000b	0~8 (CR0~CR8)	1	SPI_MISO	8bit		Register 8bit		Reg	gister [7:0] 8bit	
	Bit[7:5]	Bit[4:1]	Bit[0]	SPI_MOSI	Read Registe	er	Register	[15:8]	Rec	gister [7:0]	1
Write		0~8		351_10031	8bit		8bit			8bit]
Register	001b	(CR0~CR8)	1	SPI_MISO							
	Bit[7:5]	Bit[4:0]	SPI MOSI	Read FIFO						
Read FIFO		Data Ler	igth		8bit						
Read FIFO	011b	0 means 32	2 byte	SPI_MISO			Data 0 8bit			Data (Leng 8bit	gth-1)
	Bit[7:5]	Bit[4:0]	SPI MOSI	Write FIFO		Data 0			Data (Leng	gth-1)
Write FIFO		Data Ler	Data Length		8bit		8bit			8bit	- ·
	101b	0 means 32	2 byte	SPI_MISO							
Example:		and Deviator	Desiste		04 Pagiatar V	- 1	-0.0200				

• "090300" means Read Register, Register Address=0x04, Register Value=0x0300

• "A3253400" means Write FIFO, Data Length=0x03, Data=0x253400

Control Register Table (CR0~CR8)

Name	Addr		Description
		SPI FIFO f If the data generated	length is greater than this value, the corresponding interrupt will be
CR0: Threshold	0x00	Bit[15:12]	Reserved
			Bit[11:6]
		Bit[5:0]	SPI Rx FIFO threshold (BLE \leftarrow MCU)
		0: Corre	ipt status dicate which interrupt is triggered. sponding interrupt condition did not occur sponding interrupt condition occurs
		Bit[15:5]	Reserved
CR1: Int_Status	0x01	Bit[4]	BLE Tx FIFO not empty
		Bit[3]	BLE Tx FIFO overflow
		Bit[2]	BLE Tx FIFO over threshold
		Bit[1]	BLE Rx FIFO empty
		Bit[0]	BLE Rx FIFO under threshold



Name	Addr		Description	
		Used to er 0: Corre	upt enable control nable the corresponding interrupt function. esponding interrupt not enabled esponding interrupt enabled	
	0x02	Bit[15:5]	Reserved	
CR2: Int_Set		Bit[4]	BLE Tx FIFO not empty	
		Bit[3]	BLE Tx FIFO overflow	
		Bit[2]	BLE Tx FIFO over threshold	
		Bit[1]	BLE Rx FIFO empty	
		Bit[0]	BLE Rx FIFO under threshold	
		Used to cl 0: No ad	upt status clear control – write only. ear the corresponding interrupt status. ction the corresponding interrupt status	
		Bit[15:5]	Reserved	
CR3: Int_Clr	0x03	Bit[4]	BLE Tx FIFO not empty	
		Bit[3]	BLE Tx FIFO overflow	
		Bit[2]	BLE Tx FIFO over threshold	
		Bit[1]	BLE Rx FIFO empty	
		Bit[0]	BLE Rx FIFO under threshold	
		SPI FIFO count Used to set the Tx/Rx FIFO depth.		
CR4: FIFO_Count	0x04	Bit[15:12]	Reserved	
		Bit[11:6]	SPI Tx FIFO count (BLE \rightarrow MCU)	
		Bit[5:0]	SPI Rx FIFO count (BLE \leftarrow MCU)	



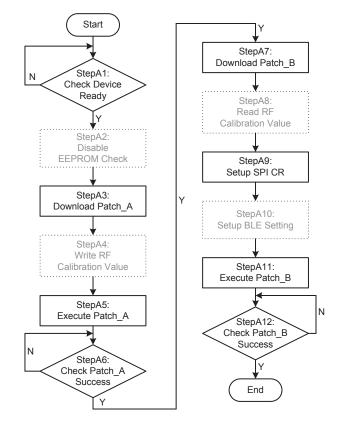
Name	Addr		Description
			e status, read only. /ICU can read this register to know the BLE device status.
		Bit[15]	Status_BLE_ROM_Init 0: Not ready 1: Ready
		Bit[14]	Status_BLE_Sleep 0: Active 1: Sleep
		Bit[13:12]	Reserved
		Bit[11]	Status INT_EXT_STATUS 0: No INT_EXT occurs 1: INT_EXT occurs
		Bit[10]	Status_BLE_Can_Sleep 0: BLE device is kept active 1: BLE device sleep/active switched automatically
		Bit[9]	Reserved
CR5: BLE_Status	0x05	Bit[8]	Status_Soft_Reset 0: Soft_Reset event does not occur or Soft_Reset event has finished 1: Soft_Reset event occurs This bit will be 1 when the Soft_Reset event occurs after setting the CR7 register bit[8] to 1. After this the bit value will be 0 and the register value will be 0x8040 after the Soft_Reset event has finished.
		Bit[7]	Status_Buffer_Reset 0: Buffer_Reset event does not occur or Buffer_Reset event has finished 1: Buffer_Reset occurs This bit will be 1 when the Buffer_Reset event occurs after setting the CR7 register bit[7] to 1. After this the bit value will be 0 after the Buffer_ Reset event has finished.
		Bit[6]	Status_Wait_For_Patch 0: Not necessary to download the patch 1: Wait for patch download
		Bit[5:3]	Reserved
		Bit[2]	Status_BLE_UUID_0xFFF1 0: Disable Notify 1: Enable Notify
		Bit[1]	Status_BLE_Connection 0: Not connected 1: Connected
		Bit[0]	Status_BLE_Cmd_Analysing 0: No analysis 1: Analysing If this bit is kept as "1" for a long period a Ctrl_Buffer_Reset execution is necessary.



Name	Addr		Description	
			e status set control, write only. can set the corresponding bit high to trigger various BLE device actions.	
		Bit[15:11]	Reserved	
	0x07	Bit[10]	Set_BLE_Can_Sleep Setting this bit high will enable the BLE device active/sleep auto-switch function.	
			Bit[9]	Reserved
CR7: BLE_Status_ Set		Bit[8]	Set_Soft_Reset Setting this bit high will trigger a BLE device Soft_Reset operation. The corresponding status bit, CR5[8], will be 1. After the Soft_Reset operation has completed, the CR5[8] value will be zero.	
			Bit[7]	Set_Buffer_Reset Setting this bit high will trigger a BLE device Buffer_Reset operation. The corresponding status bit, CR5[7], will be 1. After the Buffer_Reset operation has completed, the CR5[7] value will be zero.
		Bit[6:0]	Reserved	
			e status clear control, write only. can set the corresponding bit high to clear the BLE device action.	
		Bit[15:11]	Reserved	
		Bit[10]	Clr_BLE_Can_Sleep Setting this bit high will disable the BLE device active/sleep auto-switch function.	
CR8: BLE Status Clr	0x08	Bit[9]	Reserved	
	5,00	Bit[8]	Clr_Soft_Reset Setting this bit high will cancel a BLE device Soft_Reset action. After this the corresponding status bit, CR5[8], will be zero after a cancellation.	
		Bit[7]	Clr_Buffer_Reset Setting this bit high will cancel a BLE device Buffer_Reset action. After this the corresponding status bit, CR5[7] will be zero.	
		Bit[6:0]	Reserved	



Initialization Flow for the Mode_A – Patch from the MCU using the SPI Interface





Mode A – Patch from the MCU using the SPI Interface Flow

StepA1: Check Device Ready

- Read the Physical Address 0x0060_2020 to check whether the device Power-On is ready or not. If Bit[15]=1, it means that the device Power-On is ready and is waiting for the Patch.
- ◆ Reading the Physical Address 0x0060_2020 should be bit[15]=1, bit[10]=0, bit[6]=1.

• StepA2: Disable the EEPROM Check – optional

- If the IIC_SDA pin is kept high or floating, the EEPROM Check function must be disabled. Otherwise, the device will be in an endless check loop.
- Write the Physical Address 0x0020_0134 with a value of 0x0000_0001.

StepA3: Download Patch_A

 The MCU sends the Patch_A code to the device and writes the Patch_A code to the Physical Address 0x0020_0500.

StepA4: Write RF Calibration Value – optional

- This step should be ignored for the first boot. Otherwise, update the RF Calibration Value in this step if it has already been obtained from StepA8.
- Obtain the address where the RF Calibration Value is stored from the Physical Address 0x0020_0488.
- Write the RF Calibration Value to the address where the RF Calibration Value is stored.
- There should be at least 128 bytes of memory capacity to store the RF calibration value if this step is selected to be executed.

StepA5: Execute Patch_A

Write the Physical Address 0x0020_1F80 with a value of 0x0020_0500 after which the Patch_A code will start to boot for the variable setup, RF calibration, etc.

StepA6: Check Patch_A Success

- Read the Physical Address 0x0060_2020 to check whether the Patch_A execution is ready or not. If the Bit[6]=0, it means that the device Patch_A boot is successful.
- Reading the Physical Address 0x0060_2020 should be bit[15]=1,bit[10]=0,bit[6]=0.

StepA7: Download Patch_B

 The MCU sends the Patch_B code to the device and writes the Patch_B code to the Physical Address 0x0020_0500.

StepA8: Read RF Calibration Value – optional

- This operation should be executed for the first boot. Otherwise, this step can be ignored.
- Obtain the RF Calibration Value Address from the Physical Address 0x0020_0488.
- Obtain the RF Calibration Value Size from the Physical Address 0x0020_048C (unit: byte).
- Read the RF Calibration Value from the RF Calibration Value Address and save it for next initialization flow.
- There should be at least 128 bytes of memory capacity to store the RF calibration value if this step is selected to be executed.

StepA9: Setup SPI CR

- The MCU configures the SPI Control Register for the SPI_INT Interrupt that is used. If the EXT_ INT is only used this step can be ignored.
- The interrupt configurations will be available after StepA12.

StepA10: Setup BLE Setting – optional

 The MCU sends the Read/Write Command to setup the BLE device, such as BD_ADDR, BD_ Name, etc.

StepA11: Execute Patch_B

 The MCU writes the Physical Address 0x0020_1F80 with a value of 0x0000_0000 after which the Patch_B code will start to boot.

StepA12: Check Patch_B Success

- Read the Physical Address 0x0060_2020 to check whether the Patch_B boot is ready or not. If Bit[10]=1, than this means that the device Patch_B boot is successful.
- Reading the Physical Address 0x00602020 should be bit[15]=1, bit[10]=1, bit[6]=0.



Example for Mode_A – Patch from MCU using SPI Interface

Text Font	Normal	Bold	Italic
Subject	MCU_Rx	MCU_Tx	Patch
means that the device F	ess [°] 0x0060_2020 to check w Power-On is ready and is wai	/hether the device Power-On i ting for the Patch. be bit[15]=1, bit[10]=0, bit[6]=:	
A6560120206000 (Write FIF	-		
090000 (Read Register: SPI	,))	
		,	
090300 (Read Register: SPI	Tx FIFO count(CR4[11:6])=()x()C)	
6C570100002020600040800			
StepA2: Disable EEPRON	I Check – optional ot high or floating, the EEPR(ess check loop.	OM Check function must be di 0x0000_0001.	sabled. Otherwise the
AC55010000340120000100	0000 (Write FIFO)		
 StepA3: Download Patch The MCU sends the Pat 0x0020_0500. 	-	I write the Patch_A code to the	Physical Address
A8553800000052000 (Write	e FIFO)		
A0D01400E035029014D014	7A1060935093403A030C7	093CD7B9014D01475106093	(Write FIFO)
A05393403A030C7393CD7	B9014D014F0E313369014D	0014EFE37FFE9014D0146D1	0 (Write FIFO)
A060935393403A030C7303			
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	CD/B9014D014681060935	393403A030C7393CD7B9014	(Write FIFO)
		393403A030C7393CD7B9014 E1304B327B348B3023246B	,
A0D014F0E3BD079014D01	4F0E3B9079014780740006		3 (Write FIFO)
A0D014F0E3BD079014D01 A0013246B33C78D114C134	4F0E3B9079014780740006 48F44789463E4FF3063EC0	E1304B327B348B3023246B	3 (Write FIFO) C (Write FIFO)
A0D014F0E3BD079014D01 A0013246B33C78D114C134 A0A20067B46D94803B6DE	4F0E3B9079014780740006 48F44789463E4FF3063EC0 346894A13B68B46894803B	E1304B327B348B3023246B 90078B4661369B4679463EC	3 (Write FIFO) C (Write FIFO) 30 (Write FIFO)
A0D014F0E3BD079014D01 A0013246B33C78D114C134 A0A20067B46D94803B6DE A06DB4436C6432FFE3D7F	4F0E3B9079014780740006 48F44789463E4FF3063EC0 46894A13B68B46894803B 5F00C02050FA300540F0E3	E1304B327B348B3023246B 90078B4661369B4679463EC 68B4363361B46D94A53B01	3 (Write FIFO) C (Write FIFO) 30 (Write FIFO)
A0D014F0E3BD079014D01 A0013246B33C78D114C134 A0A20067B46D94803B6DE A06DB4436C6432FFE3D7F A855380000E0052000 (Writ	4F0E3B9079014780740006 48F44789463E4FF3063EC0 946894A13B68B46894803B F60C02050FA300540F0E3 e FIFO)	E1304B327B348B3023246B 90078B4661369B4679463EC 68B4363361B46D94A53B01	3 (Write FIFO) 2 (Write FIFO) 30 (Write FIFO) 4 (Write FIFO)
A0D014F0E3BD079014D01 A0013246B33C78D114C134 A0A20067B46D94803B6DE A06DB4436C6432FFE3D7F A855380000E0052000 (Writ A0853B61B49114C1144574	4F0E3B9079014780740006 48F44789463E4FF3063EC0 46894A13B68B46894803B F00C02050FA300540F0E3 e FIFO) 40032C36C03290B6C06048	E1304B327B348B3023246B 90078B4661369B4679463EC 68B4363361B46D94A53B01 C9277612003246B344B3619	3 (Write FIFO) 2 (Write FIFO) 30 (Write FIFO) 4 (Write FIFO) (Write FIFO)
A0D014F0E3BD079014D01 A0013246B33C78D114C134 A0A20067B46D94803B6DE A06DB4436C6432FFE3D7F A855380000E0052000 (Writ A0853B61B49114C1144574 A0FA0B81146C126093403E	4F0E3B9079014780740006 48F44789463E4FF3063EC0 46894A13B68B46894803B F00C02050FA300540F0E3 e FIFO) 40032C36C03290B6C06048 3040801326B124EA36A126	E1304B327B348B3023246B 90078B4661369B4679463EC 68B4363361B46D94A53B01 C9277612003246B344B3619 85B80840022105889744964	3 (Write FIFO) 2 (Write FIFO) 30 (Write FIFO) 4 (Write FIFO) (Write FIFO) B (Write FIFO)
A0D014F0E3BD079014D01 A0013246B33C78D114C134 A0A20067B46D94803B6DE A06DB4436C6432FFE3D7F A855380000E0052000 (Writ A0853B61B49114C1144574 A0FA0B81146C126093403E A0E0336F4343DC0822C13	4F0E3B9079014780740006 48F44789463E4FF3063EC0 46894A13B68B46894803B F00C02050FA300540F0E3 e FIFO) 40032C36C03290B6C06048 3040801326B124EA36A126 36F434493A83A44B320314	E1304B327B348B3023246B3 90078B4661369B4679463EC 68B4363361B46D94A53B013 C9277612003246B344B3619 85B80840022105889744964 E83312349126C5B6C5A418 01222B28031214123B25993	3 (Write FIFO) 2 (Write FIFO) 30 (Write FIFO) 4 (Write FIFO) (Write FIFO) B (Write FIFO) (Write FIFO)
A0D014F0E3BD079014D01 A0013246B33C78D114C134 A0A20067B46D94803B6DE A06DB4436C6432FFE3D7F A855380000E0052000 (Writ A0853B61B49114C1144574 A0FA0B81146C126093403E A0E0336F4343DC0822C133 A042EC1C0059B35993853	4F0E3B9079014780740006 48F44789463E4FF3063EC0 46894A13B68B46894803B F00C02050FA300540F0E3 e FIFO) 0032C36C03290B6C06048 3040801326B124EA36A126 36F434493A83A44B320314 A59B302EACBFF52B33C1	E1304B327B348B3023246B3 90078B4661369B4679463EC 68B4363361B46D94A53B013 C9277612003246B344B3619 85B80840022105889744964 E83312349126C5B6C5A418 01222B28031214123B25993 13CB35393843A53B35393A5	3 (Write FIFO) 3 (Write FIFO) 30 (Write FIFO) 4 (Write FIFO) (Write FIFO) B (Write FIFO) (Write FIFO) 3A (Write FIFO)
A0D014F0E3BD079014D01 A0013246B33C78D114C134 A0A20067B46D94803B6DE A06DB4436C6432FFE3D7F A855380000E0052000 (Writ A0853B61B49114C1144574 A0FA0B81146C126093403E A0E0336F4343DC0822C13 A042EC1C0059B35993853, A053B35393A23A53B3539	4F0E3B9079014780740006 48F44789463E4FF3063EC0 46894A13B68B46894803B F00C02050FA300540F0E3 e FIFO) 0032C36C03290B6C06048 8040801326B124EA36A126 36F434493A83A44B320314 A59B302EACBFF52B33C1 3A43A53B37611003240B33	E1304B327B348B3023246B3 90078B4661369B4679463EC 68B4363361B46D94A53B013 C9277612003246B344B3619 85B80840022105889744964 E83312349126C5B6C5A418 01222B28031214123B25993 13CB35393843A53B35393A5 251124B33C78C214C0323411	3 (Write FIFO) 2 (Write FIFO) 30 (Write FIFO) 4 (Write FIFO) (Write FIFO) B (Write FIFO) (Write FIFO) 3A (Write FIFO) 1 (Write FIFO)
A0D014F0E3BD079014D01 A0013246B33C78D114C134 A0A20067B46D94803B6DE A06DB4436C6432FFE3D7F A855380000E0052000 (Writ A0853B61B49114C1144574 A0FA0B81146C126093403E A0E0336F4343DC0822C133 A042EC1C0059B35993853 A053B35393A23A53B3539 A0434200EA3206E0358242	4F0E3B9079014780740006 48F44789463E4FF3063EC0 46894A13B68B46894803B F00C02050FA300540F0E3 e FIFO) 40032C36C03290B6C06048 3040801326B124EA36A126 36F434493A83A44B320314 A59B302EACBFF52B33C11 3A43A53B37611003240B33 AF45945C80940022E0338	E1304B327B348B3023246B3 90078B4661369B4679463EC 68B4363361B46D94A53B013 C9277612003246B344B36194 85B80840022105889744964 6E83312349126C5B6C5A4184 101222B28031214123B25993 13CB35393843A53B35393A5 151124B33C78C214C0323411 0A90A646F430121F50B3093	3 (Write FIFO) 2 (Write FIFO) 30 (Write FIFO) 4 (Write FIFO) (Write FIFO) B (Write FIFO) (Write FIFO) 3A (Write FIFO) (Write FIFO) (Write FIFO) (Write FIFO)
A0D014F0E3BD079014D01 A0013246B33C78D114C134 A0A20067B46D94803B6DE A06DB4436C6432FFE3D7F A855380000E0052000 (Writ A0853B61B49114C1144574 A0FA0B81146C126093403E A0E0336F4343DC0822C133 A042EC1C0059B359938533 A053B35393A23A53B35393 A0434200EA3206E0358242	4F0E3B9079014780740006 48F44789463E4FF3063EC0 46894A13B68B46894803B F00C02050FA300540F0E3 e FIFO) 40032C36C03290B6C06048 3040801326B124EA36A126 36F434493A83A44B320314 A59B302EACBFF52B33C11 3A43A53B37611003240B33 AF45945C80940022E0338	E1304B327B348B3023246B3 90078B4661369B4679463EC 68B4363361B46D94A53B013 C9277612003246B344B3619 85B80840022105889744964 E83312349126C5B6C5A418 01222B28031214123B25993 13CB35393843A53B35393A5 251124B33C78C214C0323411	3 (Write FIFO) 2 (Write FIFO) 30 (Write FIFO) 4 (Write FIFO) (Write FIFO) B (Write FIFO) (Write FIFO) 3A (Write FIFO) (Write FIFO) (Write FIFO) (Write FIFO)
A0D014F0E3BD079014D01 A0013246B33C78D114C134 A0A20067B46D94803B6DE A06DB4436C6432FFE3D7F A855380000E0052000 (Writ A0853B61B49114C1144574 A0FA0B81146C126093403E A0E0336F4343DC0822C133 A042EC1C0059B359938534 A0434200EA3206E0358242 A0471122DC3310319322D0  • StepA4: Write RF Calibrat • This step should be igno already been obtained f • Obtain the address whe • Write the RF Calibration	4F0E3B9079014780740006 48F44789463E4FF3063EC0 46894A13B68B46894803B F00C02050FA300540F0E3 e FIFO) 90032C36C03290B6C06048 3040801326B124EA36A126 36F434493A83A44B320314 A59B302EACBFF52B33C11 3A43A53B37611003240B33 AF45945C80940022E03386 C3410329322DC3510339322 tion Value – optional pred for the first boot. Otherw rom StepA8. re the RF Calibration Value i Value to the address where	E1304B327B348B3023246B3 90078B4661369B4679463EC 68B4363361B46D94A53B013 C9277612003246B344B36194 85B80840022105889744964 6E83312349126C5B6C5A4184 101222B28031214123B25993 13CB35393843A53B35393A5 151124B33C78C214C0323411 0A90A646F430121F50B3093	3 (Write FIFO) 2 (Write FIFO) 30 (Write FIFO) 4 (Write FIFO) 4 (Write FIFO) B (Write FIFO) (Write FIFO) 3A (Write FIFO) (Write FIFO) (Write FIFO) 4 (Write FIFO) 5 (Write FIFO) 6 (Write FIFO) 6 (Write FIFO) 7
A0D014F0E3BD079014D01 A0013246B33C78D114C134 A0A20067B46D94803B6DE A06DB4436C6432FFE3D7F A855380000E0052000 (Writ A0853B61B49114C1144574 A0FA0B81146C126093403E A0E0336F4343DC0822C133 A042EC1C0059B35993853 A0434200EA3206E0358242 A0434200EA3206E0358242 A0471122DC3310319322D0  • StepA4: Write RF Calibration * This step should be ignoralized be obtained f • Obtain the address whe • Write the RF Calibration • There should be at least to be executed.	4F0E3B9079014780740006 48F44789463E4FF3063EC0 46894A13B68B46894803B F00C02050FA300540F0E3 e FIFO) 90032C36C03290B6C06048 3040801326B124EA36A126 36F434493A83A44B320314 A59B302EACBFF52B33C1 3A43A53B37611003240B33 2AF45945C80940022E03380 C3410329322DC351033932 tion Value – optional ored for the first boot. Otherw rom StepA8. re the RF Calibration Value i Value to the address where t 128 bytes of memory capac	E1304B327B348B3023246B3 90078B4661369B4679463EC 68B4363361B46D94A53B013 C9277612003246B344B36194 85B80840022105889744964 6E83312349126C5B6C5A4184 901222B28031214123B25993 13CB35393843A53B35393A5 951124B33C78C214C0323411 0A90A646F430121F50B3093 2DC3610349322DC371023D8 vise update the RF Calibration s stored from the Physical Add the RF Calibration Value is stored	
A0D014F0E3BD079014D01 A0013246B33C78D114C134 A0A20067B46D94803B6DE A06DB4436C6432FFE3D7F A855380000E0052000 (Writ A0853B61B49114C1144574 A0FA0B81146C126093403E A0E0336F4343DC0822C13 A042EC1C0059B35993853 A0434200EA3206E0358242 A0471122DC3310319322D0 	4F0E3B9079014780740006 48F44789463E4FF3063EC0 46894A13B68B46894803B F00C02050FA300540F0E3 e FIFO) 0032C36C03290B6C06048 3040801326B124EA36A126 36F434493A83A44B320314 A59B302EACBFF52B33C17 3A43A53B37611003240B33 2AF45945C80940022E03386 C3410329322DC351033932 tion Value – optional ored for the first boot. Otherw rom StepA8. re the RF Calibration Value i Value to the address where t 128 bytes of memory capac	E1304B327B348B3023246B3 90078B4661369B4679463EC 68B4363361B46D94A53B013 C9277612003246B344B36194 85B80840022105889744964 6E83312349126C5B6C5A4184 01222B28031214123B25993 13CB35393843A53B35393A5 251124B33C78C214C0323411 0A90A646F430121F50B3093 2DC3610349322DC371023D8 vise update the RF Calibration s stored from the Physical Add the RF Calibration Value is stored the RF Calibration Value is stored the RF Calibration Value is stored the RF calibration	3 (Write FIFO) 2 (Write FIFO) 30 (Write FIFO) 4 (Write FIFO) 4 (Write FIFO) (Write FIFO) 3A (Write FIFO) 7 (Write FIFO) 7 (Write FIFO) 9 (Write FIFO) Value in this step if it has dress 0x0020_0488. ored. value if this step is selected (Write FIFO)
A0D014F0E3BD079014D01 A0013246B33C78D114C134 A0A20067B46D94803B6DE A06DB4436C6432FFE3D7F A855380000E0052000 (Writ A0853B61B49114C1144574 A0FA0B81146C126093403E A0E0336F4343DC0822C133 A042EC1C0059B359938533 A043220EA3206E0358242 A0471122DC3310319322D0  • StepA4: Write RF Calibrat • This step should be ignor already been obtained f • Obtain the address whe • Write the RF Calibration • There should be at lease to be executed. A055060000A01E2000AA55	4F0E3B9079014780740006 48F44789463E4FF3063EC0 46894A13B68B46894803B 5F00C02050FA300540F0E3 e FIFO) 40032C36C03290B6C06048 3040801326B124EA36A126 36F434493A83A44B320314 A59B302EACBFF52B33C11 3A43A53B37611003240B33 AF45945C80940022E0338 C3410329322DC351033932 tion Value – optional ored for the first boot. Otherw rom StepA8. re the RF Calibration Value i Value to the address where t 128 bytes of memory capac 575737575777577777797979 838385858585858787878787898	E1304B327B348B3023246B3 90078B4661369B4679463EC 68B4363361B46D94A53B013 C9277612003246B344B36194 85B80840022105889744964 85B80840022105889744964 82B3312349126C5B6C5A4184 801222B28031214123B25993 13CB35393843A53B35393A5 851124B33C78C214C0323411 0A90A646F430121F50B3093 2DC3610349322DC371023D8 vise update the RF Calibration s stored from the Physical Add the RF Calibration Value is stored the RF Calib	3 (Write FIFO) 2 (Write FIFO) 30 (Write FIFO) 4 (Write FIFO) 4 (Write FIFO) 5 (Write FIFO) 7 (Write FIFO) 7 (Write FIFO) 7 (Write FIFO) 8 (Write FIFO) 9 (Write FIFO) 7 (Write FIFO) 7 (Write FIFO) 8 (Write FIFO) 7 (Write FIFO) 7 (Write FIFO) 7 (Write FIFO) 7 (Write FIFO) 7 (Write FIFO) 7 (Write FIFO)
A0D014F0E3BD079014D01 A0013246B33C78D114C134 A0A20067B46D94803B6DE A06DB4436C6432FFE3D7F A855380000E0052000 (Writ A0853B61B49114C1144574 A0FA0B81146C126093403E A0E0336F4343DC0822C133 A042EC1C0059B35993853 A0434200EA3206E0358242 A0471122DC3310319322D0  • StepA4: Write RF Calibration already been obtained f • Obtain the address whe • Write the RF Calibration • There should be ignor already been obtained f • Obtain the address whe • Write the RF Calibration • There should be at least to be executed. A055060000A01E2000AA58 A055060000B81E20008383 A055060000D01E20009191	4F0E3B9079014780740006 48F44789463E4FF3063EC0 46894A13B68B46894803B F00C02050FA300540F0E3 e FIFO) 40032C36C03290B6C06048 3040801326B124EA36A126 36F434493A83A44B320314 A59B302EACBFF52B33C1 3A43A53B37611003240B33 A4F45945C80940022E03386 C3410329322DC3510339322 tion Value – optional ored for the first boot. Otherwork to StepA8. re the RF Calibration Value i Value to the address where t 128 bytes of memory capac 575737575777577777797979 8383858585858587878787898 93930D0B11111313151317	E1304B327B348B3023246B3 90078B4661369B4679463EC 68B4363361B46D94A53B013 C9277612003246B344B36194 85B80840022105889744964 E83312349126C5B6C5A4184 01222B28031214123B25993 I3CB35393843A53B35393A5 251124B33C78C214C0323411 DA90A646F430121F50B3093 2DC3610349322DC371023D8 vise update the RF Calibration s stored from the Physical Add the RF Calibration Value is stored the	



Text Font	Normal	Bold	Italic
Subject	MCU_Rx	MCU_Tx	Patch
<ul> <li>StepA5: Execute Patch_A</li> <li>Write the Physical Addre to boot for the variable set</li> </ul>	ss 0x0020_1F80 with a valu	e of 0x0020_0500 after which	the Patch_A code will start
AC55010000801F200000052	2000 (Write FIFO)		
StepA6: Check Patch_A S	uccess		
Bit[6]=0, it means that th	e device Patch_A boot is su	hether the Patch_A execution ccessful. be bit[15]=1,bit[10]=0,bit[6]=0.	
A6560120206000 (Write FIFC	—		
090000 (Read Register: SPI	,	)	
		,	
090300 (Read Register: SPI	Tx FIFO count(CR4[11:6])=0	x0C)	
6C570100002020600000800	· · · · · · · · · · · · · · · · · · ·	,	
StepA7: Download Patch	B		
· · -	-	writes the Patch_B code to the	ne Physical Address
A8553800000052000 (Write	e FIFO)		
A0D01400E039009014D014	7A1060935093403A030C70	93CD7B9014D01475106093	(Write FIFO)
A05393403A030C7393CD7E	39014D01400E0D7009014D	014EFE37FFE9014D0146D1	0 (Write FIFO)
A060935393403A030C7393	CD7B9014D0146810609353	393403A030C7393CD7B9014	(Write FIFO)
A0D014F0E3BD079014D014	4F0E3B9079014780740006	3106093431041B33C780000	(Write FIFO)
A0780740002C0520006B12	003121B3409302C4802803	0C013122B322C48028040C	(Write FIFO)
A06512023242B3641201312	21B33C78D014F0E3B42961	1124093933A40B3C1336F43	(Write FIFO)
A04493943A44B39014D414	9D116084403B0508FFE3E	EFF00A43E047A114083403A	(Write FIFO)
A855380000E0052000 (Write	e FIFO)		
A00308193240A3781180834	03C1608FFE3E0FF03EAFI	=01C2642E0C71116083015B	(Write FIFO)
A00074721100A30274E0C7	8028020C015C6C1160830D	0641F0CAD110036E5D86320	(Write FIFO)
A0C5DC632080C120708711	00842258F0E3A90880C12	074E5DC63206084153B0408	(Write FIFO)
A0002360A408047E1040112	208340824959C0A440A394	145810639203C48028030C (	Write FIFO)
A0013125B223C48028040C	7310023245B33C78C1336I	-43449342EC001844B34593	(Write FIFO)
		B30F3267104DB301EAFEFF	
A02EB300324CB3013241B3	302312BB34BB33C780000	007060000490600082002000	(Write FIFO)
StepA8: Read RF Calibrati	ion Value – ontional		
		Otherwise, this step can be igi	nored.
		ysical Address 0x0020_0488.	
		al Address 0x0020_048C (un	5 ,
		on Value Address and save it f ity to store the RF calibration	
to be executed.	120 bytes of memory capac		value II this step is selected
A656018C042000 (Write FIF	0)		
090000 (Read Register: SPI	,	)	
		/	
090300 (Read Register: SPI	Tx FIFO count(CR4[11:6])=0	x0C)	
6C570100008C04200078000		,	
A6560188042000 (Write FIFC	`		
<b>09</b> 0000 (Read Register: SPI	,	)	
		1	
090300 (Read Register: SPI		xuu)	

## BC7601/BC7602/BC32F7611 Preliminary BLE Transparent Transmission Controller Programming User Guide



Text Font	Normal	Bold	Italic
Subject	MCU_Rx	MCU_Tx	Patch
6C5701000088042000A0E12		_	201E0A)
A65606A01E2000 (Write FIF	0)		,
090000 (Read Register: SPI	Tx FIFO count(CR4[11:6])=(	0)	
090800 (Read Register: SPI	Tx FIFO count(CR4[11:6])=0	0x20)	
6056060000A01E2000AA55	7573757577757777797979	797B7B7B7B7B7D7D8181818	1 (Read FIFO: RF Calibration
Value)			
A65606B81E2000 (Write FIF	1		
090000 (Read Register: SPI	Tx FIFO count(CR4[11:6])=(	0)	
090800 (Read Register: SPI	( 6 2/	,	
6056060000B81E200083838 Value)	3838383838383838787878787898	399999999999999999999999999999999999999	(Read FIFU: RF Calibration
A65606D01E2000 (Write FIF	0)		
090000 (Read Register: SPI	,	0)	
	-(- L -1) -	,	
090800 (Read Register: SPI	Tx FIFO count(CR4[11:6])=(	0x20)	
6056060000D01E200091919 Value)	93930D0B111113131513171	15191719191B1B21212321	(Read FIFO: RF Calibration
A65606E81E2000 (Write FIF	O)		
090000 (Read Register: SPI	Tx FIFO count(CR4[11:6])=(	0)	
090800 (Read Register: SPI	Tx FIFO count(CR4[11:6])=(	0x20)	
6056060000E81E200023232	( L 2/	,	(Read FIFO: RF Calibration
6056060000E81E200023232 Value)	525272729272B292B2B31	,	(Read FIFO: RF Calibration
6056060000E81E200023232 Value) A65606001F2000 (Write FIF	525272729272B292B2B31	313331333353537373937	(Read FIFO: RF Calibration
6056060000E81E200023232 Value) A65606001F2000 (Write FIF	525272729272B292B2B31	313331333353537373937	(Read FIFO: RF Calibration
6056060000E81E200023232 Value) A65606001F2000 (Write FIF 090000 (Read Register: SPI 	2525272729272B292B2B31 O) Tx FIFO count(CR4[11:6])=(	313331333353537373937 )	(Read FIFO: RF Calibration
6056060000E81E200023232 Value) A65606001F2000 (Write FIF 090000 (Read Register: SPI  090800 (Read Register: SPI	2525272729272B292B2B31 O) Tx FIFO count(CR4[11:6])=( Tx FIFO count(CR4[11:6])=(	313331333353537373937 0) 0x20)	· · · · · · · · · · · · · · · · · · ·
6056060000E81E200023232 Value) A65606001F2000 (Write FIF 090000 (Read Register: SPI  090800 (Read Register: SPI 6056060000001F200039393	2525272729272B292B2B31 O) Tx FIFO count(CR4[11:6])=( Tx FIFO count(CR4[11:6])=(	313331333353537373937 0) 0x20)	· · · · · · · · · · · · · · · · · · ·
6056060000E81E200023232 Value) A65606001F2000 (Write FIF 090000 (Read Register: SPI  090800 (Read Register: SPI 605606000001F200039393 Value)	2525272729272B292B2B31 O) Tx FIFO count(CR4[11:6])=( Tx FIFO count(CR4[11:6])=(	313331333353537373937 0) 0x20)	· · · · · · · · · · · · · · · · · · ·
6056060000E81E200023232 Value) A65606001F2000 (Write FIF 090000 (Read Register: SPI  090800 (Read Register: SPI 605606000001F200039393 Value) • StepA9: Setup SPI CR • The MCU configures the	2525272729272B292B2B31 O) Tx FIFO count(CR4[11:6])=( Tx FIFO count(CR4[11:6])=( B3B3D3D44164316421842 SPI Control Register for the	313331333353537373937 0) 0x20)	) (Read FIFO: RF Calibration
6056060000E81E200023232 Value) A65606001F2000 (Write FIF 090000 (Read Register: SPI  090800 (Read Register: SPI 605606000001F200039393 Value) • StepA9: Setup SPI CR • The MCU configures the used this step can be ign	2:525272729272B292B2B31 O) Tx FIFO count(CR4[11:6])=( Tx FIFO count(CR4[11:6])=( B3B3D3D44164316421842 SPI Control Register for the nored.	313331333353537373937 D) Dx20) 0C410C2401003812240000 e SPI_INT Interrupt that is us	) (Read FIFO: RF Calibration
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605606000E81E200023232 Value) A65606001F2000 (Write FIF 090000 (Read Register: SPI  090800 (Read Register: SPI 605606000001F200039393 Value) • StepA9: Setup SPI CR • The MCU configures the used this step can be igu • The interrupt configuratio 010000 (Read Register: CR0 030017 (Read Register: CR1	2525272729272B292B2B31 O) Tx FIFO count(CR4[11:6])=( B3B3D3D44164316421842 SPI Control Register for the hored. ons will be available after St _Threshold=0x0000) _Int_Status=0x0017)	313331333353537373937 D) Dx20) 0C410C2401003812240000 e SPI_INT Interrupt that is us	) (Read FIFO: RF Calibration
6056060000E81E200023232 Value) A65606001F2000 (Write FIF 090000 (Read Register: SPI  090800 (Read Register: SPI 605606000001F200039393 Value) • StepA9: Setup SPI CR • The MCU configures the used this step can be igu • The interrupt configuratio 010000 (Read Register: CR1 070000 (Read Register: CR3	2525272729272B292B2B31 O) Tx FIFO count(CR4[11:6])=( Tx FIFO count(CR4[11:6])=( B3B3D3D44164316421842 SPI Control Register for the hored. ons will be available after St _Threshold=0x0000) _Int_Status=0x0017) _Int_Clr=0x0000)	313331333353537373937 D) Dx20) 0C410C2401003812240000 e SPI_INT Interrupt that is us	) (Read FIFO: RF Calibration
6056060000E81E200023232 Value) A65606001F2000 (Write FIF- 090000 (Read Register: SPI  090800 (Read Register: SPI 605606000001F200039393 Value) • StepA9: Setup SPI CR • The MCU configures the used this step can be igi • The interrupt configuratii 010000 (Read Register: CR3 050000 (Read Register: CR3	2525272729272B292B2B31 O) Tx FIFO count(CR4[11:6])=( Tx FIFO count(CR4[11:6])=( B3B3D3D44164316421842 SPI Control Register for the nored. ons will be available after St _Threshold=0x0000) _Int_Status=0x0017) _Int_CIr=0x0000) _Int_Set=0x0000)	313331333353537373937 D) Dx20) 0C410C2401003812240000 e SPI_INT Interrupt that is us	) (Read FIFO: RF Calibration
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6056060000E81E200023232 Value) A65606001F2000 (Write FIF 090000 (Read Register: SPI  090800 (Read Register: SPI 605606000001F200039393 Value) • StepA9: Setup SPI CR • The MCU configures the used this step can be ign • The interrupt configuration 010000 (Read Register: CR0 030017 (Read Register: CR3 050000 (Read Register: CR4 090000 (Read Register: CR4 090000 (Read Register: CR4	2525272729272B292B2B31 O) Tx FIFO count(CR4[11:6])=( B3B3D3D44164316421842 SPI Control Register for the hored. Dns will be available after St _Threshold=0x0000) _Int_Status=0x0017) _Int_CIr=0x0000) _FIFO_Count=0x0000) SBLE_Status=8400) _BLE_Status_Set=0000)	313331333353537373937 D) Dx20) 0C410C2401003812240000 e SPI_INT Interrupt that is us	) (Read FIFO: RF Calibration
6056060000E81E200023232 Value) A65606001F2000 (Write FIF- 090000 (Read Register: SPI  090800 (Read Register: SPI 605606000001F200039393 Value) • StepA9: Setup SPI CR • The MCU configures the used this step can be igi • The interrupt configuration 010000 (Read Register: CR3 050000 (Read Register: CR4 0B8400 (Read Register: CR5 0F0000 (Read Register: CR5	2:525272729272B292B2B31 O) Tx FIFO count(CR4[11:6])=( Tx FIFO count(CR4[11:6])=( B3B3D3D44164316421842 SPI Control Register for the nored. Dns will be available after St _Threshold=0x0000) _Int_Status=0x0017) _Int_CIr=0x0000) _Int_Set=0x0000) _FIFO_Count=0x0000) SBLE_Status=8400) _BLE_Status_CIr=0000) _BLE_Status_CIr=0000)	313331333353537373937 D) Dx20) 0C410C2401003812240000 e SPI_INT Interrupt that is us	) (Read FIFO: RF Calibration
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6056060000E81E200023232 Value) A65606001F2000 (Write FIF 090000 (Read Register: SPI  090800 (Read Register: SPI 605606000001F200039393 Value) • StepA9: Setup SPI CR • The MCU configures the used this step can be igi • The interrupt configuratio 010000 (Read Register: CR3 050000 (Read Register: CR3 050000 (Read Register: CR4 0B8400 (Read Register: CR5 0F0000 (Read Register: CR5	2525272729272B292B2B31 O) Tx FIFO count(CR4[11:6])=( Tx FIFO count(CR4[11:6])=( B3B3D3D44164316421842 SPI Control Register for the bored. SPI Control Register for the spin control Register for	313331333353537373937 D) Dx20) 0C410C2401003812240000 e SPI_INT Interrupt that is us repA12.	) (Read FIFO: RF Calibration
6056060000E81E200023232 Value) A65606001F2000 (Write FIF 090000 (Read Register: SPI  090800 (Read Register: SPI 605606000001F200039393 Value) • StepA9: Setup SPI CR • The MCU configures the used this step can be igi • The interrupt configuratio 010000 (Read Register: CR0 030017 (Read Register: CR2 090000 (Read Register: CR3 050000 (Read Register: CR4 0B8400 (Read Register: CR5 0F0000 (Read Register: CR5 0F0000 (Read Register: CR5 0F0000 (Read Register: CR3 27000F (Write Register: CR3 250010 (Write Register: CR5	2525272729272B292B2B31 O) Tx FIFO count(CR4[11:6])=( B3B3D3D44164316421842 SPI Control Register for the hored. Drs will be available after St _Threshold=0x0000) _Int_Status=0x0017) _Int_Clr=0x0000) _FIFO_Count=0x0000) _FIFO_Count=0x0000) _BLE_Status=8400) _BLE_Status_Set=0000) _BLE_Status_Clr=0000) _Int_Set=0010) _Threshold=0000, read bac	313331333353537373937 D) Dx20) 0C410C2401003812240000 e SPI_INT Interrupt that is us repA12. k for check)	) (Read FIFO: RF Calibration
6056060000E81E200023232 Value) A65606001F2000 (Write FIF 090000 (Read Register: SPI  090800 (Read Register: SPI 605606000001F200039393 Value) • StepA9: Setup SPI CR • The MCU configures the used this step can be ign • The interrupt configuration 010000 (Read Register: CR0 030017 (Read Register: CR3 050000 (Read Register: CR4 090000 (Read Register: CR5 0F0000 (Read Register: CR5 0F0000 (Read Register: CR8 27000F (Write Register: CR3 250010 (Write Register: CR2 010000 (Read Register: CR2	2525272729272B292B2B31 	31333133335353537373937 D) Dx20) 0C410C2401003812240000 e SPI_INT Interrupt that is us iepA12. k for check) k for check) k for check)	) (Read FIFO: RF Calibration



Text Font	Normal	Bold	Italic		
Subject	MCU Rx	MCU Tx	Patch		
90000 (Read Register: CR4_FIFO_Count=0000, read back for check)					
0B8400 (Read Register: CR					
0F0000 (Read Register: CR7	 '_BLE_Status_Set=0000, rea	ad back for check)			
StepA10: Setup BLE Setti	ing – optional	the BLE device, such as BD_/	ADDR. BD Name, etc.		
A6253103313131 (Write FIF		_	, <u> </u>		
090000 (Read Register: SPI	Tx FIFO count(CR4[11:6])=0	)			
		,			
0900C0 (Read Register: SPI	Tx FIFO count(CR4[11:6])=0	0x03)			
63263100 (Read FIFO: BDN	ameWrite Evt )				
A9253306112233445566 (W	rite FIFO: BDAddrWrite Com	imand)			
090000 (Read Register: SPI	Tx FIFO count(CR4[11:6])=0	)			
0900C0 (Read Register: SPI		0x03)			
63263300 (Read FIFO: BDA	,				
A725350464000000 (Write F		,			
090000 (Read Register: SPI	Tx FIFO count(CR4[11:6])=0	)			
0900C0 (Read Register: SPI		JXU3)			
63263500 (Read FIFO: Advir	,				
A425380100 (Write FIFO: Tx 090000 (Read Register: SPI	,	)			
00000 (Read Register. SFT		)			
0900C0 (Read Register: SPI	Tx FIFO count(CR4[11:6])=0	)x(),3)			
63263800 (Read FIFO: TxPo	· · · · · · · · · · · · · · · · · · ·				
StepA11: Execute Patch_	B	with a value of 0x0000_0000	after which the Patch_B		
AC55010000801F20000000000 (Write FIFO)					
<ul> <li>StepA12: Check Patch_B Success</li> <li>Read the Physical Address 0x0060_2020 to check whether the Patch_B boot is ready or not. If Bit[10]=1, then this means that the device Patch_B boot is successful.</li> <li>Reading the Physical Address 0x00602020 should be bit[15]=1, bit[10]=1, bit[6]=0.</li> <li>A6560120206000 (Write FIFO)</li> </ul>					
090000 (Read Register: SPI	1	)			
		,			
090300 (Read Register: SPI	090300 (Read Register: SPI Tx FIFO count(CR4[11:6])=0x0C)				
	6C570100002020600040800000 (Read FIFO)				
StepN: Connection Established					
090000 (Read Register: SPI Tx FIFO count(CR4[11:6])=0)					
0900C0 (Read Register: SPI Tx FIFO count(CR4[11:6])=0x03)					
6322FF11 (Read FIFO)					
StepN+1: Receive Payload Packet from cell phone					
090000 (Read Register: SPI	090000 (Read Register: SPI Tx FIFO count(CR4[11:6])=0)				
· · · · · ·	090140 (Read Register: SPI Tx FIFO count(CR4[11:6])=0x05) 652203123456 (Read FIFO: payload=123456)				
002203123456 (Read FIFO:	payload=123456)				



Text Font	Normal	Bold	Italic
Subject	MCU_Rx	MCU_Tx	Patch

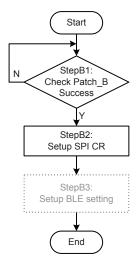
### Patch Time for the Mode_A – Patch from the MCU using the SPI Interface

The patch time may be different due to various versions. The following patch time is measured for the patch version 161025A5, in which the Patch_A size=0x02C0 bytes and the Patch_B size=0x1480 bytes.

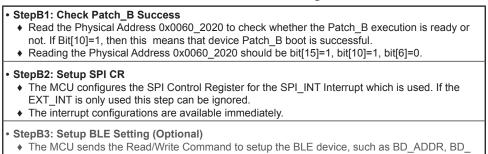
SPI=1Mhz, total time=500ms (typical), A1+A2+A3+A5+A6+A7+A9+A11+A12

SPI=1Mhz, total time=140ms (typical), A1+A2+A3+A4+A5+A6+A7+A9+A11+A12

## Initialization Flow for the Mode_B – Patch from the EEPROM using the SPI Interface



### Procedures for the Mode B – Patch from the EEPROM using the SPI Interface



Name, etc.



-	Mode_B – Patch from th	e EEPROM using the SP		
Text Font	Normal	Bold	Italic	
Subject	MCU_Rx	MCU_Tx	Patch	
<ul> <li>StepB1: Check Patch_B Success</li> <li>Read the Physical Address 0x0060_2020 to check whether the Patch_B execution is ready or not. If Bit[10]=1 then this means that device Patch_B boot is successful.</li> <li>Reading the Physical Address 0x0060_2020 should be bit[15]=1, bit[10]=1, bit[6]=0.</li> </ul>				
A6560120206000 (Write FIF	0)			
090000 (Read Register: SPI	Tx FIFO count(CR4[11:6])=0)	)		
090300 (Read Register: SPI	Tx FIFO count(CR4[11:6])=0;	x0C)		
6C570100002020600040800	0000 (Read FIFO)			
used, this step can be ig		SPI_INT Interrupt which is us	ed. If the EXT_INT is only	
010000 (Read Register: CR0	)_Threshold=0x0000)			
030017 (Read Register: CR1	I_Int_Status=0x0017)			
070000 (Read Register: CR3	3_Int_Clr=0x0000)			
050000 (Read Register: CR2	/			
090000 (Read Register: CR4	LFIFO_Count=0x0000)			
0B8400 (Read Register: CR	5_BLE_Status=8400)			
0F0000 (Read Register: CR7				
110000 (Read Register: CR8	BLE_Status_Clr=0000)			
27000F (Write Register: CR3	/			
250010 (Write Register: CR2				
010000 (Read Register: CR0_Threshold=0000, read back for check)				
030017 (Read Register: CR1_Int_Status=0017, read back for check)				
070000 (Read Register: CR3_Int_Clr=0000, read back for check)				
050010 (Read Register: CR2_Int_Set=0010, read back for check)				
090000 (Read Register: CR4_FIFO_Count=0000, read back for check) 0B8400 (Read Register: CR5_BLE_Status=8400, read back for check)				
	7_BLE_Status_Set=0000, rea	id back for check)		
<ul> <li>StepB3: Setup BLE Setting (Optional)</li> <li>The MCU sends the Read/Write Command to setup the BLE device, such as BD_ADDR, BD_Name, etc.</li> </ul>				
46253103313131 (Write FIFO: BDNameWrite Cmd)				
090000 (Read Register: SPI Tx FIFO count(CR4[11:6])=0)				
 0900C0 (Read Register: SPI Tx FIFO count(CR4[11:6])=0x03)				
63263100 (Read Register of Fixer in Countries Even )				
A9253306112233445566 (Write FIFO: BDAddrWrite Command)				
090000 (Read Register: SPI Tx FIFO count(CR4[11:6])=0)				
		,		
0900C0 (Read Register: SPI	Tx FIFO count(CR4[11:6])=0	x03)		
63263300 (Read FIFO: BDAddrWrite Evt )				
A725350464000000 (Write FIFO: AdvIntvWrite Command)				
090000 (Read Register: SPI Tx FIFO count(CR4[11:6])=0)				
	· · · · · · · · · · · · · · · · · · ·			
0900C0 (Read Register: SPI Tx FIFO count(CR4[11:6])=0x03)				
63263500 (Read FIFO: Advi	ntvWrite Evt)			

## Example for the Mode_B – Patch from the EEPROM using the SPI Interface

## BC7601/BC7602/BC32F7611 Preliminary BLE Transparent Transmission Controller Programming User Guide



Text Font	Normal	Bold	Italic		
Subject	MCU_Rx	MCU_Tx	Patch		
A425380100 (Write FIFO: T>	PowerWrite Command)				
090000 (Read Register: SPI	Tx FIFO count(CR4[11:6])=0	)			
0900C0 (Read Register: SPI	Tx FIFO count(CR4[11:6])=0	x03)			
63263800 (Read FIFO: TxPo	owerWrite Evt )				
StepN: Connection Estab	lished				
090000 (Read Register: SPI	Tx FIFO count(CR4[11:6])=0	)			
0900C0 (Read Register: SPI	Tx FIFO count(CR4[11:6])=0	x03)			
6322FF11 (Read FIFO)					
<ul> <li>StepN+1: Receive Payloa</li> </ul>	StepN+1: Receive Payload Packet from cell phone				
090000 (Read Register SPI Tx FIFO count(CR4[11:6])=0)					
090140 (Read Register SPI Tx FIFO count(CR4[11:6])=0x05)					
652203123456 (Read FIFO: payload=123456)					

### Patch Time for the Mode_B – Patch from the EEPROM using the SPI Interface

The patch time may be different due to various versions. The following patch time is measured for the patch version 161025A5, in which the Patch_A size=0x02C0 bytes and the Patch_B size=0x1480 bytes.

First boot with the RF calibration: SPI=1MHz, total time=850ms (typical), B1+B2

After boot the device will write the RF calibration value into the EEPROM.

Second boot without RF calibration: SPI=1MHz, total time=350ms (typical), B1+B2

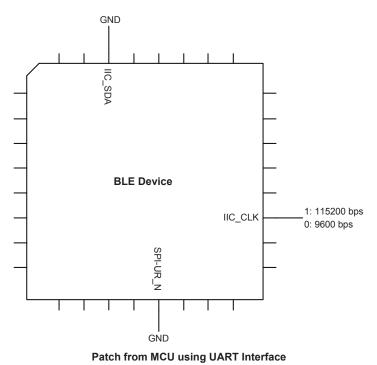


## **UART Interface**

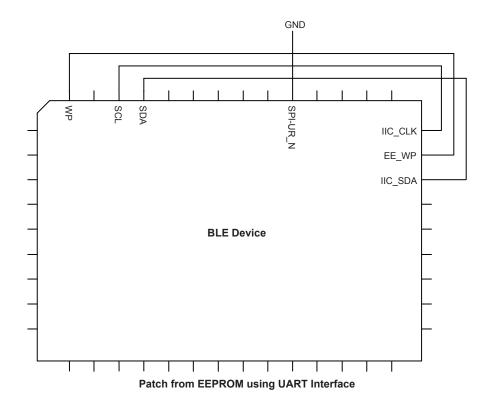
## **Hardware Setup**

The hardware environment should be established before using the UART interface.

- Keep the SPI-UR_N pin=0 before the RST_N pin=1
- If patched from the MCU, keep the IIC_SDA pin=0. The IIC_CLK pin can then be used to select the default baudrate.
- If patched from the EEPROM, connect the IIC_CLK/IIC_SDA/EE_WP pins to the EEPROM corresponding pins.
- The recommended retry period is 100ms to avoid the BLE buffer overflowing when using the UART interface.





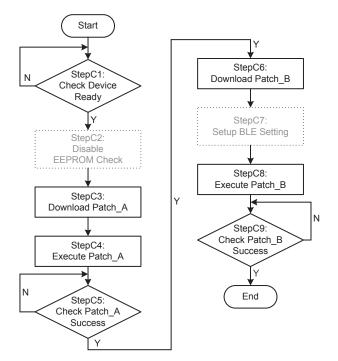


## **UART Interface Default Setup**

Flow control	: Enable
Data length	: 8 bits
Stop bit	: 1 bit
Parity	: None
Baudrate	: 115200 bps



## Initialization Flow for the Mode C – Patch from the MCU using the UART Interface



#### Procedures for the Mode C - Patch from the MCU using the UART Interface

#### • StepC1: Check Device Ready

Read the Physical Address 0x0060_2020 to check whether the device is powered on and is ready or not. If Bit[15]=1, this means that the device is powered on and waiting for the Patch.
 Reading the Physical Address 0x0060_2020 should be bit[15]=1,bit[10]=0,bit[6]=1.

StepC2: Disable EEPROM Check – optional

- If the IIC_SDA pin is kept high or floating, the EEPROM Check function must be disabled. Otherwise the device will remain in an endless check loop.
- Write the Physical Address 0x0020_0134 with a value of 0x0000_0001.

#### StepC3: Download Patch_A

 The MCU sends the Patch_A code to the device and writes the Patch_A code to the Physical Address 0x0020_0500.

#### StepC4: Execute Patch_A

Write the Physical Address 0x0020_1F80 with a value of 0x0020_0500 after which the Patch_A code will start to boot for the variable setup, RF calibration etc.

#### StepC5: Check Patch_A Success

- Read the Physical Address 0x0060_2020 to check whether the Patch_A execution is ready or not. If Bit[6]=0, then this means that the device Patch_A boot has been successful.
- Reading the Physical Address 0x0060_2020 should be bit[15]=1, bit[10]=0, bit[6]=0.
- The recommended retry period is 100ms to avoid the BLE buffer overflowing when using the UART interface.

#### • StepC6: Download Patch_B

 The MCU sends the Patch_B code to the device and writes the Patch_B code to the Physical Address 0x0020_0500.

• StepC7: Setup BLE Setting – optional

 The MCU sends the Read/Write Command to setup the BLE device, such as BD_ADDR, BD_ Name, etc.



### StepC8: Execute Patch_B

 The MCU writes the Physical Address 0x0020_1F80 with a value of 0x0000_0000 after which the Patch_B code will start to boot.

#### StepC9: Check Patch_B Success

- Read the Physical Address 0x0060_2020 to check whether the Patch_B boot is ready or not. If
- Bit[10]=1, than this means that the device Patch_B boot has been successful.
- Reading the Physical Address 0x0060_2020 should be bit[15]=1, bit[10]=1, bit[6]=0.

### Example for the Mode_C – Patch from the MCU using the UART Interface

		-			
Text Font	Text Font Normal Bold Italic				
Subject	MCU_Rx	MCU_Tx	Patch		
<ul> <li>StepC1: Check Device Ready</li> <li>Read the Physical Address 0x0060_2020 to check whether the device is powered on and is ready or not. If Bit[15]=1, this means that the device is powered on and waiting for the Patch.</li> <li>Reading the Physical Address 0x0060_2020 should be bit[15]=1, bit[10]=0, bit[6]=1.</li> </ul>					
UART_Tx=560120206000 UART_Rx=57010000202060	0040800000				
StepC2: Disable EEPRON     If the IIC_SDA pin is kep     device will remain in an	I Check – optional ot high or floating, the EEPRO	DM Check function must be di e of 0x0000_0001.	sabled. Otherwise the		
UART_Tx=55010000340120	0001000000				
<ul> <li>StepC3: Download Patch</li> <li>The MCU sends the Pat 0x0020_0500.</li> </ul>		writes the Patch_A code to th	e Physical Address		
UART_Tx=D01400E035029014D0147A1060935093403A030C7093CD7B9014D01475106093 UART_Tx=5393403A030C7393CD7B9014D014F0E313369014D014EFE37FFE9014D0146D10 UART_Tx=60935393403A030C7393CD7B9014D014681060935393403A030C7393CD7B9014 UART_Tx=D014F0E3BD079014D014F0E3B9079014780740006E1304B327B348B3023246B3 UART_Tx=013246B33C78D114C1348F44789463E4FF3063EC090078B4661369B4679463EC UART_Tx=420067B46D94803B6DB46894A13B68B46894803B68B4363361B46D94A53B0130 UART_Tx=6DB4436C6432FFE3D7FF00C02050FA300540F0E3C9277612003246B344B36194 UART_Tx=5380000E0052000 UART_Tx=55380000E0052000 UART_Tx=853B61B49114C11445740032C36C03290B6C0604885B80840022105889744964 UART_Tx=60B81146C126093403B040801326B124EA36A126E83312349126C5B6C5A418B UART_Tx=6036F4343DC0822C1336F434493A83A44B32031401222B28031214123B25993 UART_Tx=42EC1C0059B35993853A59B302EACBFF52B33C113CB35393843A53B35393A53A UART_Tx=53B35393A23A53B35393A43A53B37611003240B3351124B33C78C214C0323411 UART_Tx=434200EA3206E0358242AF45945C80940022E03380A90A646F430121F50B3093 UART_Tx=471122DC3310319322DC3410329322DC3510339322DC3610349322DC371023D8 					
<ul> <li>StepC4: Execute Patch_A</li> <li>Write the Physical Address 0x0020_1F80 with a value of 0x0020_0500 after which the Patch_A code will start to boot for the variable setup, RF calibration etc.</li> </ul>					
UART_Tx=55010000801F200000052000					
<ul> <li>StepC5: Check Patch_A Success</li> <li>Read the Physical Address 0x0060_2020 to check whether the Patch_A execution is ready or not. If Bit[6]=0, then this means that the device Patch_A boot has been successful.</li> <li>Reading the Physical Address 0x0060_2020 should be bit[15]=1, bit[10]=0, bit[6]=0.</li> <li>The recommended retry period is 100ms to avoid the BLE buffer overflowing when using the UART interface.</li> </ul>					
UART_Tx=560120206000	JART_Tx=560120206000				

UART_Rx=570100002020600000800000



Text Font	Normal	Bold	Italic			
Subject	MCU_Rx	MCU_Tx	Patch			
	StepC6: Download Patch_B ◆ The MCU sends the Patch_B code to the device and writes the Patch_B code to the Physical Address					
UART_Tx=5393403A030C7 UART_Tx=60935393403A03 UART_Tx=D014F0E3BD079 UART_Tx=780740002C0520 UART_Tx=6512023242B364 UART_Tx=6512023242B364 UART_Tx=55380000E00520 UART_Tx=0308193240A373 UART_Tx=0074721100A302 UART_Tx=0074721100A302 UART_Tx=002360A4080471 UART_Tx=013125B223C480	014D0147A1060935093403, 393CD7B9014D01400E0D7 30C7393CD7B9014D014681 0014D014F0E3B907901478 0006B12003121B3409302C 12013121B33C78D014F0E 014D4149D116084403B050 000 3118083403C1608FFE3E0F1 274E0C78028020C015C6C1 2070871100842258F0E3A90 E104011208340824959C0A4 028040C7310023245B33C7	A030C7093CD7B9014D0147 009014D014EFE37FFE9014 1060935393403A030C7393C 07400063106093431041B33 48028030C013122B322C480 3B42961124093933A40B3C 8FFE3EEFF00A43E047A114 F03EAFF01C2642E0C711160 160830D641F0CAD110036E 8880C12074E5DC632060841 440A394145810639203C480 8C1336F43449342EC001844 3321033B30F3267104DB301	D0146D10 D7B9014 C780000 28040C 1336F43 083403A 083015B 5D86320 53B0408 28030C 4B34593			
		278000000706000049060008				
StepC7: Setup BLE Settin     The MCU sends the Res		the BLE device, such as BD /	ADDR BD Name etc			
UART_Tx=253110493D3530 UART Rx=263100	· · · · · · · · · · · · · · · · · · ·					
UART_Tx=2031 UART_Rx=213110493D3530	306D735F544F3D36736563	300				
UART_Tx=25320406000000 UART_Rx=263200						
UART_Tx=2032 UART_Rx=21320406000000						
UART_Tx=25330615181409 UART_Rx=263300	B0BA					
UART_Tx=2033 UART_Rx=21330615181409	B0BA					
	<ul> <li>StepC8: Execute Patch_B</li> <li>The MCU writes the Physical Address 0x0020_1F80 with a value of 0x0000_0000 after which the Patch_B code will start to boot.</li> </ul>					
UART_Tx=55010000801F20000000000						
<ul> <li>StepC9: Check Patch_B Success</li> <li>Read the Physical Address 0x0060_2020 to check whether the Patch_B boot is ready or not. If Bit[10]=1, then this means that the device Patch_B boot is successful.</li> <li>Reading the Physical Address 0x0060_2020 should be bit[15]=1, bit[10]=1, bit[6]=0.</li> </ul>						
<b>JART_Tx=560120206000</b> JART_Rx=570101012020600001840000						
· ·	StepN: Connection Established					
UART_Rx=22FF11						
	StepN+1: Receive Payload Packet from cell phone					
UART_Rx=2203123456 (pay	UART_Rx=2203123456 (payload=123456)					

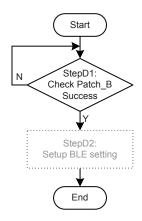


### Patch Time for the Mode_C – Patch from the MCU using the UART Interface

The patch time may be different due to various versions. The following patch time is measured for the patch version 161025A5, in which the Patch_A size=0x02C0 bytes and the Patch_B size=0x1480 bytes.

UART Baudrate=115200 bps, total time=1000ms (typical), C1+C2+C3+C4+C5+C6+C8+C9

## Initialization Flow for the Mode D – Patch from the EEPROM using the UART Interface



### Procedures for the Mode D – Patch from the EEPROM using the UART Interface

#### • StepD1: Check Patch_B Success

- Read the Physical Address 0x0060_2020 to check whether the Patch_B execution is ready or not. If Bit[10]=1, then this means that the device Patch_B boot has been successful.
- Reading the Physical Address 0x0060_2020 should be bit[15]=1, bit[10]=1, bit[6]=0.
- StepD2: Setup BLE Setting optional
  - The MCU sends the Read/Write Command to setup the BLE device, such as BD_ADDR, BD_ Name, etc.

### Example for the Mode_D – Patch from the EEPROM using the UART Interface

Text Font	Normal	Bold	Italic		
Subject	MCU_Rx MCU_Tx Patch				
<ul> <li>StepD1: Check Patch_B Success</li> <li>Read the Physical Address 0x0060_2020 to check whether the Patch_B execution is ready or not. If Bit[10]=1, then this means that the device Patch_B boot has been successful.</li> <li>Reading the Physical Address 0x0060_2020 should be bit[15]=1, bit[10]=1, bit[6]=0.</li> </ul>					
UART_Tx=560120206000 UART_Rx=57010101202060	00001840000				
<ul> <li>StepD2: Setup BLE Setting – optional</li> <li>The MCU sends the Read/Write Command to setup the BLE device, such as BD ADDR, BD Name, etc.</li> </ul>					
UART_Tx=253110493D3530306D735F544F3D3673656300 UART_Rx=263100					
UART_Tx=2031 UART_Rx=213110493D3530306D735F544F3D3673656300					
UART_Tx=25320406000000 UART_Rx=263200					
UART_Tx=2032 UART_Rx=21320406000000					
UART_Tx=25330615181409B0BA UART_Rx=263300					
UART_Tx=2033 UART_Rx=21330615181409B0BA					



Text Font	Normal	Bold	Italic	
Subject	MCU_Rx	MCU_Tx	Patch	
StepN: Connection Established				
UART_Rx=22FF11				
StepN+1: Receive Payload Packet from cell phone				
UART_Rx=2203123456 (payload=123456)				

### Patch Time for the Mode_D – Patch from the EEPROM using the UART Interface

The patch time may be different due to various versions. The following patch time is measured for the patch version 161025A5, in which the Patch_A size=0x02C0 bytes and the Patch_B size=0x1480 bytes.

First boot with the RF calibration: UART Baudrate=115200 bps, total time=850ms (typical), D1 only.

After booting the device will write the RF calibration value into the EEPROM.

Second boot without RF calibration: UART Baudrate=115200 bps, total time=350ms (typical), D1 only.



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