Features

- Frequency bands:
  - BC2302A: 315MHz, 433MHz
  - BC2302B: 315MHz, 433MHz, 868MHz, 915MHz
- Operating voltage range: 2.5V~5.5V
- 0.5μA deep sleep current with data retention
- Low RX current:
  - 3.2mA @ 433MHz
  - 4.0mA @ 868MHz
- Good reception sensitivity under 0.1% BER
  - -112dBm at 10Ksps @ 433MHz
  - -111dBm at 10Ksps @ 868MHz
- Wide RF input power range: from sensitivity to +10dBm
- Up to 20Ksps symbol rate
- Support 2-wire I²C interface for operation configuration
- Support sniff application for lower power application
- Low cost package: 8-pin SOP-EP

Applications

- RF wireless ceiling lights/fans
- Keyless entry systems
- Smart home appliances
- Door remote controllers
- Other wireless products

General Description

The BC2302x receiver devices adopt a fully-integrated, low-IF OOK receiver with an automatic gain control (AGC) function and a fully-integrated OOK demodulator. The synthesizer is formed by an integrated VCO and a fractional-N PLL to support the 315, 433, 868, and 915MHz frequency bands. The devices only require a crystal and a minimum number of passive components to fully implement an OOK receiver. With this high level of functional integration, these devices provide excellent solutions for low-cost, low power wireless applications.

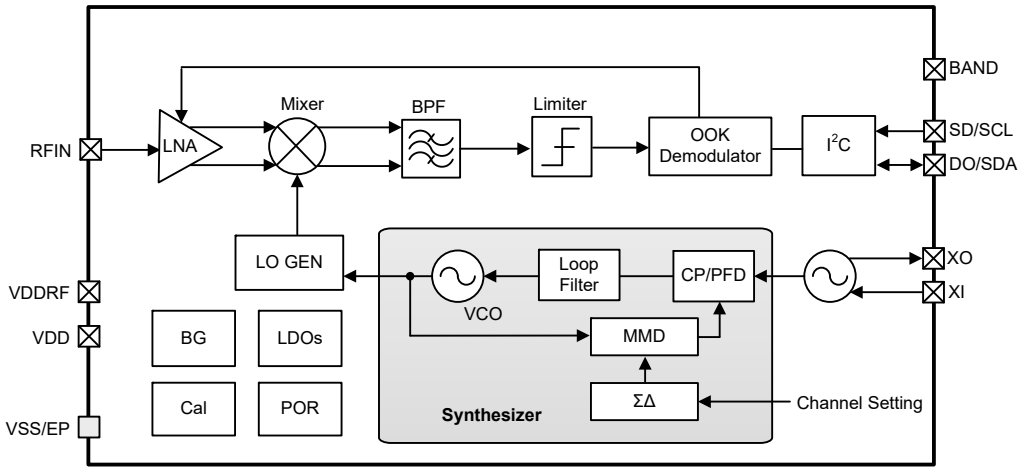
The devices achieve -112dBm and -111dBm sensitivity for the 433.92MHz and 868MHz bands, respectively. They operate from a supply voltage of 2.5 to 5.5V and typically require 3.2mA and 4.0mA at 433.92MHz and 868MHz, respectively. An agile RSSI threshold detection mechanism can further alleviate the impact of interference on OOK reception. There are two operation modes, one of which is the Auto RX mode. By properly setting certain PCB wirings, they can directly enter the RX mode. The devices also support a sniff RX mode, where the on/off RX mode function can be controlled by an MCU to achieve a lower than average power consumption using duty RX mode operation.

The BC2302 series offers two types of ICs. One is the BC2302A which covers the 315 and 433MHz bands while the BC2302B offers a choice of four frequency bands.

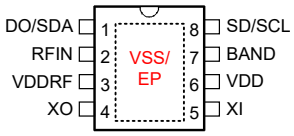
Selection Table

Part Number	Frequency Band
BC2302A	315MHz, 433MHz
BC2302B	315MHz, 433MHz, 868MHz, 915MHz

Block Diagram



Pin Assignment



BC2302A/BC2302B
8 SOP-EP-A

Pin Description

Pin No.	Pin Name	I/O	Description
1	DO/SDA(1)	DO	Demodulated data output in RX Mode
		DI/DO	I²C data line in Configuration Mode
2	RFIN	AI	RF LNA signal input
3	VDDRF	PWR	Analog positive power supply
4	XO	AO	Crystal oscillator output
5	XI	AI	Crystal oscillator input
6	VDD	PWR	Digital positive power supply.
7	BAND	DI	Pin option for frequency selection: • GND: 315MHz (BC2302A/BC2302B) • Floating: 433.92MHz (BC2302A/BC2302B) • VDD: 868.35MHz (BC2302B only)
8	SD/SCL(1)	DI	RX mode shut-down control, should be pulled low in RX Mode
		DI	I²C clock input line in Configuration Mode
—	VSS/EP(2)	PWR	Exposed pad, must be connected to ground

Legend: DI=Digital Input DO=Digital Output
AI=Analog Input AO=Analog Output
PWR=Power

Note: 1. The DO/SDA & SD/SCL pins are default connected to a pull-high resistor after a power on reset. After entering the RX mode, these pull-high resistors are disconnected automatically. An analog debounce function is added to these two pins.

2. The VSS/EP pin is located at the exposed pad.

3. The backside plate of EP shall be well soldered to ground on PCB, otherwise it will downgrade RF performance.

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to 5.5V

Input Digital Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V

Storage Temperature ..... -60°C to 150°C

Operating Temperature ..... -40°C to 85°C

ESD HBM ..... > ±2kV

*Devices being ESD sensitive. HBM (Human Body Mode) is based on MIL-STD-883.

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C, V_{DD}=5.0V, f_{XTAL}=16MHz, OOK demodulation with matching circuit, unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{OP}	Operating Temperature	—	-40	—	85	°C
V_{DD}	Operating Voltage	—	2.5	5.0	5.5	V
Current Consumption						
I_{SLP}	Current Consumption, Deep Sleep Mode	—	—	0.5	—	μA
I_{RX}	Current Consumption, RX Mode	@315MHz	—	3.4	—	mA
		@433MHz	—	3.2	—	
		@868MHz	—	4.0	—	
		@915MHz	—	4.0	—	
R_{PH}	Pull-high Resistance for I/O Ports	—	—	100	—	kΩ

A.C. Characteristics

Ta=25°C, V_{DD}=5.0V, f_{XTAL}=16MHz, OOK demodulation with matching circuit, unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Receiver Characteristics						
f_{RF}	RF Frequency Range	BC2302A/BC2302B	—	315	—	MHz
		BC2302A/BC2302B	—	433.92	—	
		BC2302B only	—	868.35	—	
		BC2302B only	—	915	—	
SR	Symbol Rate	OOK Modulation	0.5	—	20	Ksps
P_{SENS}	RX Sensitivity – 315MHz (Instrument: Keysight E4438C)	SR=1Ksps, BER=0.1%	—	-113	—	dBm
		SR=10Ksps, BER=0.1%	—	-113	—	
	RX Sensitivity – 433.92MHz (Instrument: Keysight E4438C)	SR=1Ksps, BER=0.1%	—	-112	—	
		SR=10Ksps, BER=0.1%	—	-112	—	
	RX Sensitivity – 868.35MHz (Instrument: Keysight E4438C)	SR=1Ksps, BER=0.1%	—	-111	—	
		SR=10Ksps, BER=0.1%	—	-111	—	
	RX Sensitivity – 915MHz (Instrument: Keysight E4438C)	SR=1Ksps, BER=0.1%	—	-110	—	
		SR=10Ksps, BER=0.1%	—	-110	—	
SE_{RX}	Receiver Spurious Emission	25MHz ~ 1GHz	—	—	-57	dBm
		Above 1GHz	—	—	-47	
	Blocking Immunity	±2MHz offset	—	40	—	dBc
		±10MHz offset	—	64	—	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Cof_{ST}	Configuration Mode Settling Time (Deep Sleep to Configuration Mode)	49US XO	—	2	—	ms
		SMD3225 XO	—	3	—	ms
RX_{ST}	RX Mode Settling Time (Deep Sleep Mode to RX Mode Data Out)	49US XO	—	2	—	ms
		SMD3225 XO	—	3	—	
LO Characteristics						
f_{LO}	Frequency Coverage Range	BC2302A/BC2302B	300	—	360	MHz
		BC2302A/BC2302B	390	—	450	
		BC2302B only	850	—	935	
	Frequency Resolution	—	—	—	0.1	kHz
	Synthesizer Locking Time	—	—	130	—	μs
Crystal Oscillator Characteristics						
f_{XTAL}	Crystal frequency	General case	—	16	—	MHz
t_{SU}	X'tal Startup Time	f_{XTAL}=16MHz(Note)	—	0.5	—	ms
ESR	X'tal Equivalent Series Resistance	—	—	—	100	Ω
C_L	X'tal Load Capacitance	—	—	16	—	pF
TOL	X'tal Tolerance	—	-20	—	+20	ppm

Note: X'tal start-up time is characterized by a reference design using the 49US XO.

I²C Characteristics

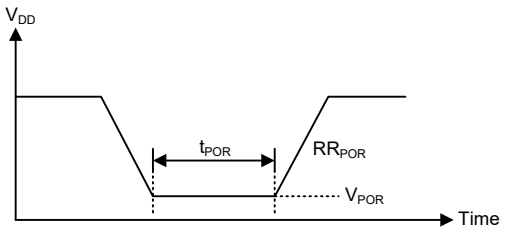
Ta=-40°C~85°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	Serial Clock Frequency	—	—	—	1	MHz
t_{BUF}	Bus Free Time between Stop and Start Condition	SCL=1MHz	250	—	—	ns
t_{LOW}	SCL Low Time	SCL=1MHz	500	—	—	ns
t_{HIGH}	SCL High Time	SCL=1MHz	500	—	—	ns
$t_{su(DAT)}$	Data Setup Time	SCL=1MHz	100	—	—	ns
$t_{su(STA)}$	Start Condition Setup Time	SCL=1MHz	250	—	—	ns
$t_{su(STO)}$	Stop Condition Setup Time	SCL=1MHz	250	—	—	ns
$t_{h(DAT)}$	Data Hold Time	SCL=1MHz	100	—	—	ns
$t_{h(STA)}$	Start Condition Hold Time	SCL=1MHz	250	—	—	ns
$t_{r(SCL)}$	Rise Time of SCL Signal	SCL=1MHz	—	—	100	ns
$t_{f(SCL)}$	Fall Time of SCL Signal	SCL=1MHz	—	—	100	ns
$t_{r(SDA)}$	Rise Time of SDA Signal	SCL=1MHz	—	—	100	ns
$t_{f(SDA)}$	Fall Time of SDA Signal	SCL=1MHz	—	—	100	ns

Power on Reset Characteristics

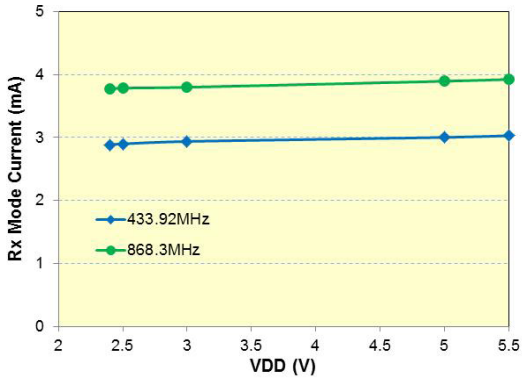
Ta=25°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	—	—	—	100	mV
RR_{POR}	V_{DD} Rising Rate to Ensure Power-on Reset	—	0.035	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} Stays at V_{POR} to Ensure Power-on Reset	—	1	—	—	ms

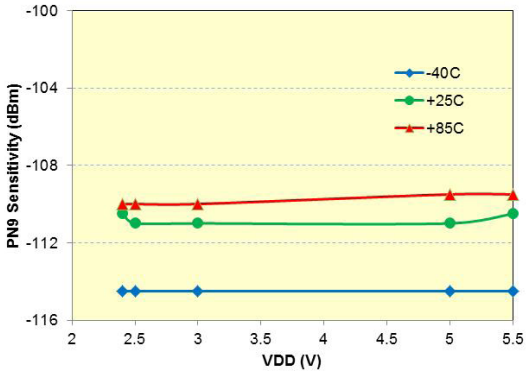


Typical Characteristics

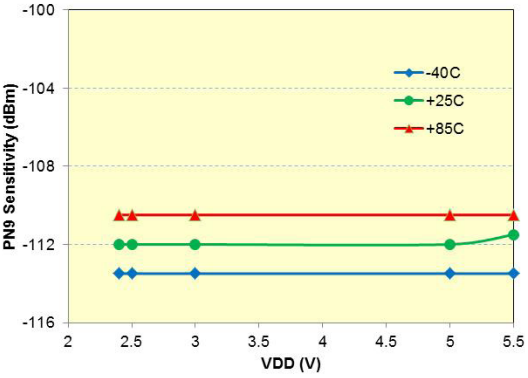
Ta=25°C, V_{DD}=5.0V, f_{XTAL}=16MHz, OOK demodulation with matching circuit, unless otherwise noted



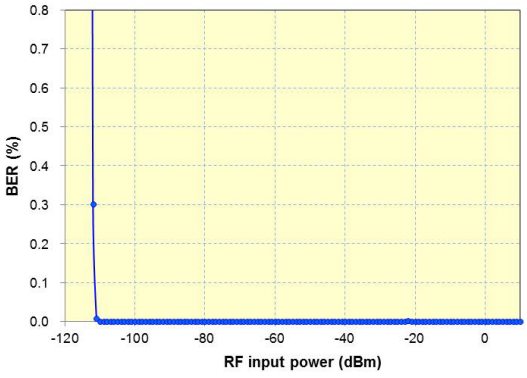
Current vs. Supply voltage (433.92 and 868.3MHz)



Sensitivity vs. Supply voltage & Temperature (433.92MHz)



Sensitivity vs. Supply voltage & Temperature (868.3MHz)



BER vs. RF input power (433.92MHz)

Functional Description

The BC2302x devices are ultra-low power, high performance, low-cost OOK receivers suitable for use in wireless applications with a frequency of 315, 433, 868, 915MHz respectively. The devices are formed by a low-IF receiver, followed by an OOK demodulator and a fractional-N synthesizer. They only require a crystal and a minimum number of passive components to implement an OOK receiver. These devices provide two operation modes. One is the Auto RX mode. By properly setting the PCB pin wirings, they can directly enter the RX mode. Another is the sniff RX mode where the on/off RX mode function can be controlled by an MCU to achieve a lower than average power consumption.

OOK RF Receiver

The BC2302x devices adopt a fully-integrated, low-IF receiver architecture. The received RF signal is first amplified by a low noise amplifier (LNA), after which the frequency is reduced to an intermediate frequency (IF). The IF signal is filtered by a channel-selected filter which rejects the unwanted out-of-band interference signals and image signal. After the BPF stage, the desired IF signal is amplified by the limiter amplifier which generates a received-signal-strength-indicator (RSSI) signal.

The devices feature an automatic gain control (AGC) unit which adjusts the front-end gain according to the RSSI. The AGC can increase the dynamic range of the RSSI and enable the devices to receive a wide dynamic range RF signal.

The OOK one/zero type data is generated by comparing the RSSI signal to a manipulated threshold. This threshold is crucial to the performance of OOK demodulation. The devices adopt an agile threshold detection mechanism. It can alleviate the impact of the interference on OOK reception quality. The agile threshold detection mechanism can reduce glitches when there is no RF signal or when long zero data streams are received. It also includes a fast tracking threshold to offer good immunity from co-channel interferences.

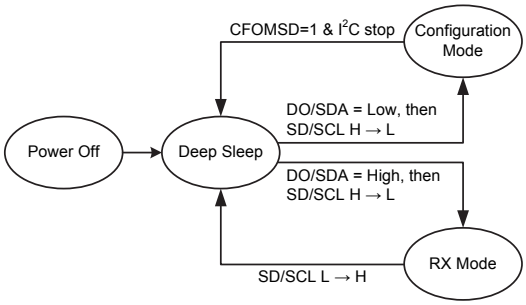
Operation Modes

The devices provide four operation modes, power off mode, deep sleep mode, RX mode and configuration mode.

In the deep sleep mode, there is less than 1μA of sleep mode leakage current with register data retention.

In the RX Mode, the devices execute normal RX operations that receive incoming RF signals from the antenna and then output the demodulated data onto the DO/SDA pin. There are two types of RX mode, one is the Auto RX mode and the other is the sniff RX mode.

In the Configuration Mode, the devices are operated as I^2C slaves and are programmed by an external MCU. Users can select the desired RX channel by configuring the internal registers. After the configuration has completed, the devices will return to the deep sleep mode by setting the CFOMSD bit high.



Operation Mode Switching

Note: The CFOMSD bit will be cleared to zero automatically when the device leaves the configuration mode.

Mode	Register Retention	5V	Crystal Oscillator	Synthesizer &VCO	RX
Power Off	No	OFF	OFF	OFF	OFF
Deep Sleep Mode	Yes	ON	OFF	OFF	OFF
RX Mode	Yes	ON	ON	ON	ON
Configuration Mode	Yes	ON	ON	OFF	OFF

Auto RX Mode

The devices provide an Auto RX Mode. After power-on, the devices will enter the RX mode after a 30ms delay from the power-on reset. In this mode, frequency selection is achieved using a pin option together with external PCB wirings as shown in the following table.

BAND Pin	Selected Frequency For BC2302A	Selected Frequency For BC2302B
GND	315MHz	315MHz
Floating	433.92MHz	433.92MHz
V_{DD}	Unavailable	868.35MHz

To directly enter this mode, the SD/SCL pin should be connected to ground and the BAND pin should be connected to the required level before power is applied.

Note that there is only one method for the device to leave the RX mode which is to remove the power.

Sniff RX Mode

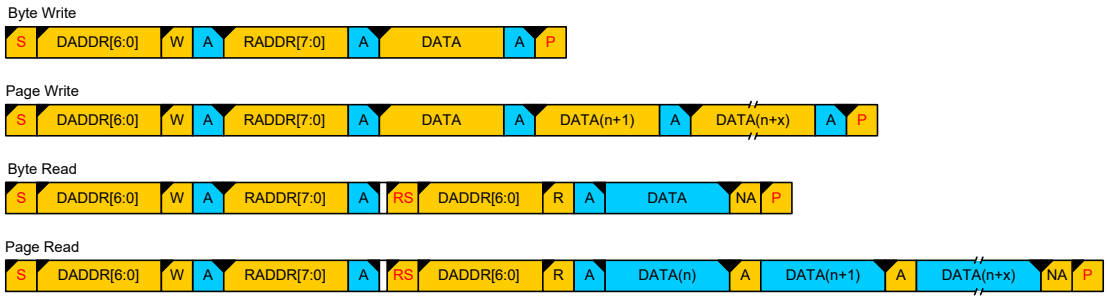
The devices also provide a Sniff RX mode as it is controlled by an MCU. The SD/SCL pin defaults to a pull-high state. After power-on the devices will enter the deep sleep mode. An MCU could control the SD/SCL pin to make it enter or leave the RX mode. With additional SD/SCL control, users can optimize the average power consumption based on their applications.

Configuration Mode

The devices include an I²C serial interface, which is used for bidirectional, two-line communication between multiple I²C devices. The two lines of this interface are the serial data line, SDA, and the serial clock line, SCL. Both lines are equipped with analog de-bounce functions. After a power on reset, these two pins are pulled to VDD by default using internal pull-high resistors. When entering the RX mode, the pull-high resistors are disconnected.

The devices support the I²C format for byte write, page write, byte read and page read formats. Every byte placed onto the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit, MSB, first.

It should be noted that the I2C is a non-standard I2C interface, which only supports a single device for connection.



Bus Direction: : Host to device; : Device to host;

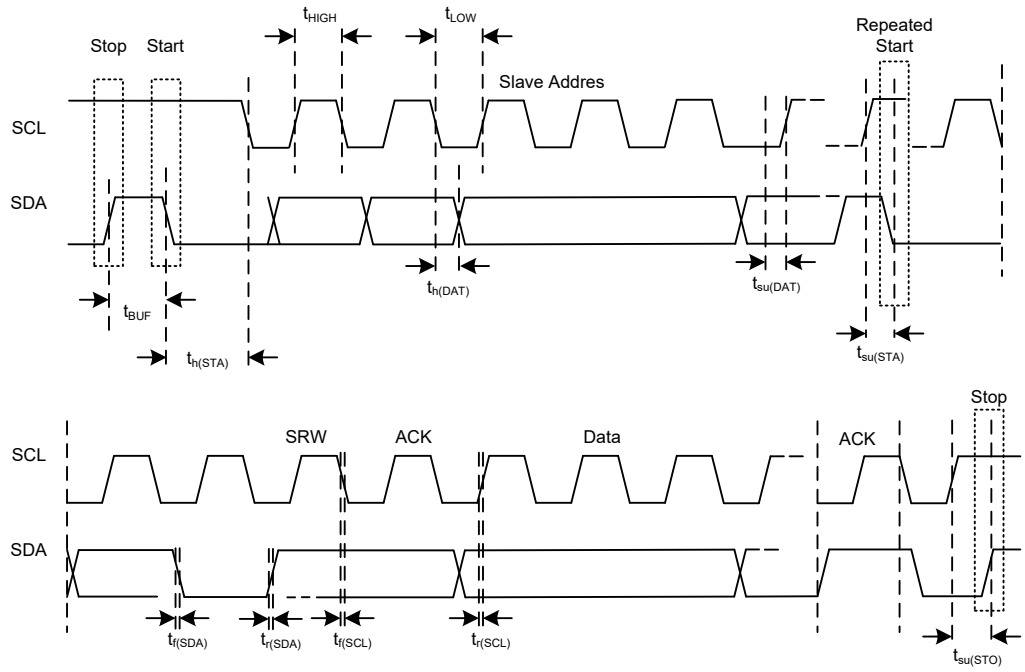
Symbol Definitions: S: Start; RS: Repeated Start; P: Stop;

DADDR[6:0]: Device Address, 23h;

R:Read(1); W: Write(0);

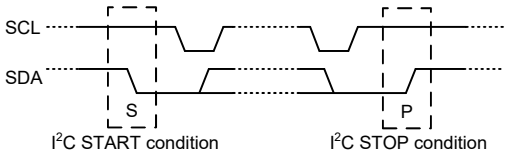
RADDR[7:0]: register address;

A: ACK(0); NA: NAK(1)



I²C Communication Timing Diagram

I²C START and STOP Conditions

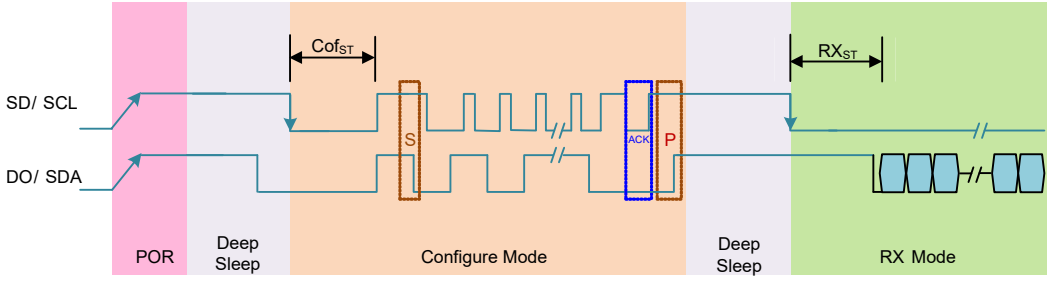


- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus remains busy if a Repeated START (RS) is generated instead of a STOP condition. The START (S) and Repeated START (RS) conditions are functionally identical.

Configuration Mode Switching and Timing

As shown in the following diagram, when SDA is low and a SCL falling edge occurs, the device changes from the Deep Sleep Mode to the Configuration Mode after a Cof_{ST} delay time. If the SCL level remains high for a time greater than or equal to 20ms, the device will be forced to leave the Configuration Mode.

If the devices are connected to an MCU through the I²C interface, users can set the CFOMSD bit of the register, at address 42h, to leave the Configuration Mode.



Entering and Leaving Configuration Mode Timing Diagram

Register Map

When connected to an external MCU, the device's RF frequency can be setup using a series of internal registers in the Configuration Mode. The register data is written to and read from the devices using their internal I²C interface. The following provides a summary of all internal registers and their detailed descriptions.

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
05h	CFG0	Setting 0							
10h	OM	—	BAND_SEL[1:0]		—	—	—	—	—
11h	CFG1	Setting 1							
12h	SX1	—	D_N[6:0]						
13h	SX2	D_K[7:0]							
14h	SX3	D_K[15:8]							
15h	SX4	—	—	—	—	D_K[19:16]			
17h	CFG2	Setting 2							
18h	CFG3	Setting 3							
19h	CFG4	Setting 4							
39h	CFG5	Setting 5							
42h	I2C1	—	—	—	—	—	—	—	CFOMSD
52h	—	Reserved							

Note: The addresses which are not listed in this table are reserved for future use, it is suggested not to change their initial values by any methods.

For the CFG0~CFG5 registers, the recommended values are listed as follow.

Register \ Frequency	315MHz	433.92MHz	868.35MHz	915MHz
CFG0	07h@Symbol rate ≤ 20Ksps; 04h@Symbol rate =20Ksps			
CFG1	F5h	F5h	F6h	F6h
CFG2	7Fh	7Fh	7Fh	7Fh
CFG3	74h	74h	D0h	D0h
CFG4	8Dh	8Dh	91h	91h
CFG5	C2h	C2h	C2h	C2h

The recommended value for the register at 52h is listed below:

Addr.	Setting
52h	315MHz Band: 84h 433/868/915MHz Bands: 80h

- **OM – Operation Mode Control Register (Addr: 10H)**

Bit	7	6	5	4	3	2	1	0
Name	—	BAND_SEL[1:0]		—	—	—	—	—
R/W	—	R/W		—	—	—	—	—
POR	0	0	0	0	0	0	0	0

Bit 7 Reserved bit, cannot be changed

Bit 6~5 **BAND_SEL[1:0]**: Band selection

00: 300~360MHz Band

01: 390~450MHz Band

10: Reserved

11: 850~935MHz Band – BC2302B only

Note that for the BC2302A, these two bits cannot be set to "10"/"11"

Bit 4~0 Reserved bit, cannot be changed

- **SX1 – Fractional-N Synthesizer Control Register 1 (Addr: 12H)**

Bit	7	6	5	4	3	2	1	0
Name	—	D_N[6:0]						
R/W	—	R/W						
POR	0	0	1	0	1	0	1	1

Bit 7 Note that this bit must be set to "1"

Bit 6~0 **D_N[6:0]**: RF channel frequency integer number code

$D\_N[6:0]=Floor\left(\frac{f_{RF}-f_{IF}}{f_{XTAL}\div 2}\times 0.8\right)\times M$, (315MHz: M=2, Other Bands: M=1)

For example:

f_{XTAL}=16MHz, RF channel frequency(f_{RF})=315MHz, Intermediate Frequency (f_{IF})=200kHz

→ (315MHz-0.2MHz)/(16MHz/2)×0.8×2=62.96

→ D_N=62

→ Dec2Bin(62)=011_1110

f_{XTAL}=16MHz, RF channel frequency(f_{RF})=433.92MHz, Intermediate Frequency (f_{IF})=200kHz

→ (433.92MHz-0.2MHz)/(16MHz/2)×0.8=43.372

→ D_N=43

→ Dec2Bin(43)=010_1011

- **SX2 – Fractional-N Synthesizer Control Register 2 (Addr: 13H)**

Bit	7	6	5	4	3	2	1	0
Name	D_K[7:0]							
R/W	R/W							
POR	1	0	1	1	0	1	1	1

Bit 7~0 **D_K[7:0]**: RF channel frequency fractional number code lowest byte

- **SX3 – Fractional-N Synthesizer Control Register 3 (Addr: 14H)**

Bit	7	6	5	4	3	2	1	0
Name	D_K[15:8]							
R/W	R/W							
POR	1	1	1	1	0	0	1	1

Bit 7~0 **D_K[15:8]**: RF channel frequency fractional number code medium byte

- **SX4 – Fractional-N Synthesizer Control Register 4 (Addr: 15H)**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	D_K[19:16]			
R/W	—	—	—	—	R/W			
POR	0	1	1	0	0	1	0	1

Bit 7~4 Reserved bit, cannot be changed

Bit 3~0 **D_K[19:16]**: RF channel frequency fractional number code highest byte

$D\_K[19:0]=\text{Floor}\ \{(\frac{f_{RF}-f_{IF}}{f_{XTAL}\div 2}\times 0.8\times M - D\_N[6:0])\times 2^{20}\}$, (315MHz: M=2, Other Bands: M=1)

For example:

f_{XTAL}=16MHz, RF channel frequency(f_{RF})=315MHz, Intermediate Frequency (f_{IF})=200kHz

→ (315MHz-0.2MHz)/(16MHz/2)×0.8×2=62.96

→ D_K=0.96×2^{20}=1006632

→ Dec2Bin(1006632)=1111_0101_1100_0010_1000

f_{XTAL}=16MHz, RF channel frequency(f_{RF})=433.92MHz, Intermediate Frequency (f_{IF})=200kHz

→ (433.92MHz-0.2MHz)/(16MHz/2)×0.8=43.372

→ D_K=0.372×2^{20}=390070

→ Dec2Bin(390070)=0101_1111_0011_1011_0110

- **I2C1 – I²C Control Register 1 (Addr: 42H)**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	CFOMSD
R/W	—	—	—	—	—	—	—	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~1 Reserved bit, cannot be changed

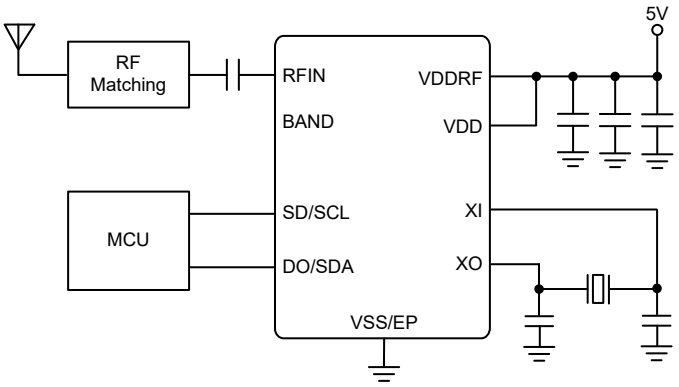
Bit 0 **CFOMSD**: Configuration Mode shut down control

0: No operation

1: Exit Configuration Mode

In the configuration mode the devices can be forced to leave this mode by first setting the CFOMSD bit high and then followed by an I²C stop condition. After leaving the Configuration Mode the CFOMSD bit will be reset to zero automatically.

Application Circuits



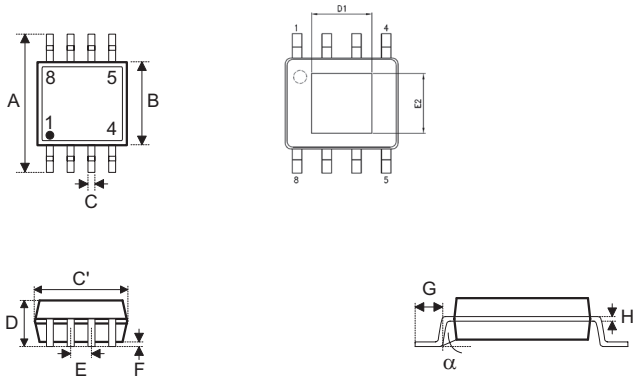
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

8-pin SOP-EP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.020
C'	—	0.193 BSC	—
D	—	—	0.069
D1	0.076	—	0.090
E	—	0.050 BSC	—
E2	0.076	—	0.090
F	0.000	—	0.006
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.00 BSC	—
B	—	3.90 BSC	—
C	0.31	—	0.51
C'	—	4.90 BSC	—
D	—	—	1.75
D1	1.94	—	2.29
E	—	1.27 BSC	—
E2	1.94	—	2.29
F	0.00	—	0.15
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°

Note: For this package type, refer to the package information provided here, which will not be updated by the Holtek website.

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